

## 100V N-Channel MOSFET

### ❖ GENERAL DESCRIPTION

These N-Channel enhancement mode power field effect transistors are produced using DMOS technology.

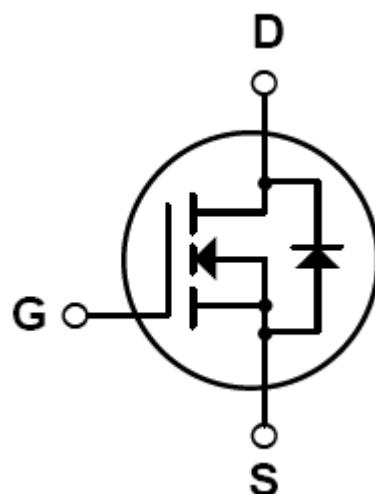
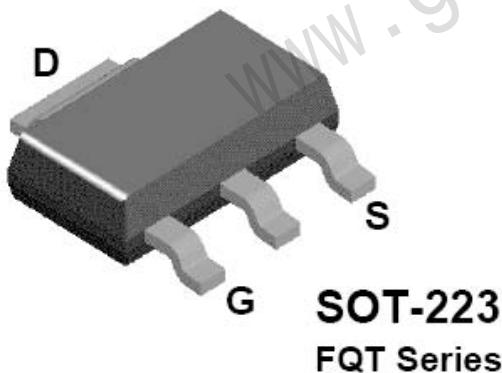
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

### ❖ FEATURES

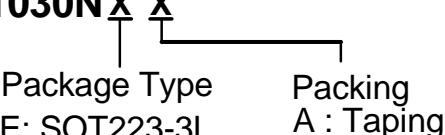
- 3.0A, 100V,  $R_{DS(on)} = 0.19\Omega$  @ $V_{GS} = 10$  V
- Low gate charge ( typical 5.8 nC)
- Low Crss ( typical 10 pF)
- Fast switching
- Improved dv/dt capability

### ❖ PIN ASSIGNMENT

The package of AM1030N is SOT-223; the pin assignment is given by:



❖ ORDER/MARKING INFORMATION

Order Information	Top Marking
<b>AM1030N X X</b> 	Logo <b>AM</b> 1 0 3 0 N → Part number Y WWX → ID code:internal WW:01~52 Year: A=2010 1=2011

❖ ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DSS}$	100	V
Drain Current Continuous ( $T_c = 25^\circ\text{C}$ )	$I_D$	3.0	A
Continuous ( $T_c = 70^\circ\text{C}$ )		2.36	A
Drain Current – Pulsed (Note 1)	$I_{DM}$	6.8	A
Gate-Source Voltage	$V_{GSS}$	$\pm 25$	V
Single Pulsed Avalanche Energy (Note 2)	$E_{AS}$	50	mJ
Avalanche Current (Note 1)	$I_{AR}$	3.0	A
Repetitive Avalanche Energy (Note 1)	$E_{AR}$	0.2	mJ
Peak Diode Recovery $dv/dt$ (Note 3)	$dv/dt$	6.0	V/ns
Power Dissipation ( $T_c = 25^\circ\text{C}$ )	$P_D$	2.0	W
Derate above $25^\circ\text{C}$		0.016	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	$T_L$	300	$^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient (Note 4)	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

Note1: Pulse width limited by max. junction temperature

Note2: Package limitation current is 75A

Note3: Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board

Note4: When mounted on the minimum pad size recommended (PCB Mount)

### ❖ ELECTRICAL CHARACTERISTICS

( $T_C = 25^\circ\text{C}$ , unless otherwise specified)

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, I_{\text{D}} = 250 \mu\text{A}$	100	-	-	V
Breakdown Voltage Temperature Coefficient	$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	$I_{\text{D}} = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.1	-	$\text{V}/^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = 100 \text{ V}, V_{\text{GS}} = 0 \text{ V}$	-	-	1	$\mu\text{A}$
		$V_{\text{DS}} = 80 \text{ V}, T_C = 125^\circ\text{C}$	-	-	10	$\mu\text{A}$
Gate-Body Leakage Current, Forward	$I_{\text{GSSF}}$	$V_{\text{GS}} = 25 \text{ V}, V_{\text{DS}} = 0 \text{ V}$	-	-	100	nA
Gate-Body Leakage Current, Reverse	$I_{\text{GSSR}}$	$V_{\text{GS}} = -25 \text{ V}, V_{\text{DS}} = 0 \text{ V}$	-	-	-100	nA
On Characteristics						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = 250 \mu\text{A}$	1	-	2.5	V
Static Drain-Source On-Resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}} = 10 \text{ V}, I_{\text{D}} = 0.85 \text{ A}$	-	0.13	0.19	$\Omega$
Forward Transconductance	$g_{\text{FS}}$	$V_{\text{DS}} = 40 \text{ V}, I_{\text{D}} = 0.85 \text{ A}$ (Note 4)	-	1.85	-	S
Dynamic Characteristics						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = 25 \text{ V}, V_{\text{GS}} = 0 \text{ V}, f = 1.0 \text{ MHz}$	-	190	250	pF
Output Capacitance	$C_{\text{oss}}$		-	60	75	pF
Reverse Transfer Capacitance	$C_{\text{rss}}$		-	10	13	pF
Switching Characteristics						
Turn-On Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}} = 50 \text{ V}, I_{\text{D}} = 7.3 \text{ A}, R_G = 25 \Omega$ (Note 4, 5)	-	7	25	ns
Turn-On Rise Time	$t_r$		-	24	60	ns
Turn-Off Delay Time	$t_{\text{d(off)}}$		-	13	35	ns
Turn-Off Fall Time	$t_f$		-	19	50	ns
Total Gate Charge	$Q_g$	$V_{\text{DS}} = 80 \text{ V}, I_{\text{D}} = 7.3 \text{ A}, V_{\text{GS}} = 10 \text{ V}$ (Note 4, 5)	-	5.8	7.5	nC
Gate-Source Charge	$Q_{\text{gs}}$		-	1.4	-	nC
Gate-Drain Charge	$Q_{\text{gd}}$		-	2.5	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
Maximum Continuous Drain-Source Diode Forward Current	$I_s$		-	-	3.0	A
Maximum Pulsed Drain-Source Diode Forward Current	$I_{\text{SM}}$		-	-	6.8	A
Drain-Source Diode Forward Voltage	$V_{\text{SD}}$	$V_{\text{GS}} = 0 \text{ V}, I_s = 1.7 \text{ A}$	-	-	1.5	V
Reverse Recovery Time	$t_{\text{rr}}$	$V_{\text{GS}} = 0 \text{ V}, I_s = 7.3 \text{ A}, dI/F / dt = 100 \text{ A}/\mu\text{s}$ (Note 4)	-	70	-	ns
Reverse Recovery Charge	$Q_{\text{rr}}$		-	150	-	nC

Note1: Repetitive Rating: Pulse width limited by maximum junction temperature

Note2:  $L = 26\text{mH}$ ,  $I_{\text{AS}} = 1.7\text{A}$ ,  $V_{\text{DD}} = 25\text{V}$ ,  $R_G = 25 \Omega$ , Starting  $T_J = 25^\circ\text{C}$

Note3:  $I_{\text{SD}} \leq 7.3\text{A}$ ,  $dI/dt \leq 300\text{A}/\mu\text{s}$ ,  $V_{\text{DD}} \leq \text{BV}_{\text{DSS}}$ , Starting  $T_J = 25^\circ\text{C}$

Note4: Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$

Note5: Essentially independent of operating temperature

❖ TYPICAL CHARACTERISTICS

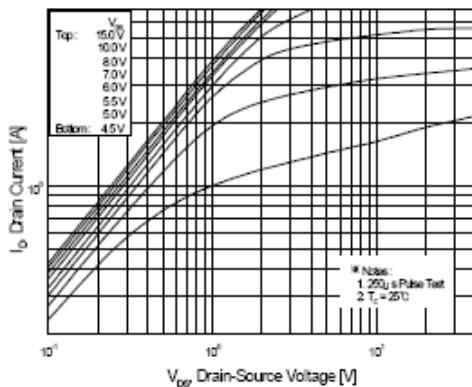


Figure 1. On-Region Characteristics

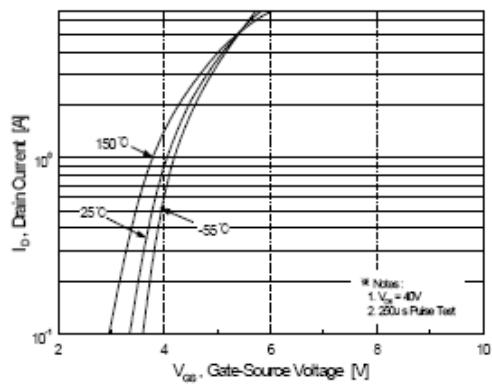


Figure 2. Transfer Characteristics

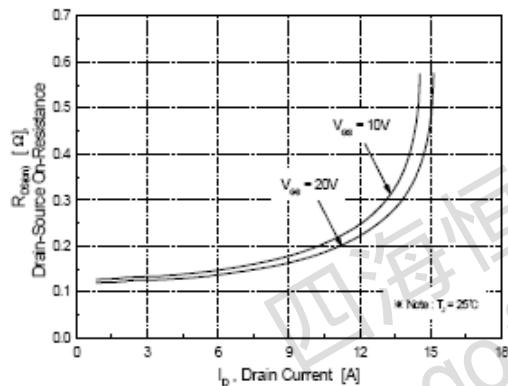


Figure 3. On-Resistance Variation vs.  
Drain Current and Gate Voltage

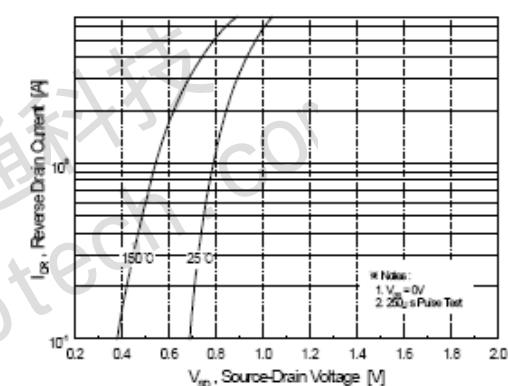


Figure 4. Body Diode Forward Voltage  
Variation vs. Source Current  
and Temperature

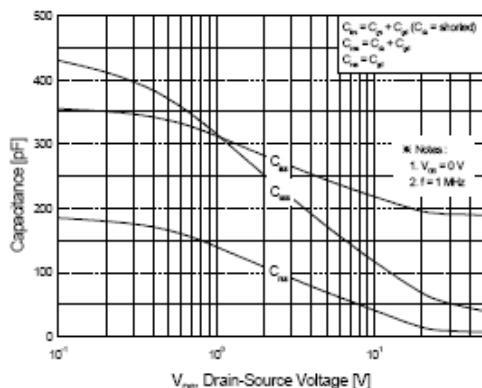


Figure 5. Capacitance Characteristics

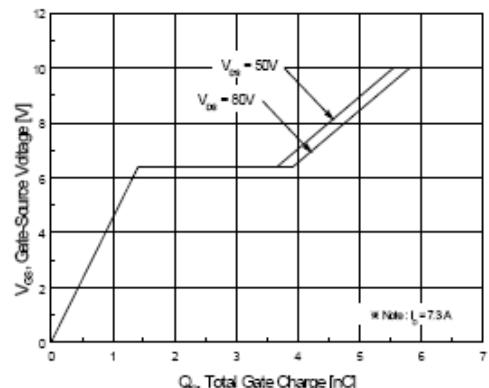


Figure 6. Gate Charge Characteristics

❖ TYPICAL CHARACTERISTICS (CONTINUES)

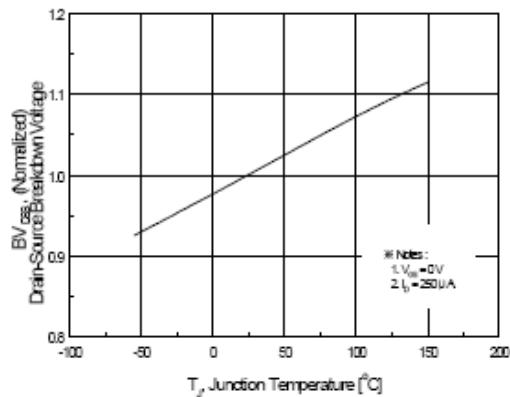


Figure 7. Breakdown Voltage Variation  
vs. Temperature

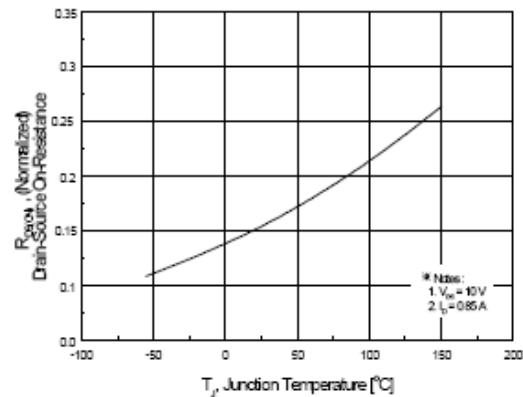


Figure 8. On-Resistance Variation  
vs. Temperature

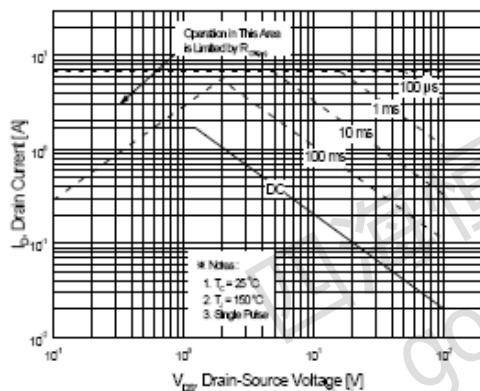


Figure 9. Maximum Safe Operating Area

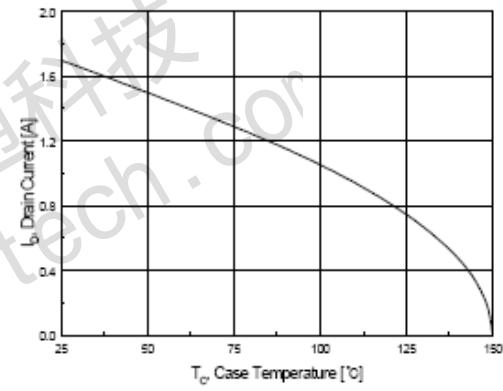


Figure 10. Maximum Drain Current  
vs. Case Temperature

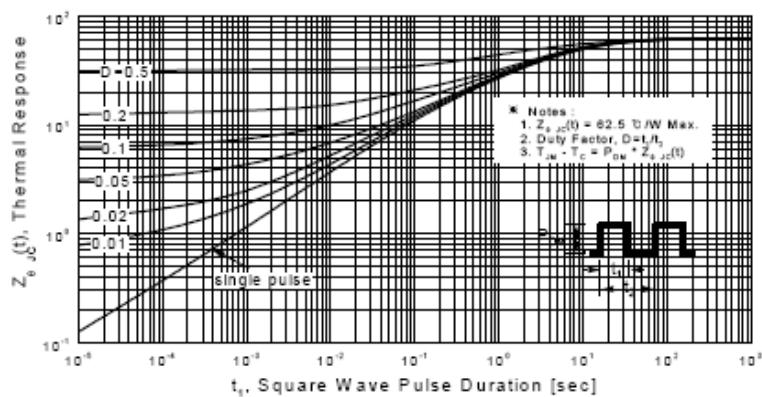
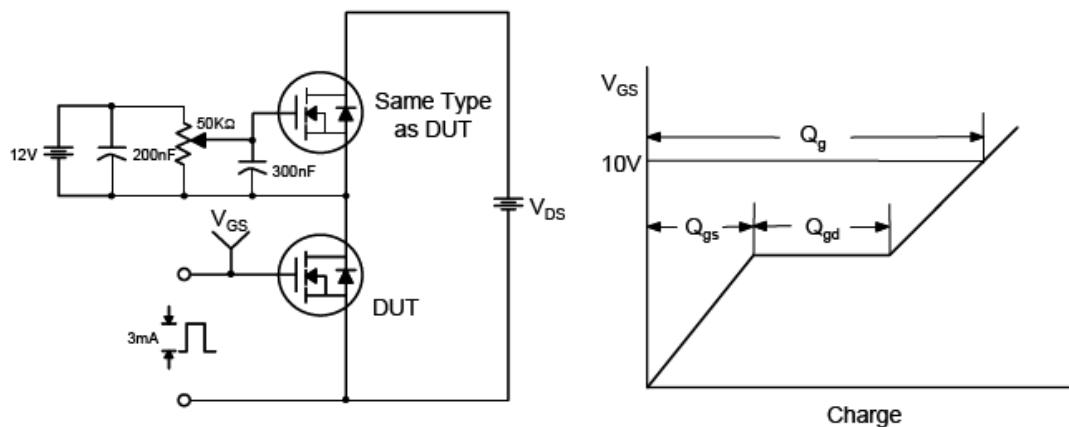
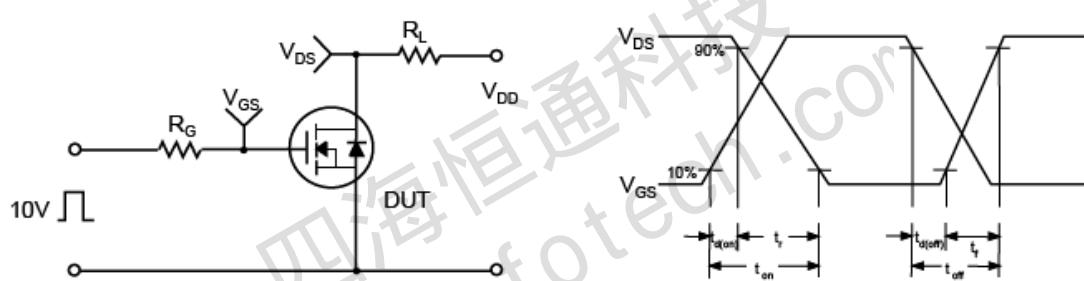


Figure 11. Transient Thermal Response Curve

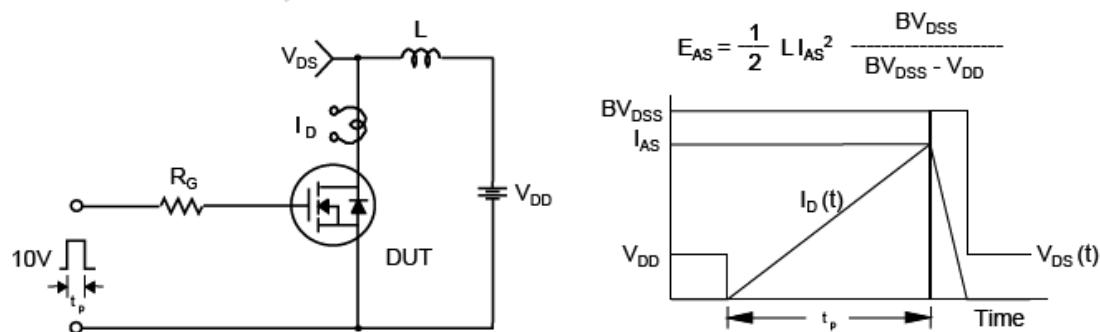
Gate Charge Test Circuit & Waveform



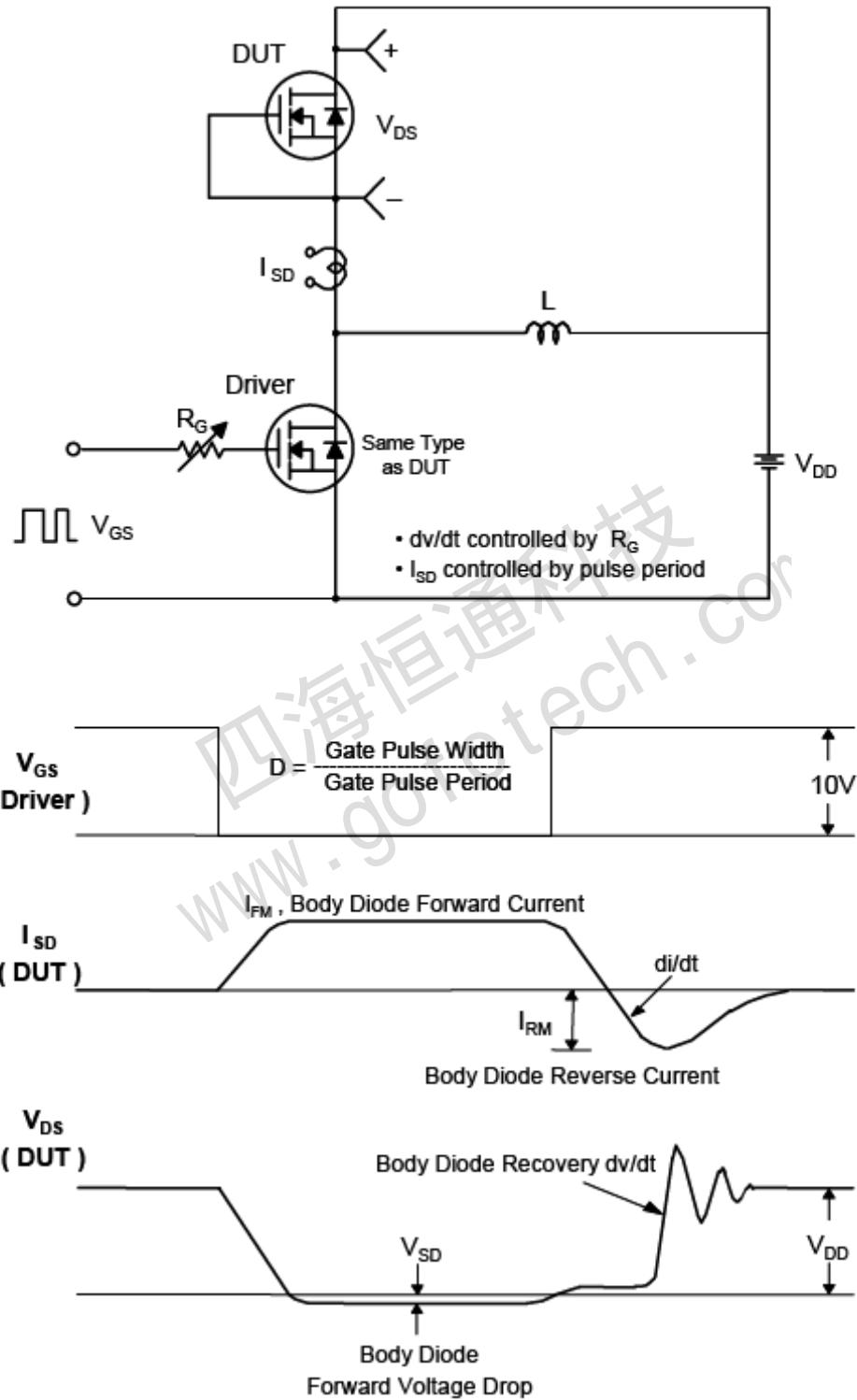
Resistive Switching Test Circuit & Waveforms



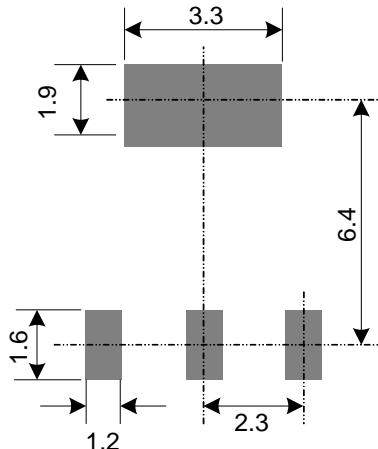
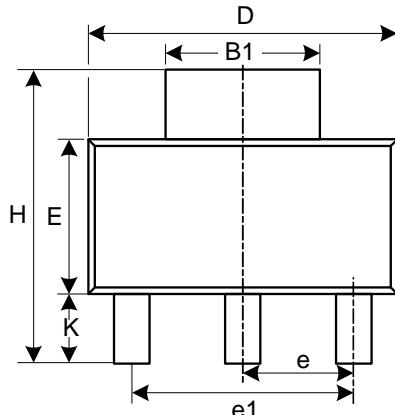
Unclamped Inductive Switching Test Circuit & Waveforms



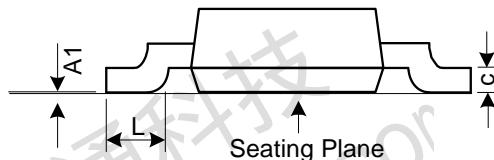
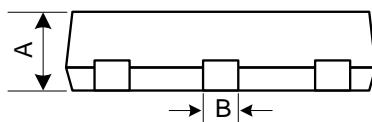
Peak Diode Recovery dv/dt Test Circuit & Waveforms



## ❖ PACKAGE OUTLINES



Land Pattern Recommendation (Unit: mm)



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.8	-	-	0.071
A1	0.02	0.06	0.1	0.001	0.002	0.004
B	0.66	0.75	0.84	0.026	0.03	0.033
B1	2.9	3	3.1	0.114	0.118	0.122
C	0.23	0.315	0.35	0.009	0.012	0.014
D	6.3	6.5	6.7	0.248	0.256	0.264
E	3.3	3.5	3.7	0.13	0.138	0.146
H	6.7	7	7.3	0.264	0.278	0.287
L	0.75	-	-	0.03	-	-
K	1.5	1.75	2	0.059	0.069	0.079
e	2.3 Basic			0.091 Basic		
e1	4.6 Basic			0.181 Basic		

JEDEC outline: TO-261 AB