N-Channel 40V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY				
V _{DS} (V)	$V) \qquad \eta_{DS(on)}(\Omega) \qquad I_D(A)$			
40	$0.086 @V_{CS} = 10 V$	3.5		
	$0.128 @V_{CS} = 4.5V$	2.9		

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SC70-6 saves board space
- Fast switching speed
- High performance trench technology

	SC	70-6		$D_{\scriptscriptstyle{1}}$
	Top	View	•	γ'
		_	_	
РЩ	1	6	□ D	$G_1 \circ \sqcup \vdash \uparrow$
рЩ	2	5	⊞ D	. Н
GЩ	3	4	s	S_1
				N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)					
Parameter Parameter			Maximum	Units	
Drain-Source Voltage			40	V	
Gate-Source Voltage			±20	V	
C . D . C . A	T _A =25°C	T_	3.5		
Continuous Drain Current ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	1D	2.9	A	
Pulsed Drain Current ^b		I_{DM}	±20	l	
Continuous Source Current (Diode Conduction) ^a		I_S	1.6	A	
D D: : ,: a	$T_A=25^{\circ}C$	D_	1.56	W	
Power Dissipation ^a	T_{A} =25°C T_{A} =70°C	I D	0.81	• • •	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Maximum	Units		
M · I	t <= 5 sec	D	100	00/MI	
Maximum Junction-to-Ambient ^a	Steady-State	R_{THJA}	166	°C/W	

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)							
Demonstra	6.11		Limits			TT *4	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Cate-Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS}$, $I_D=250$ uA	1			V	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			±100	nA	
Zero Cate Voltage Drain Current	IDSS	$V_{DS} = 32 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA	
	IDSS	$V_{DS} = 32 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^{\circ}\text{C}$			10	uA	
On-State Drain Current ^A	I _{D(on)}	$V_{DS}=5V$, $V_{GS}=4.5V$	10			Α	
D : C O D : A	******	$V_{GS} = 10 \text{ V}, I_D = 3.5 \text{ A}$			86	mΩ	
Drain-Source On-Resistance ^A	fDS(on)	$V_{GS} = 4.5 \text{ V}, I_D = 2.9 \text{ A}$			128	111.2	
Forward Tranconductance ^A	gs	$V_{DS} = 10 \text{ V, } I_D = 3.5 \text{ A}$		11.3		S	
Diode Forward Voltage	Vsd	$I_S = 1.6 A, V_{GS} = 0 V$		0.75		V	
Dynamic ^b					•		
Total Gate Charge	$Q_{\!\scriptscriptstyle g}$	$V_{DS} = 10 \text{ V}, V_{CS} = 4.5 \text{ V}, I_D = 3.5 \text{ A}$		7.5		nC	
Gate-Source Charge	Qgs			0.6			
Gate-Drain Charge	Qgd			1.0			
Input Capacitance	Gss	N/ -15X/X/ -0X/		720		рF	
Output Capacitance	Coss	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$ f		165			
Reverse Transfer Capacitance	Crss	= 1MHz		60			
Turn-On Delay Time	td(on)	$V_{DD} = 10 \text{ V}, R_L = 15 \Omega, I_D = 1 \text{ A}, V_{GEN} = 4.5 \text{ V}$		8		ns	
Rise Time	t _r			24			
Turn-Off Delay Time	td(off)			35			
Fall-Time	tf			10			

Notes

- a. Pulse test: $PW \le 300us duty cycle \le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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