

N-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology

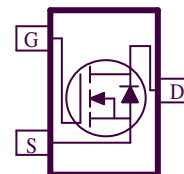
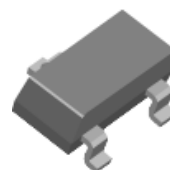


ESD Protected

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.076 @ $V_{GS} = 4.5V$	3.4
	0.103 @ $V_{GS} = 2.5V$	2.9



RoHS
COMPLIANT
HALOGEN
FREE
Available



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current ^a	$T_A = 25^\circ C$	I_D	3.4	A
	$T_A = 70^\circ C$		2.2	
Pulsed Drain Current ^b		I_{DM}	10	
Continuous Source Current (Diode Conduction) ^a		I_S	1.6	A
Power Dissipation ^a	$T_A = 25^\circ C$	P_D	1.25	W
	$T_A = 70^\circ C$		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{THJA}	100	$^\circ C/W$
	Steady-State		166	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

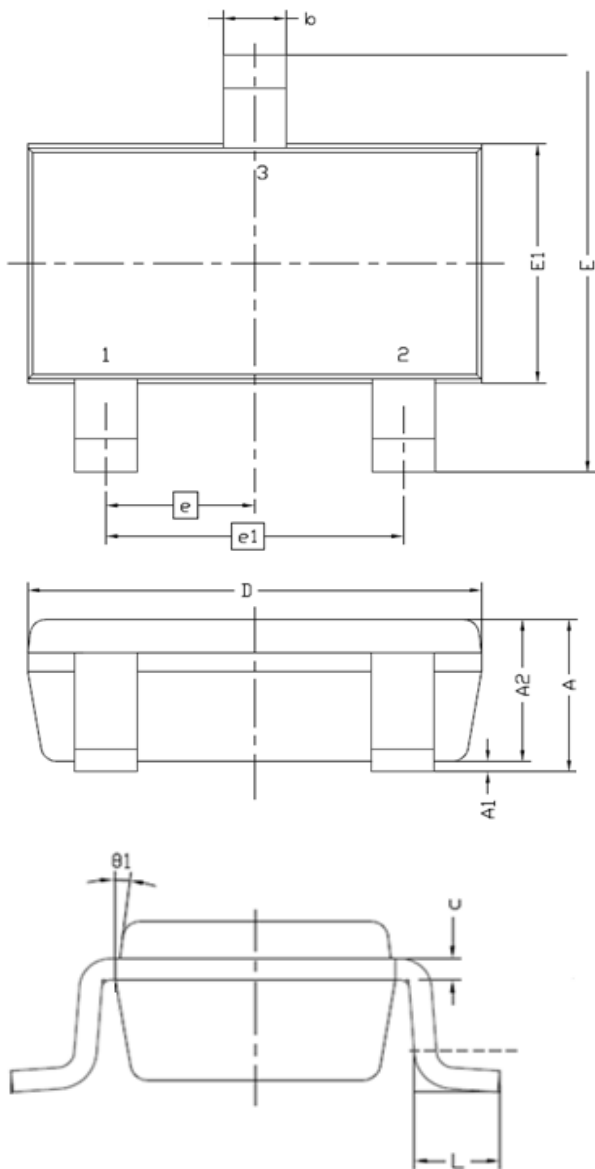
SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 uA	0.3			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = 8 V			10	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V			1	μA
		V _{DS} = 16 V, V _{GS} = 0 V, T _J = 55°C			10	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	7			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 1 A			0.076	Ω
		V _{GS} = 2.5 V, I _D = 1 A			0.103	
Forward Transconductance ^A	g _{fs}	V _{DS} = 5 V, I _D = 1 A		7		S
Diode Forward Voltage	V _{SD}	I _S = 1 A, V _{GS} = 0 V		0.7		V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 1 A		1.9		nC
Gate-Source Charge	Q _{gs}			0.4		
Gate-Drain Charge	Q _{gd}			0.6		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 6 Ω, R _G = 6 Ω, V _{GEN} = 4.5 V		7		ns
Rise Time	t _r			10		
Turn-Off Delay Time	t _{d(off)}			20		
Fall-Time	t _f			10		

Notes

- Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

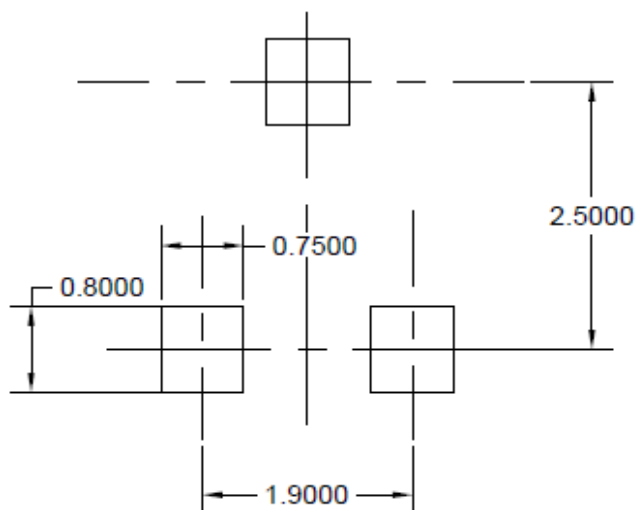
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Package Information



Symbol	MILLIMETERS	
	MIN	MAX
A	0.8	1.2
A1	0	0.1
A2	0.7	1.1
b	0.3	0.5
c	0.1	0.2
D	2.7	3.1
E	2.6	3
E1	1.4	1.8
e	0.95 BSC	
e1	1.9 BSC	
L	0.3	0.6
$\theta 1$	7° NOM	

Recommended Pad Layout



Note: Drain opening is recommended to be solder mask defined in a copper fill for improved thermal performance

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