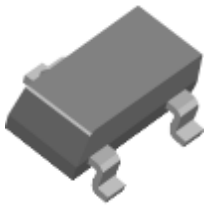
P-Channel 20-V (D-S) MOSFET

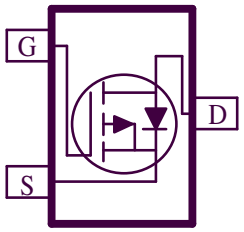
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (OHM)	I_D (A)
-20	0.100 @ V_{GS} = -4.5V	-2.9
	0.160 @ V_{GS} = -2.5V	-2.3
	0.290 @ V_{GS} = -1.8V	-1.7

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology

Pb-free
RoHS COMPLIANT
HALOGEN FREE





ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current[a]	T_A=25°C	I_D	-2.9	A
	T_A=70°C		-2.4	
Pulsed Drain Current[b]		I_{DM}	-10	
Continuous Source Current (Diode Conduction)[a]		I_S	±1.6	A
Power Dissipation[a]	T_A=25°C	P_D	1.25	W
	T_A=70°C		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient[a]	t <= 5 sec	R_{THJA}	100	°C/W
	Steady-State		166	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Limits**			**Unit**
			Min	**Typ**	**Max**	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 uA	-0.4			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +/-12 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16 V, V_{GS} = 0 V			-1	uA
		V_{DS} = -16 V, V_{GS} = 0 V, T_J = 55°C			-10	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = -5 V, V_{GS} = -4.5 V	-3			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = -4.5 V, I_D = -2.9 A			0.100	Ω
		V_{GS} = -2.5 V, I_D = -2.3 A			0.160	
		V_{GS} = -1.8 V, I_D = -1.7 A			0.290	
Forward Tranconductance[A]	g_{fs}	V_{DS} = -5 V, I_D = -2.8 A		3		S
Diode Forward Voltage	V_{SD}	I_S = -1.6 A, V_{GS} = 0 V		-0.7		V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = -5 V, V_{GS} = -4.5 V, I_D = -2.6 A		6		nC
Gate-Source Charge	Q_{gs}			0.3		
Gate-Drain Charge	Q_{gd}			1.3		
Input Capacitance	C_{iss}	P-Channel VDS=-15V, VGS=0V, f=1MHz		395		pF
Output Capacitance	C_{oss}			130		
Reverse Transfer Capacitance	C_{rss}			33		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -5 V, R_L = 5 OHM, V_{GEN} = -4.5 V, R_G = 6 OHM		6.5		ns
Rise Time	t_r			3		
Turn-Off Delay Time	$t_{d(off)}$			31		
Fall-Time	t_f			4		

Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Analog Power (APL) reserves the right to make changes without further notice to any products herein. APL makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does APL assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in APL data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. APL does not convey any license under its patent rights nor the rights of others. APL products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the APL product could create a situation where personal injury or death may occur. Should Buyer purchase or use APL products for any such unintended or unauthorized application, Buyer shall indemnify and hold APL and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that APL was negligent regarding the design or manufacture of the part. APL is an Equal Opportunity/Affirmative Action Employer.

Typical Electrical Characteristics

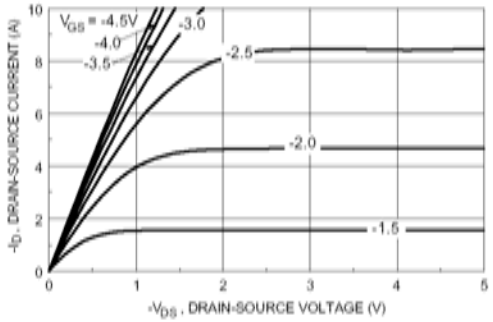


Figure 1. On-Region Characteristics.

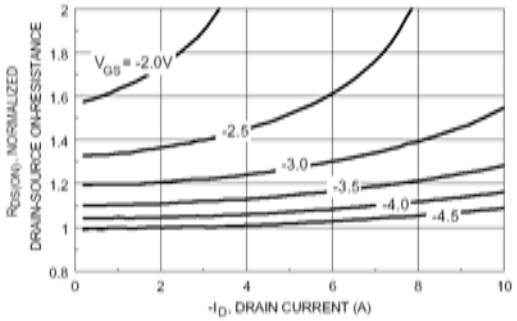


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

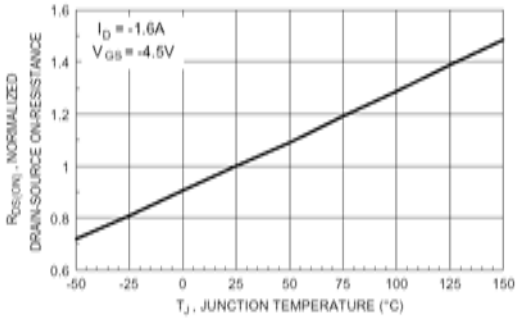


Figure 3. On-Resistance Variation with Temperature.

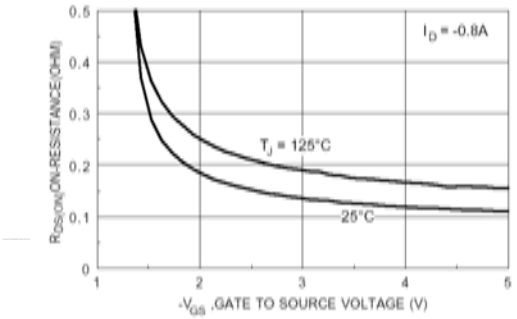


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

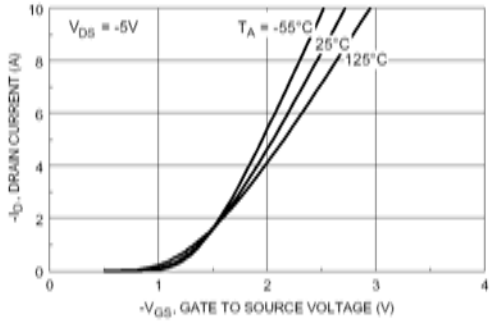


Figure 5. Transfer Characteristics.

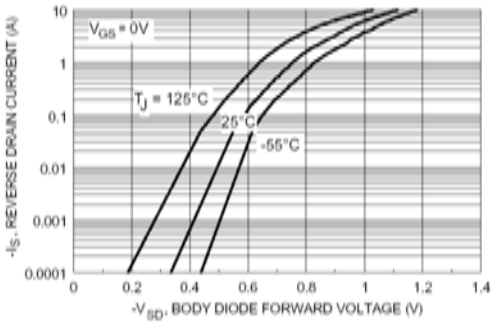


Figure 6 . Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics

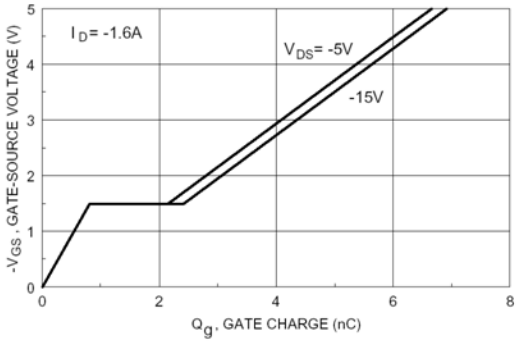


Figure 7. Gate Charge Characteristics.

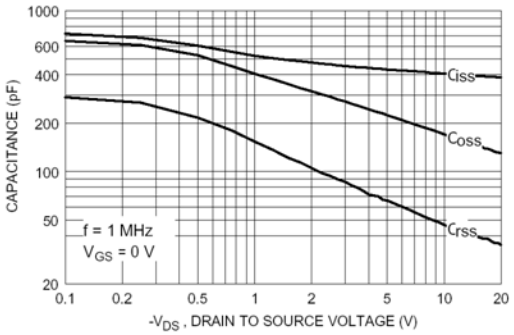


Figure 8. Capacitance Characteristics.

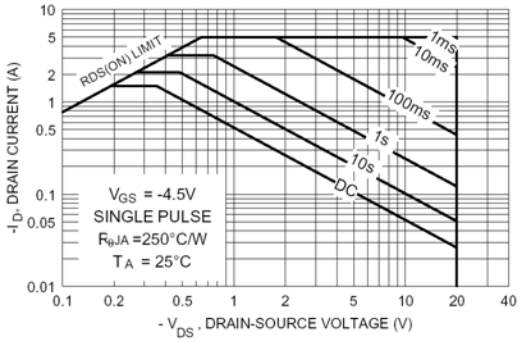


Figure 9. Maximum Safe Operating Area.

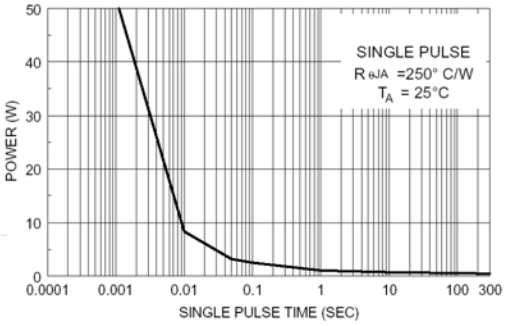


Figure 10. Single Pulse Maximum Power Dissipation.

Normalized Thermal Transient Junction to Ambient

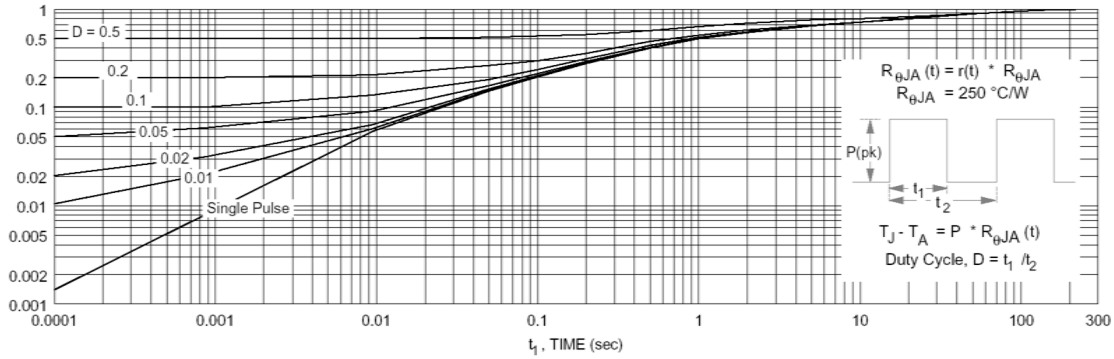
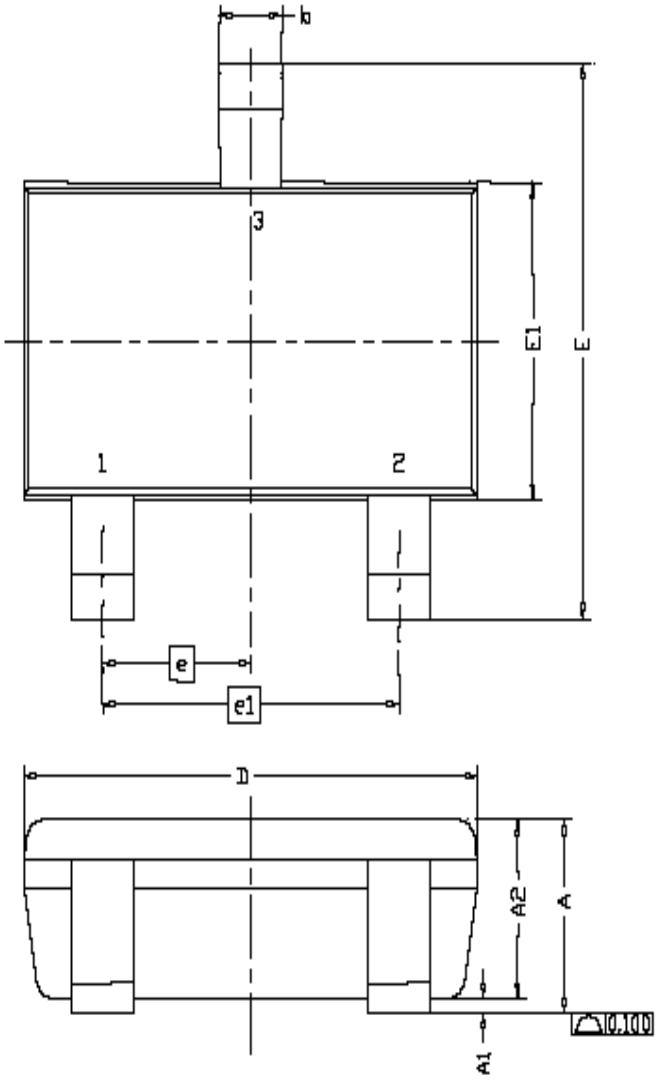


Figure 11. Transient Thermal Response Curve.

Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	0.95	1.10
A1	0.01	---	0.10
A2	0.85	0.90	0.925
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L1	0.60REF		
L2	0.25BSC		
R	0.10	---	---
θ	0°	4°	8°
θ1	7°NOM