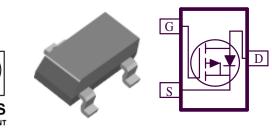
AM2317P

P - Channel Logic Level MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology
- RoHS COMPLIANT HALOGEN

PRODUCT SUMMARY				
V _{DS} (V)	$V_{DS}(V)$ $r_{DS(on)}(\Omega)$ $I_{D}(A)$			
-30	$0.30 @ V_{GS} = -10 V$	-1.0		
	$0.50 @ V_{GS} = -4.5V$	-0.9		



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V _{DS}	-30	v	
Gate-Source Voltage			±20	v	
Continuous Drain Current ^a	T _A =25°C	Т.,	±0.9		
Continuous Drain Current	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	цр	±0.75	А	
Pulsed Drain Current ^b		I _{DM}	±10		
Continuous Source Current (Diode Conduction) ^a			0.4	А	
	$T_A=25^{\circ}C$	PD	0.5	W	
Power Dissipation ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	r D	0.42	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum Units	
Maximum Junction-to-Ambient ^a	t <= 5 sec	р	250	⁰ C/111
	Steady-State	R_{THJA}	285	°C/W

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^{\circ}C$ UNLESS OTHERWISE NOTED)							
D (Limits				
Parame te r	Symbol	Test Conditions	Min	Тур	Max	Unit	
Switch Off Characteristics	-				_		
Drain-Source Breakdown Voltage	V(BR)DSS	$V_{GS} = 0 V, I_D = -250 uA$	-30				
Zana Cata Valtaga Durin Cumant	I	$V_{DS} = -24 V, V_{GS} = 0 V$			-1		
Zero Gate Voltage Drain Current	Idss	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^{\circ}\text{C}$			-10	μA	
Gate-Body Leakage	Igss	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			±100	nA	
Switch On Characteristics							
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \text{ uA}$	-0.80	-1.7	-2.6	V	
On-State Drain Current ^A	ID(on)	$V_{DS} = -5 V, V_{GS} = -4.5 V$	-2			Α	
		$V_{GS} = -10 \text{ V}, I_D = -1.0 \text{ A}$		0.25	0.30	<u> </u>	
Drain-Source On-Resistance ^A	rDS(on)	$V_{GS} = -4.5 \text{ V}, \text{ ID} = -0.9 \text{ A} \text{ T}_{J} = 55^{\circ} \text{C}$		0.53	0.66		
		$V_{GS} = -4.5 \text{ V}, I_D = -0.9 \text{ A}$		0.45	0.50		
Forward Tranconductance ^A	gfs	VDS = -5 V, ID = -1.1 A		2		S	
Diode Forward Voltage	V _{SD}	$I_{S} = -0.4 \text{ A}, V_{GS} = 0 \text{ V}$		-0.70	-1.2	V	
Dynamic ^b							
Total Gate Charge	Qg			2.0	3.0		
Gate-Source Charge	Qgs	$V_{DS} = -10 V, V_{GS} = -5 V,$		0.5		nC	
Gate-Drain Charge	Qgd	ID = -0.9 A		1.1			
Switching							
Turn-On Delay Time	t _{d(on)}			8	16		
Rise Time	tr	$V_{DS} = -10 \text{ V}, I_D = -0.9 \text{ A},$		16	32	ns	
Turn-Off Delay Time	td(off)	$R_G = 50 \Omega, V_{GEN} = -10 V$		36	93		
Fall-Time	tf			33	94		

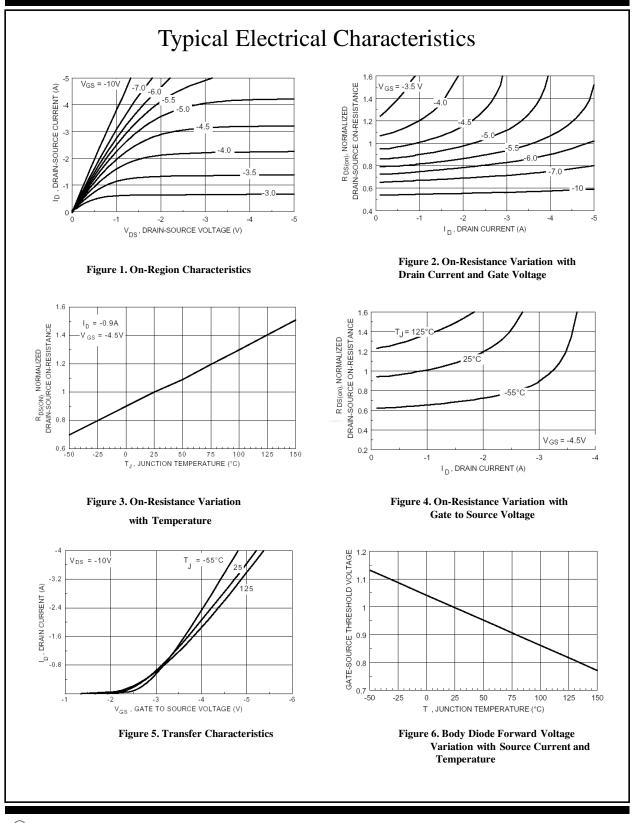
Notes

a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.

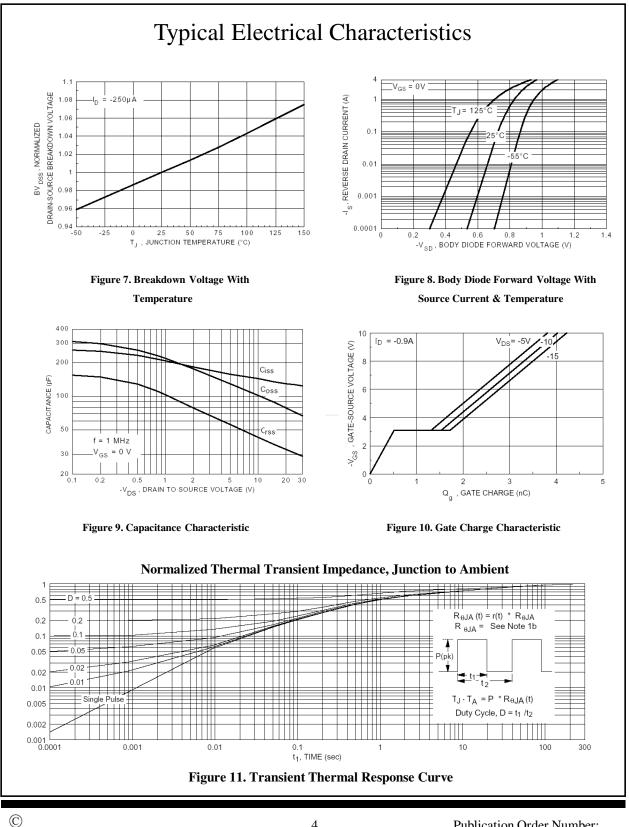
b. Guaranteed by design, not subject to production testing.

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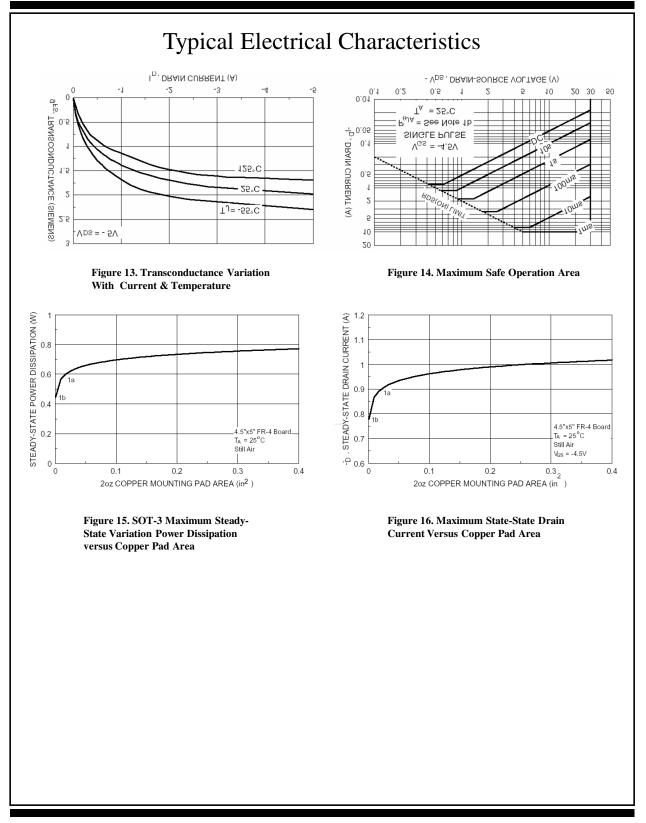


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Package Information

