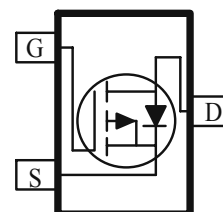
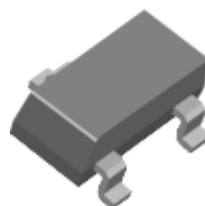


**P - Channel Logic Level MOSFET**

These miniature surface mount MOSFETs utilize High Cell Density process. Low  $r_{DS(on)}$  assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are voltage control small signal switch, power management in portable and battery-powered products such as computer portable electronics and other battery power application.

- Low  $r_{DS(on)}$  Provides Higher Efficiency and Extends Battery Life
- Fast Switch
- Low Gate Charge
- Miniature SOT-23 Surface Mount Package Saves Board Space

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
-30	0.20 @ $V_{GS} = -10$ V	-2.1
	0.30 @ $V_{GS} = -4.5$ V	-1.7



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		$V_{DS}$	-30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$T_A = 25$ °C	$I_D$	-2.1	A
	$T_A = 70$ °C		-1.7	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	$\pm 10$	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	-0.4	A
Power Dissipation <sup>a</sup>	$T_A = 25$ °C	$P_D$	1.25	W
	$T_A = 70$ °C		0.8	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 5$ sec	$R_{THJA}$	250	°C/W
	Steady-State		285	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
<b>Static</b>						
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			-10	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.30			V
On-State Drain Current <sup>A</sup>	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -4.5\text{ V}$	-3			A
Drain-Source On-Resistance <sup>A</sup>	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -2.1\text{ A}$			0.20	$\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -1.7\text{ A}$			0.30	
Forward Transconductance <sup>A</sup>	$g_{fs}$	$V_{DS} = -5\text{ V}, I_D = -2.1\text{ A}$		2		S
Diode Forward Voltage	$V_{SD}$	$I_S = -0.4\text{ A}, V_{GS} = 0\text{ V}$		-0.70	-1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -10\text{ V}, V_{GS} = -5\text{ V},$ $I_D = -2.1\text{ A}$		3.4		nC
Gate-Source Charge	$Q_{gs}$			0.8		
Gate-Drain Charge	$Q_{gd}$			1.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DS} = -10\text{ V}, I_D = -1.1\text{ A},$ $R_G = 50\text{ }\Omega, V_{GEN} = -10\text{ V}$		8		ns
Rise Time	$t_r$			18		
Turn-Off Delay Time	$t_{d(off)}$			52		
Fall-Time	$t_f$			39		

## Notes

- Pulse test:  $PW \leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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## Typical Electrical Characteristics

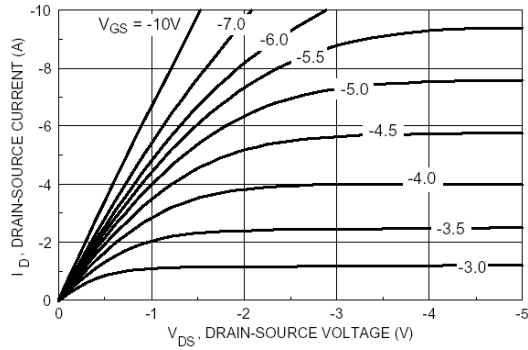


Figure 1. On-Region Characteristics

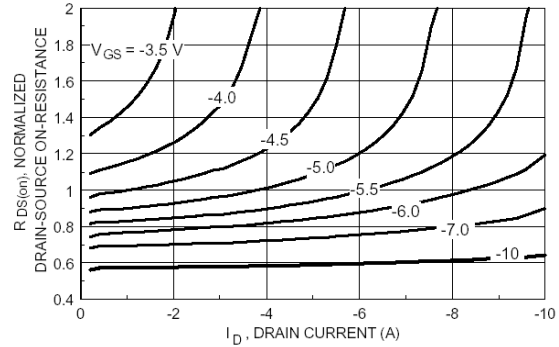


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

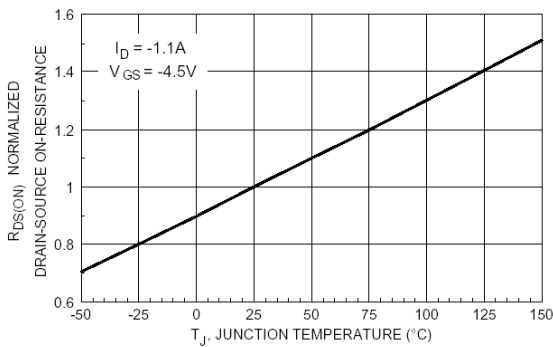


Figure 3. On-Resistance Variation with Temperature

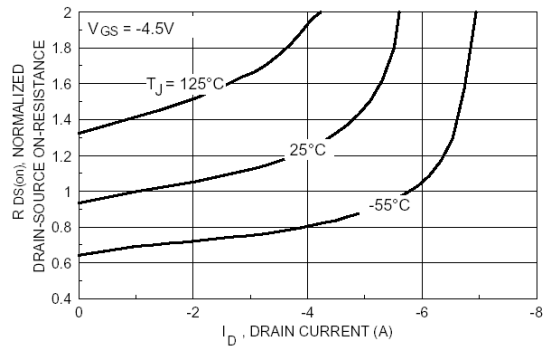


Figure 4. On-Resistance Variation with Gate to Source Voltage

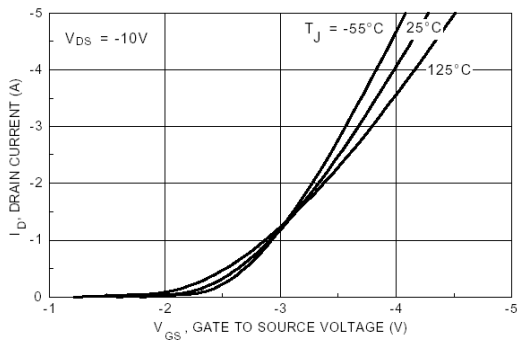


Figure 5. Transfer Characteristics

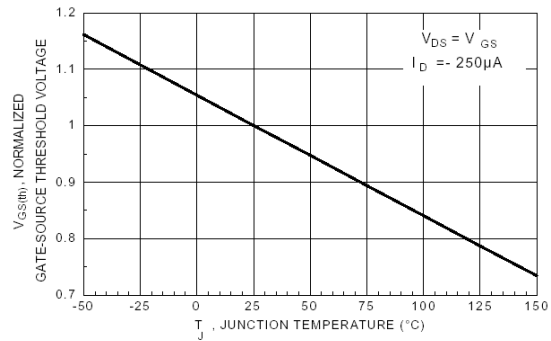


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

### Typical Electrical Characteristics

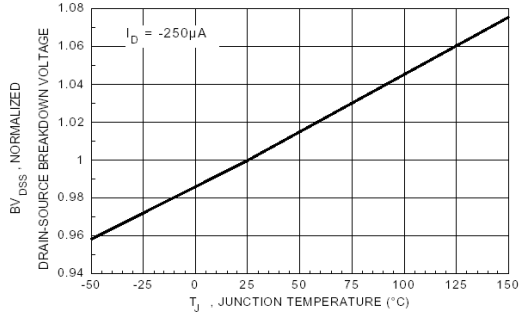


Figure 7. Breakdown Voltage Variation with Temperature.

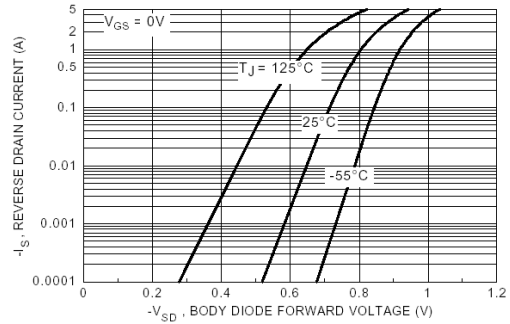


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.

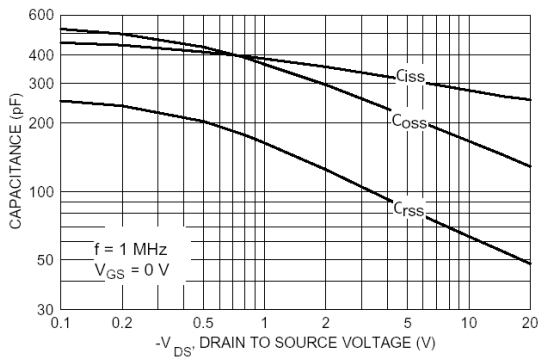


Figure 9. Capacitance Characteristic

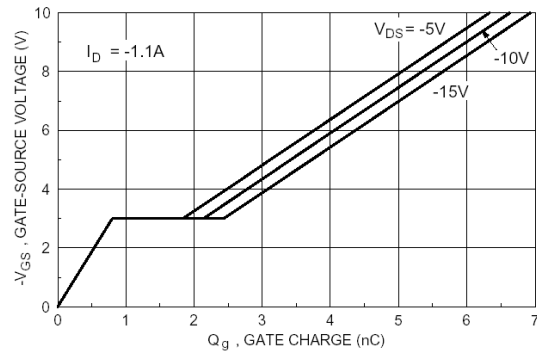


Figure 10. Gate Charge Characteristic

### Normalized Thermal Transient Impedance, Junction to Ambient

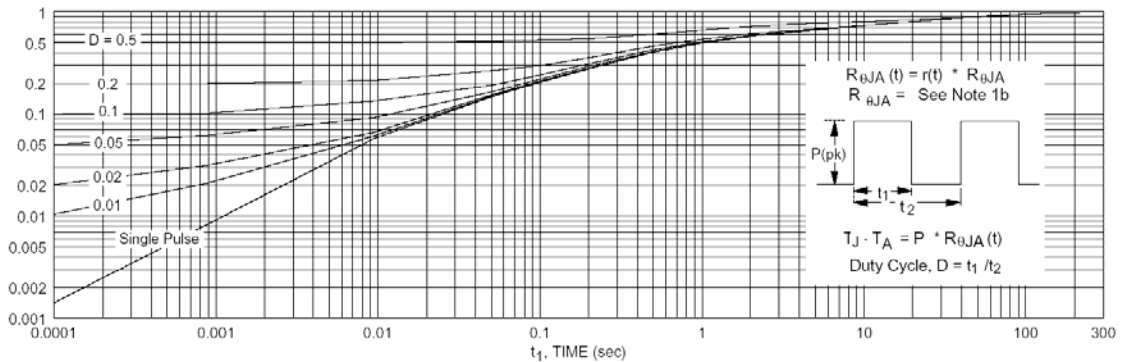


Figure 11. Transient Thermal Response Curve

### Typical Electrical Characteristics

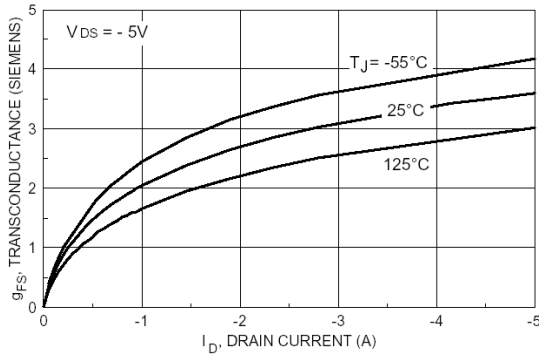


Figure 12. Transconductance Variation With Current & Temperature

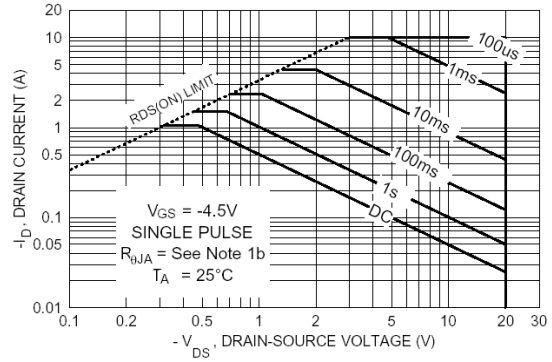


Figure 13. Maximum Safe Operation Area

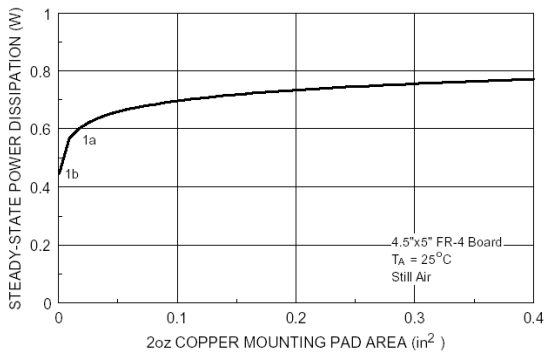


Figure 14. SOT-3 Maximum Steady-State Variation Power Dissipation versus Copper Pad Area

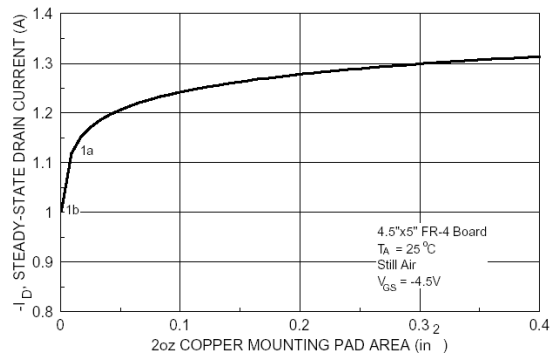
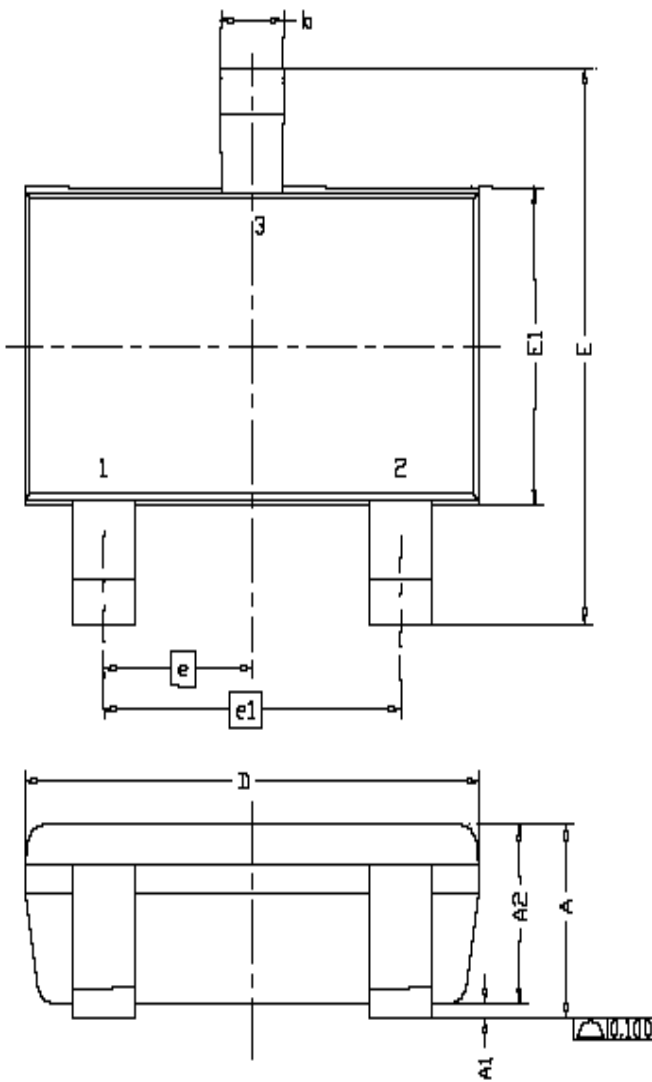


Figure 15. Maximum State-State Drain Current Versus Copper Pad Area

# Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	0.95	1.10
A1	0.01	---	0.10
A2	0.85	0.90	0.925
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L1	0.60REF		
L2	0.25BSC		
R	0.10	---	---
θ	0°	4°	8°
θ1	7°NOM		

