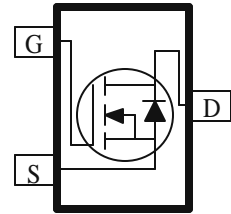
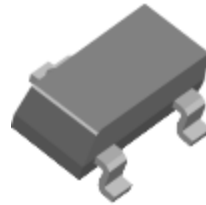


N-Channel 40-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$I_{DS(on)}$ m(O)	I_D (A)
40	86 @ $V_{GS}=10V$	5.2
	128 @ $V_{GS}=4.5V$	3.7

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_A=25^\circ\text{C}$	I_D	5.2	A
	$T_A=70^\circ\text{C}$		4.1	
Pulsed Drain Current ^b		I_{DM}	30	
Continuous Source Current (Diode Conduction) ^a		I_S	1.6	A
Power Dissipation ^a	$T_A=25^\circ\text{C}$	P_D	1.3	W
	$T_A=70^\circ\text{C}$		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 5\text{ sec}$	$R_{\theta JA}$	100	$^\circ\text{C/W}$
	Steady-State		166	$^\circ\text{C/W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

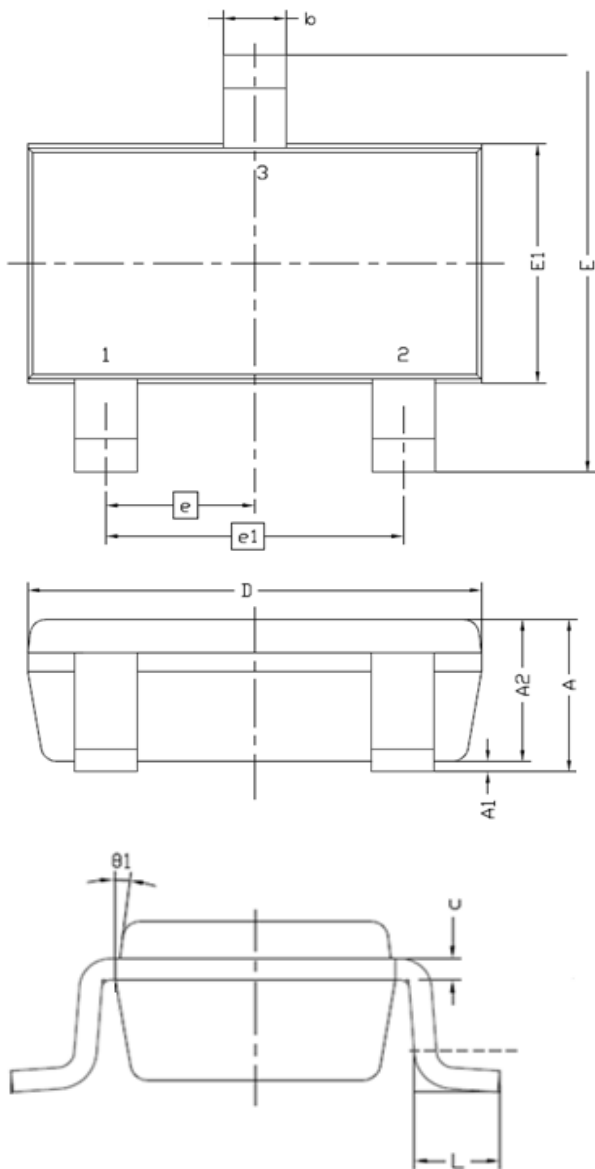
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 V, V_{GS} = 20 V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 32 V, V_{GS} = 0 V$			1	uA
		$V_{DS} = 32 V, V_{GS} = 0 V, T_J = 55^\circ C$			25	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 V, V_{GS} = 10 V$	20			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 10 V, I_D = 5.2 A$			86	m Ω
		$V_{GS} = 4.5 V, I_D = 3.7 A$			128	
Forward Transconductance ^A	g_{fs}	$V_{DS} = 15 V, I_D = 5.2 A$		40		S
Diode Forward Voltage	V_{SD}	$I_S = 2.3 A, V_{GS} = 0 V$		0.7		V
Dynami^b						
Total Gate Charge	Q_g	$V_{DS} = 15 V, V_{GS} = 4.5 V,$ $I_D = 5.2 A$		4.0		nC
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			1.4		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25 V, R_L = 25 \Omega, I_D = 1 A,$ $V_{GEN} = 10 V$		16		nS
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(off)}$			23		
Fall-Time	t_f			3		

Notes

- Pulse test: $PW \leq 300 \mu s$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

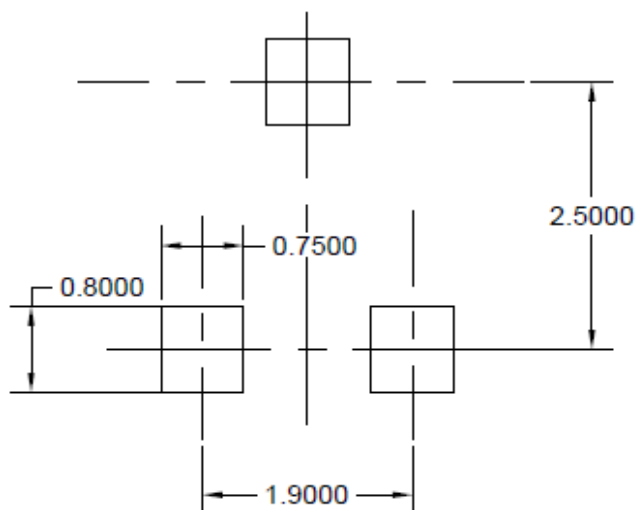
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Package Information



Symbol	MILLIMETERS	
	MIN	MAX
A	0.8	1.2
A1	0	0.1
A2	0.7	1.1
b	0.3	0.5
c	0.1	0.2
D	2.7	3.1
E	2.6	3
E1	1.4	1.8
e	0.95 BSC	
e1	1.9 BSC	
L	0.3	0.6
$\theta1$	7° NOM	

Recommended Pad Layout



Note: Drain opening is recommended to be solder mask defined in a copper fill for improved thermal performance

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