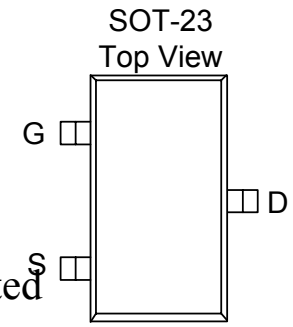
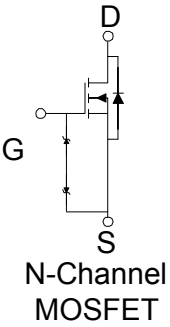
N-Channel 60V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.092 @ V_{GS} = 10 V	3.1
	0.107 @ V_{GS} = 4.5V	2.9

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology





ESD Protected
2000V

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[a]	T_A=25°C	I_D	2.8	A
	T_A=70°C		1.8	
Pulsed Drain Current[b]		I_{DM}	±15	
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	A
Power Dissipation[a]	T_A=25°C	P_D	1.3	W
	T_A=70°C		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Ambient[a]	t <= 5 sec	R_{THJA}	100	°C/W
	Steady-State		166	

Notes

a. Surface Mounted on 1” x 1” FR4 Board.

b. Pulse width limited by maximum junction temperature

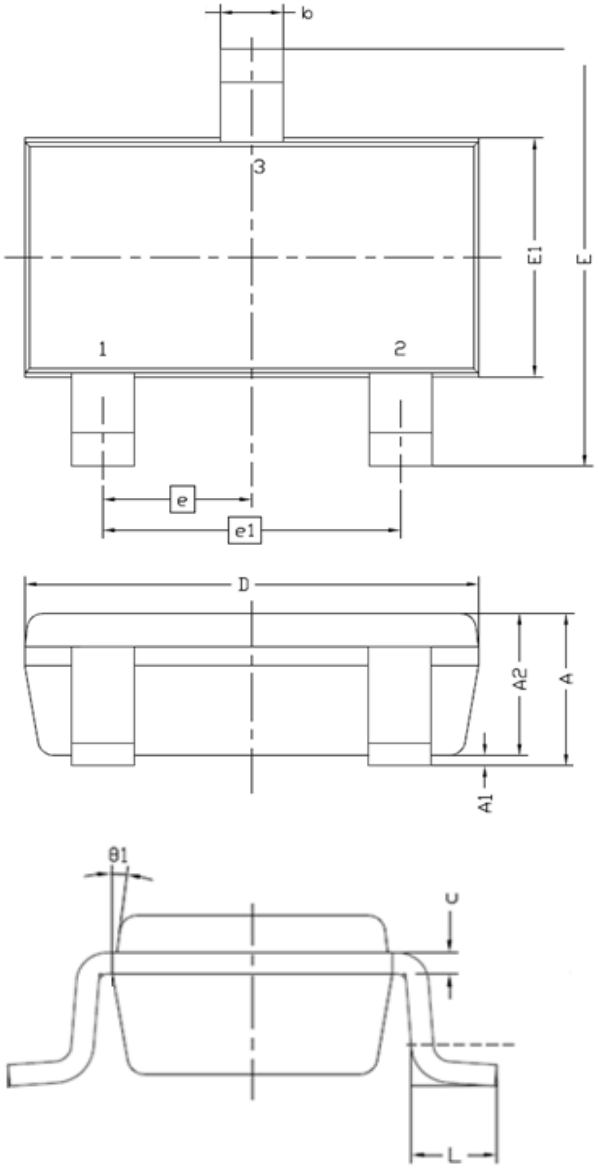
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Limits**			**Unit**
			Min	**Typ**	**Max**	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 uA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	uA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 55°C			50	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	10			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 3.1 A			92	mΩ
		V_{GS} = 4.5 V, I_D = 2.9 A			107	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 4.5 V, I_D = 3.1 A		8		S
Diode Forward Voltage	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V		1.10		V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 5 V, I_D = 3.1 A		3.6		nC
Gate-Source Charge	Q_{gs}			1.8		
Gate-Drain Charge	Q_{gd}			1.3		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 30 Ω, I_D = 1 A, V_{GEN} = 10 V		10		ns
Rise Time	t_r			10		
Turn-Off Delay Time	$t_{d(off)}$			20		
Fall-Time	t_f			10		

Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

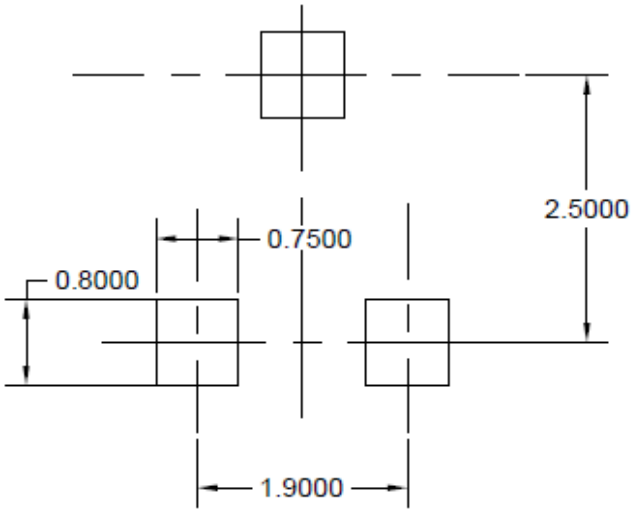
b. Guaranteed by design, not subject to production testing.

Package Information



Symbol	MILLIMETERS	
	MIN	MAX
A	0.8	1.2
A1	0	0.1
A2	0.7	1.1
b	0.3	0.5
c	0.1	0.2
D	2.7	3.1
E	2.6	3
E1	1.4	1.8
e	0.95 BSC	
e1	1.9 BSC	
L	0.3	0.6
θ1	7° NOM	

Recommended Pad Layout



Note: Drain opening is recommended to be solder mask defined in a copper fill for improved thermal performance