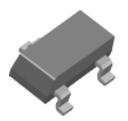
P-Channel 80-V (D-S) MOSFET

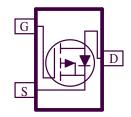
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY				
$V_{DS}(V)$	$\mathbf{r}_{\mathrm{DS(on)}}\left(\Omega\right)$ $\mathbf{I}_{\mathrm{D}}\left(\mathbf{A}\right)$			
-80	$0.5 @ V_{GS} = -10V$	1.4		
	$0.6 @ V_{GS} = -4.5V$	1.3		

- $\hbox{ Low $r_{DS(on)}$ provides higher efficiency and} \\ \hbox{ extends battery life}$
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology







ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)						
Parameter		Symbol	Maximum	Units		
Drain-Source Voltage			-80	V		
Gate-Source Voltage			±20	v		
	$T_A=25^{\circ}C$	 _{T_}	0.9			
Continuous Drain Current ^a	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	ъ	0.7	A		
Pulsed Drain Current ^b	I_{DM}	±1.6				
Continuous Source Current (Diode Conduction) ^a		I_S	-1	A		
D D:	$T_A=25^{\circ}C$	D_	1.3	w		
Power Dissipation ^a	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	Гр	0.8	**		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Maximum	Units			
	t <= 5 sec	D	100	°C/W		
Maximum Junction-to-Ambient ^a	Steady-State	R_{THJA}	166			

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

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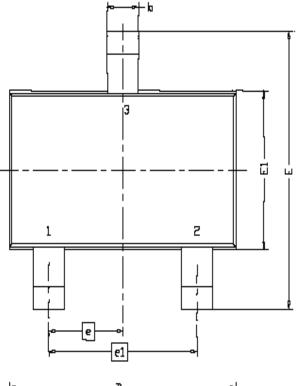
SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Domario 4 a m	Comple of	T C. 199	Limits			T I 94
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_{D} = -250 \text{ uA}$	-1.2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA
Zana Cata Valta da Duain Cumunt	T	$V_{DS} = -64 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -64 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			-10	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-1			A
A		$V_{GS} = -10 \text{ V}, I_{D} = -0.5 \text{ A}$			0.5	Ω
Drain-Source On-Resistance ^A	fDS(on)	$V_{GS} = -4.5 \text{ V}, I_D = -0.5 \text{ A}$			0.6	
Forward Tranconductance ^A	g_{fs}	$V_{DS} = -15 \text{ V}, I_D = -0.5 \text{ A}$		2.2		S
Diode Forward Voltage	V _{SD}	$I_S = -1 \text{ A}, V_{GS} = 0 \text{ V}$		0.8		V
Dynamic ^b						
Total Gate Charge	Qg			7		
Gate-Source Charge	Q_{gs}	$V_{DS} = -30 \ \underline{V}, V_{GS} = -10 \ V, I_{D} = -1.6 \ A$		1		nC
Gate-Drain Charge	Qgd			2		
Turn-On Delay Time	t _{d(on)}			7		
Rise Time	t _r	$V_{DD} = -30 \text{ V}, R_L = 30 \Omega, ID = -1 \text{ A},$		11		6
Turn-Off Delay Time	t _{d(off)}	$VGEN = -10 \text{ V}, RG = 6\Omega$		17		nS
Fall-Time	t_{f}			11		Ī

Notes

- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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Package Information



DIM,	MILLIMETERS			
	MIN	NDM	MAX	
Α	0.935	0.95	1.10	
A1	0.01		0.10	
A2	0.85	0.90	0.925	
Ь	0.30	0.40	0.50	
С	0.10	0.15	0.25	
D	2.70	2.90	3.10	
Ε	2.60	2.80	3.00	
E1	1.40	1.60	1.80	
6	0.95 BSC			
el	1.90 BSC			
L	0.30	0.40	0.60	
L1	0.60REF			
L2	0.25BSC			
R	0.10			
θ	Q+	4*	8,	
81	7*N□M			

