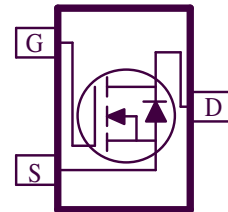
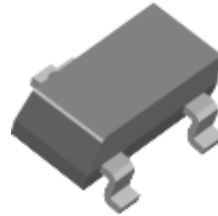


N-Channel 150V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
150	2.6 @ $V_{GS} = 10$ V	0.6
	2.8 @ $V_{GS} = 5.5$ V	0.5

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	0.6	A
Pulsed Drain Current ^b		I_{DM}	± 10	
Continuous Source Current (Diode Conduction) ^a		I_S	1.1	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	1.30	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typ	Max	
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	93	110	$^\circ\text{C/W}$
	Steady State		130	150	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

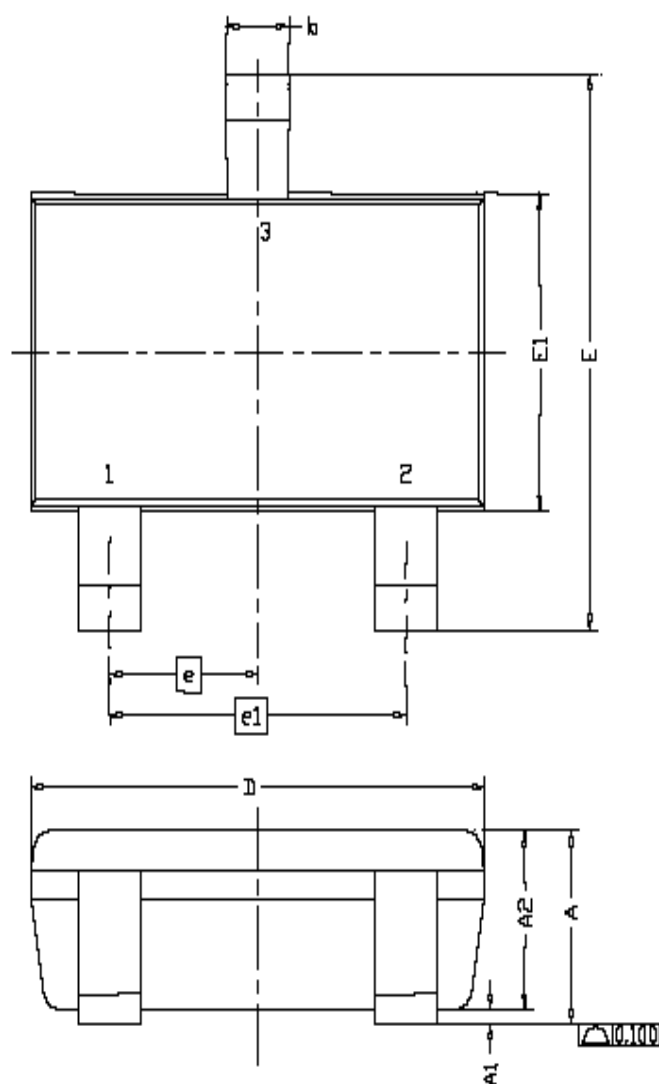
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 8\text{ V}$			± 25	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 120\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 120\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55^{\circ}\text{C}$			10	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5\text{ V}$, $V_{GS} = 10\text{ V}$	10			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 0.5\text{ A}$			2.6	Ω
		$V_{GS} = 5.5\text{ V}$, $I_D = 0.5\text{ A}$			2.8	
Forward Tranconductance ^A	g_{fs}	$V_{DS} = 10\text{ V}$, $I_D = 0.5\text{ A}$		11.3		S
Diode Forward Voltage	V_{SD}	$I_S = 0.5\text{ A}$, $V_{GS} = 0\text{ V}$		0.75		V
Dynamic ^b						
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}$, $V_{GS} = 5.5\text{ V}$, $I_D = 0.5\text{ A}$		7		nC
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}$, $R_L = 15\text{ }\Omega$, $I_D = 1\text{ A}$, $V_{GEN} = 4.5\text{ V}$		8		ns
Rise Time	t_r			24		
Turn-Off Delay Time	$t_{d(off)}$			35		
Fall-Time	t_f			10		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	0.95	1.10
A1	0.01	---	0.10
A2	0.85	0.90	0.925
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L1	0.60 REF		
L2	0.25 BSC		
R	0.10	---	---
θ	0°	4°	8°
θ1	7° NOM		

