Am2914

Vectored Priority Interrupt Controller

add xc pkg

DISTINCTIVE CHARACTERISTICS

- Accepts 8 interrupt inputs –
  Interrupts may be pulses or levels and are stored internally
- Built-in mask register –
  Six different operations can be performed on mask register
- Built-in status register –
  Status register holds code for lowest allowed interrupt
- Vectored output –
  Output is binary code for highest priority unmasked interrupt
- Expandable –
  Any number of Am2914's may be stacked for large interrupt systems
- Microprogrammable –
  Executes 16 different microinstructions
  Instruction enable pin aids in vertical microprogramming

GENERAL DESCRIPTION

The Am2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The high-speed of the Am2914 makes it ideal for use in Am2900 family microcomputer designs, but it can also be used with the Am9080A MOS microprocessor.

The Am2914 receives interrupt requests on 8 interrupt input lines ($\overline{P}_0$-$\overline{P}_7$). A LOW level is a request. An internal latch may be used to catch pulses on these lines, or the latch may be bypassed so the request lines drive the level-triggered interrupt register directly. An 8-bit mask register is used to mask individual interrupts. Considerable flexibility is provided for controlling the mask register. Requests in the interrupt register are ANDed with the corresponding bits in the mask register and the results are sent to an 8-input priority encoder, which produces a three-bit encoded vector representing the highest numbered input which is not masked.

An internal status register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the status register are compared with the output of the priority encoder, and an interrupt request output will occur if the vector is greater than or equal to status. Whenever a vector is read from the Am2914 the status register is automatically updated to point to one level higher than the vector read. (The status register can be loaded externally or read out at any time using the S pins.) Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A status overflow output indicates that an interrupt has been read at the highest priority.

The Am2914 is controlled by a 4-bit instruction field I_0-I_3. The command on the instruction lines is executed if $\overline{IE}$ is LOW and is ignored if $\overline{IE}$ is HIGH, allowing the 4 I bits to be shared with other devices.

RELATED PRODUCTS

Part No.	Description
Am2902A	Carry Look-ahead Generator
Am2913	Priority Interrupt Expander
Am25LS138	3-to-8 Decoder
Am27S19	Mapping PROM

3 Orig

004778

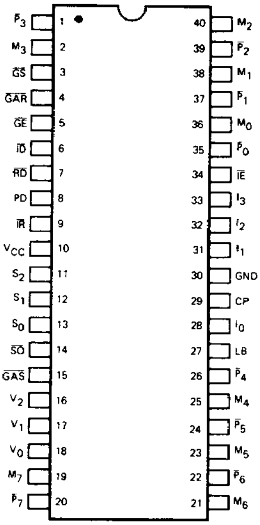
4778

AMD

Publication # 03576 Rev. E Amendment /0
Issue Date: January 1987

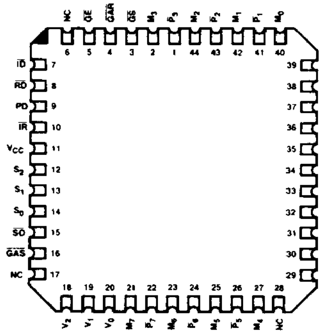
CONNECTION DIAGRAMS
Top View

Ceramic Dip



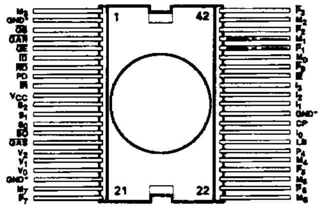
CD004212

Leadless Chip Carrier



CD004221

Flatpack

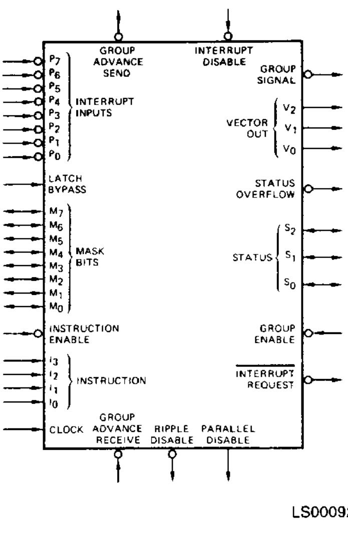


CD008031

*Note: GNDs and pins 2, 19 & 31 must all be tied together externally.

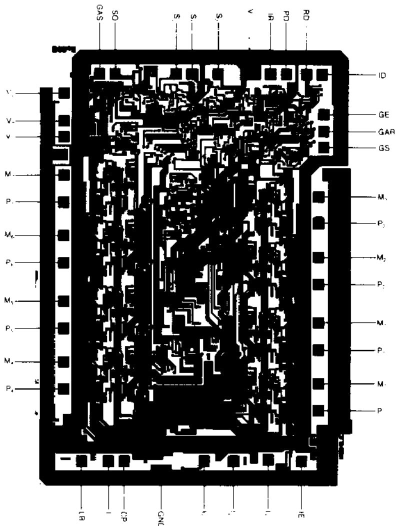
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS000921

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.133" x 0.187"

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

Am2914 D C B

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

C. PACKAGE TYPE
D = 40-Pin Ceramic DIP (CD 040)
L = 44-Pin Ceramic Leadless Chip Carrier (CL 044)
X = Dice

B. SPEED OPTION
Not Applicable

A. DEVICE NUMBER/DESCRIPTION
Am2914
Interrupt Controller

Valid Combinations	
Am2914	DC, DCB, LC, XC

add

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont.)
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-M-38510 and MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-M-38510 and MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish

Am2914 / B Q A

E. LEAD FINISH
A = Hot Solder DIP
C = Gold

D. PACKAGE TYPE
Q = 40-Pin Ceramic DIP (CD 040)
Y = 42-Pin Ceramic Topbrazed Flatpack (CFT042)

C. DEVICE CLASS
B = Class B

B. SPEED OPTION
Not Applicable

A. DEVICE NUMBER/DESCRIPTION
Am2914
Interrupt Controller

Valid Combinations	
APL	
Am2914	/BQA /BYC
CPL	
Am2914	/LMC

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A Tests consist of subgroups: 1, 2, 3, 7, 8, 9, 10, 11

CPL PRODUCTS

The order number (Valid Combination) for CPL products is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. CPL Status

Am2914 / L M C

E. CPL STATUS
C = CPL Certified

D. TEMPERATURE RANGE
M = Military (–55 to +125°C)

C. PACKAGE TYPE
L = 44-Pin Ceramic Leadless Chip Carrier (CL 044)

B. SPEED OPTION
Not Applicable

A. DEVICE NUMBER/DESCRIPTION
Am2914
Interrupt Controller

PIN DESCRIPTION

$\overline{P}_{7\text{-}0}$ Interrupt Request (Inputs)
Active LOW level or latched pulses.

LB Latch Bypass (Input)
When HIGH, the interrupt latches are transparent. When LOW, the latches are negative pulse catchers.

$M_{7\text{-}0}$ Mask Bus (Input/Ouput)
Bidirectional bus to load or read interrupt mask.

$I_{3\text{-}0}$ Microinstruction Inputs (Input)

$\overline{IE}$ $\overline{\text{Instruction Enable}}$ (Input)
The microinstruction is executed if $\overline{IE}$ is LOW and is ignored if $\overline{IE}$ is HIGH.

$\overline{GAR}$ $\overline{\text{Group Advance Receive}}$ (Input)
During a Master Clear or Read Vector microinstruction, this input signal is used to load the Lowest Group Enable flipflop. $\overline{GAR}$ of the lowest priority group must be LOW.

$\overline{GAS}$ $\overline{\text{Group Advance Send}}$ (Output)
During a Read Vector microinstruction, this output signal is LOW when the highest priority vector of the group is being read. $\overline{GAS}$ should be connected to $\overline{GAR}$ of the next higher group in a cascaded system.

$\overline{RD}$ $\overline{\text{Ripple Disable}}$ (Output)
This output is LOW when $\overline{\text{Interrupt Disable}}$ ($\overline{ID}$) is LOW, or the Lowest Group Enabled is LOW, or an $\overline{\text{Interrupt Request}}$ ($\overline{IR}$) is generated in the group. This output is connected to the $\overline{\text{Interrupt Disable}}$ ($\overline{ID}$) input of the next lower group.

PD Parallel Disable (Output)
This output is HIGH when the Lowest Group Enabled flipflop is LOW or an interrupt is generated in the group.

$\overline{GS}$ $\overline{\text{Group Signal}}$ (Output)
The output of the Lowest Group Enabled flipflop.

$\overline{GE}$ $\overline{\text{Group Enable}}$ (Input)
Input to the Lowest Group Enabled flipflop.

$\overline{SO}$ $\overline{\text{Status Overflow}}$ (Output)
This output signal is LOW after the highest priority vector of the group has been read. It stays LOW until a Master Clear or Load Status microinstruction is executed. $\overline{SO}$ of the highest priority group should be connected to the $\overline{\text{Interrupt Disable}}$ ($\overline{ID}$) of the same group. $\overline{SO}$ signals of lower priority groups are unused.

$S_{2\text{-}0}$ Status Bus (Input/Output)
Bidirectional bus to load or read the status register.

$\overline{ID}$ $\overline{\text{Interrupt Disable}}$ (Input)
When LOW, this input inhibits the $\overline{\text{Interrupt Request}}$ ($\overline{IR}$) output and generates a $\overline{\text{Ripple Disable}}$ ($\overline{RD}$) output.

$\overline{IR}$ $\overline{\text{Interrupt Request}}$ (Output)
Open collector output which is active LOW.

V_{2-0} Vector Output (Output)

CP Clock Input (Input)

FUNCTIONAL DESCRIPTION

The Microinstruction Decode circuitry decodes the Interrupt Microinstructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the Clock (CP) signal.

The Interrupt latches are set/reset-type latches. When the Latch Bypass (LB) signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass (LB) signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt ($\overline{P}_{0-7}$) Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded Interrupt Vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector is used for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S Bus. During a Vector Read, the Incrementer increments the Interrupt Vector by one, and the result is clocked into the Status Register. Thus the Status Register always points to the lowest level at which an interrupt will be accepted.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of Am2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the hinher order status bits.

The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request ($\overline{IR}$), Parallel Disable (PD), Ripple Disable ($\overline{RD}$), and Group Advance Send ($\overline{GAS}$) signals.

The Status Overflow ($\overline{SO}$) signal is used to disable all interrupts. It indicates the highest priority Interrupt Vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this group. When it is set, it enables the Clear Control Logic.

The clock (CP) signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

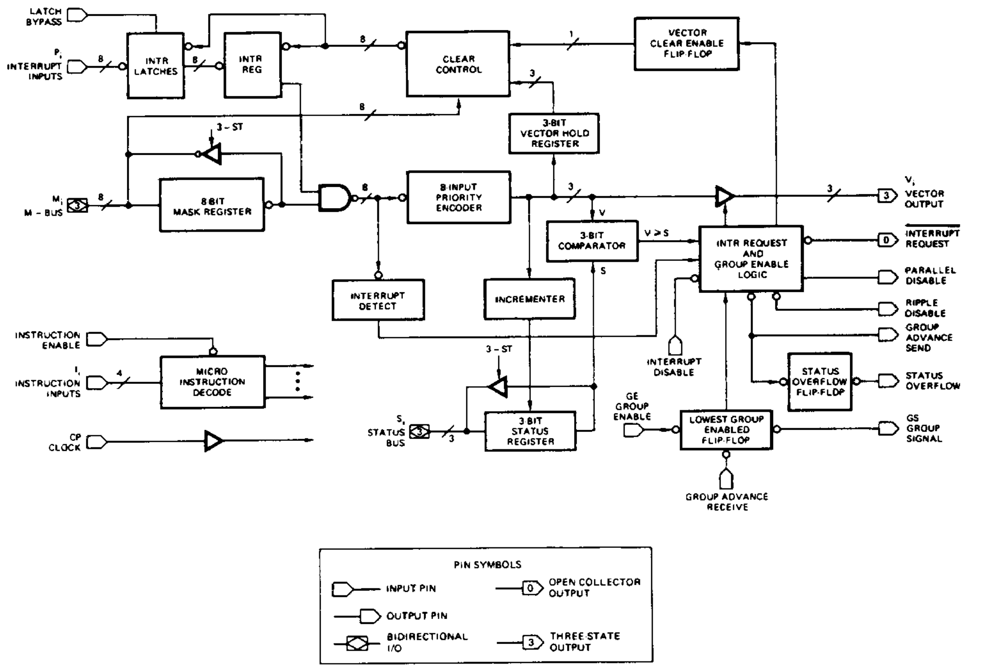


Figure 1. Detailed Block Diagram

BD001880

TABLE 1.
MICROINSTRUCTION SET FOR Am2914 PRIORITY INTERRUPT CIRCUIT

$I_3I_2I_1I_0$	Mnemonic	Instruction
		Mask Register Functions
1110	LDM	Load mask register from M bus
0111	RDM	Read mask register to M bus
1100	CLRM	Clear mask register (enables all priorities)
1000	SETM	Set mask register (inhibits all interrupts)
1010	BCLRM	Bit clear mask register from M bus *Note 1
1011	BSETM	Bit set mask register from M bus *Note 1
		Status Register Functions
1001	LDSTA	Load status register from S bus and LGE flip-flop from GE input
0110	RDSTA	Read status register to S bus
		Interrupt Request Control
1111	ENIN	Enable interrupt request
1101	DISIN	Disable interrupt request
		Vectored Output
0101	RDVC	Read vector output to V outputs, load V + 1 into status register, load V into vector hold register and set vector clear enable flip-flop.
		Priority Interrupt Register Clear
0001	CLRIN	Clear all interrupts
0011	CLRMR	Clear interrupts from mask register data (uses the M bus)
0010	CLRMB	Clear interrupts from M bus data *Note 1
0100	CLRVC	Clear the individual interrupt associated with the last vector read
		Master Clear
0000	MCLR	Clear all interrupts, clear mask register, clear status register, clear LGE flip-flop, enable interrupt request.

Note 1: SET/CLEAR those bits which have corresponding M-Bus bits equal to one.

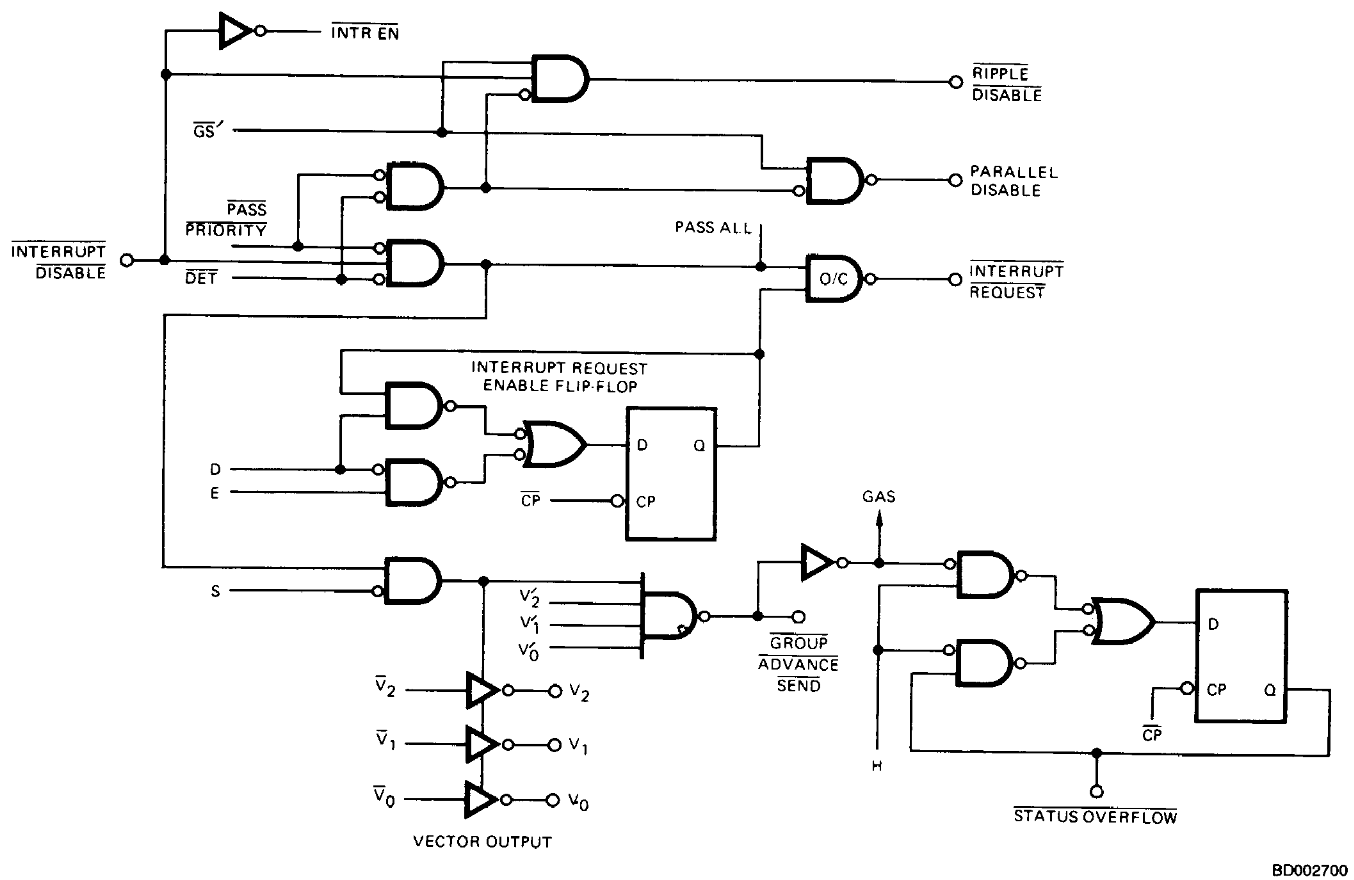


Figure 2. Interrupt Request Logic

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
(Ambient) Temperature Under Bias .... −55 to +110°C
Supply Voltage to Ground Potential
  Continuous .... −0.5 V to +7.0 V
DC Voltage Applied to Outputs For
  High Output State .... −0.5 V to $+V_{CC}$ Max.
DC Input Voltage .... −0.5 V to +5.5 V
DC Output Current, Into Outputs .... 30 mA
DC Input Current .... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
  Temperature T_A .... 0 to +70°C
  Supply Voltage .... +4.75 V to +5.25 V

Military (M) Devices
  Temperature T_C .... −55 to +125°C
  Supply Voltage .... +4.5 V to +5.5 V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified; Included in Group A, Subgroup 1, 2, 3 Tests unless otherwise noted

Parameters	Description	Test Conditions (Note 1)			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	MIL, I_{OH} = −1.0 mA		2.4		Volts
			COM'L, I_{OH} = −2.6 mA		2.4		
I_{CEX}	Output Leakage Current for IR Output	V_{CC} = Min., V_O = 5.5 V				250	μA
V_{OL}	Output LOW Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 4.0 mA			0.4	Volts
			I_{OL} = 8.0 mA			0.45	
			I_{OL} = 12.0 mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0		Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V	M_{0-7}			−0.15	mA
			S_{0-2}			−0.1	
			L. B.			−0.4	
			$\overline{\text{I. D.}}$			−2.0	
			$\overline{\text{IE}}$			−1.2	
			All Others			−0.8	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V	M_{0-7}			150	μA
			S_{0-2}			100	
			$\overline{\text{GE}}$, $\overline{\text{GAR}}$			40	
			$\overline{\text{IE}}$			60	
			$\overline{\text{I. D.}}$			60	
			All Others			20	
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V				1.0	mA
I_{OZL}	Off-State Output Current	V_{CC} = Max.	V_{OUT} = 0.5 V	M_{0-7}		−150	μA
				S_{0-2}		−100	
				V_{0-2}		−50	
I_{OZH}			V_{OUT} = 2.4 V	M_{0-7}		150	
				S_{0-2}		100	
				V_{0-2}		50	
I_{CC}	Power Supply Current	V_{CC} = Max.	COM'L	0 to +70°C		305	mA
				70°C		285	
			MIL	−55 to +125°C		310	
				125°C		260	
I_{SC}	Output Short Circuit Current (Note 2)	V_{CC} = Max. + V_{OUT}, V_{OUT} = 0.5 V			−30	−85	mA

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Operating Ranges for the applicable device type.
2. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating voltage and temperature range; included in Group A, Subgroups 9, 10, 11 Tests unless otherwise noted

C_L = 50pF. Measurements made at 1.5V.

TABLE I. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	COMMERCIAL	MILITARY
Minimum Clock LOW Time	30	30
Minimum Clock HIGH Time	30	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	40	40
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	8	8
Minimum Clock Period, $\overline{IE}$ = H on current cycle and previous cycle	50	55
Minimum Clock Period, $\overline{IE}$ = L on current cycle or previous cycle	100	110

TABLE II. MAXIMUM COMBINATIONAL PROPAGATION DELAYS (ns)

	To Output											
	COMMERCIAL						MILITARY					
From Input	M Bus	S Bus	V_{012}	$\overline{IR}$	$\overline{RD}$	$\overline{GAS}$	M Bus	S Bus	V_{012}	$\overline{IR}$	$\overline{RD}$	$\overline{GAS}$
$\overline{IE}$	52*	60*	65*	–	–	56	60*	68*	70*	–	–	62
I_{0123}	52*	60*	65*	–	–	56	60*	68*	70*	–	–	62
Irpt. Disable	–	–	45*	52	20	30	–	–	48*	60	22	33

*Enable/Disable. Disable: C_L = 5 pF, 0.5 V Change on outputs.

TABLE III. MAXIMUM DELAYS FROM CLOCK TO OUTPUTS (ns)

	COMMERCIAL							MILITARY						
Clock Path	To V_{012}	To $\overline{IR}$	To PD	To $\overline{RD}$	To $\overline{GAS}$	To $\overline{SO}$	To $\overline{GS}$	To V_{012}	To $\overline{IR}$	To PD	To $\overline{RD}$	To $\overline{GAS}$	To $\overline{SO}$	To $\overline{GS}$
Irpt Latches and Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Mask Register	–	97	67	67	–	–	–	–	105	75	75	–	–	–
Status Register	67	88	63	63	–	–	–	73	96	66	66	–	–	–
Lowest Group Enabled Flip–Flop	–	–	48	52	–	–	38	–	–	54	58	–	–	45
Irpt Request Enable Flip–Flop	–	62	–	–	–	–	–	–	66	–	–	–	–	–
Status Overflow Flip–Flop	–	–	–	–	–	35	–	–	–	–	–	–	40	–

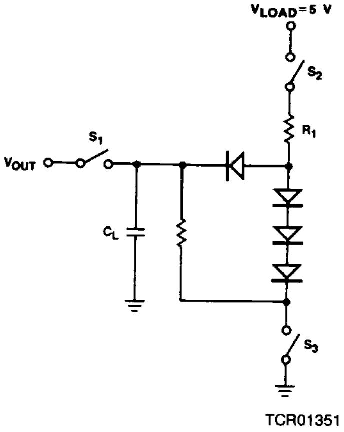
TABLE IV. SETUP AND HOLD TIME REQUIREMENTS (ns)
(All relative to clock LOW-to-HIGH transition)

	COMMERCIAL		MILITARY	
From Input	Set-Up Time	Hold Time	Set-Up Time	Hold Time
S-Bus	15	19	15	19
M-Bus	15	16	15	16
$\overline{P}_0$-$\overline{P}_7$	15	9	15	9
LB	20	0	20	0
$\overline{IE}$ I_{0123} (See Note)	55 t_{pwL} + 33	0	55 t_{pwL} + 40	0
$\overline{GE}$	15	13	15	13
$\overline{GAR}$	15	17	15	17
$\overline{ID}$	42	14	42	14
$\overline{P}_0$-$\overline{P}_7$ Hold Time Relative to LB	–	25	–	25

Note: t_{pwL} is the Clock LOW Time. Both Set-up times must be met.

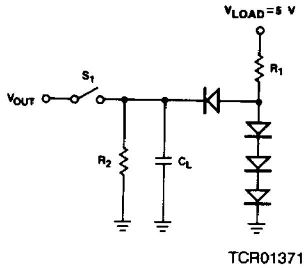
SWITCHING TEST CIRCUITS

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{1K}}$$

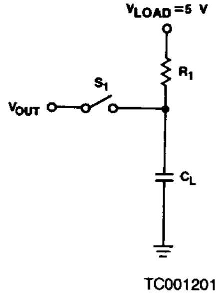
B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{\frac{I_{OL} + V_{OL}}{R_2}}$$

C. OPEN-COLLECTOR OUTPUTS



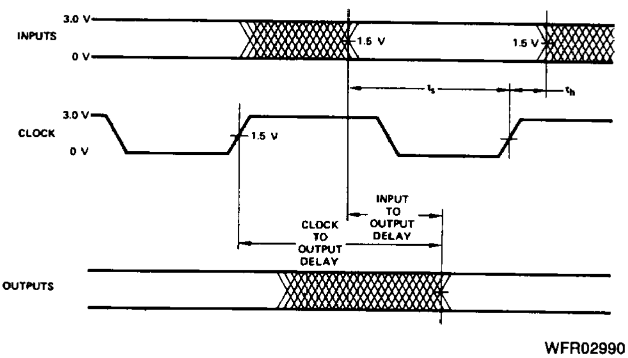
$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

TEST OUTPUT LOADS

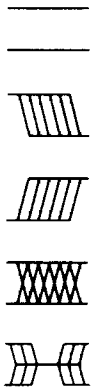
Pin Label	Test Circuit	R_1	R_2
Group Signal	B	300	2.4K
Group Advance Receive	B	300	2.4K
Ripple Disable	B	300	2.4K
Parallel Disable	B	300	2.4K
Interrupt Request	C	390	–
S_{0-2}	A	300	1K
Status Overflow	B	300	2.4K
V_{0-2}	A	300	1K
M_{0-7}	A	300	1K

Notes:
1. C_L = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test. S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0 pF for output disable tests.
5. Disable times measured from 0.5 V change on the output.

SWITCHING WAVEFORMS



KEY TO SWITCHING WAVEFORMS



WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

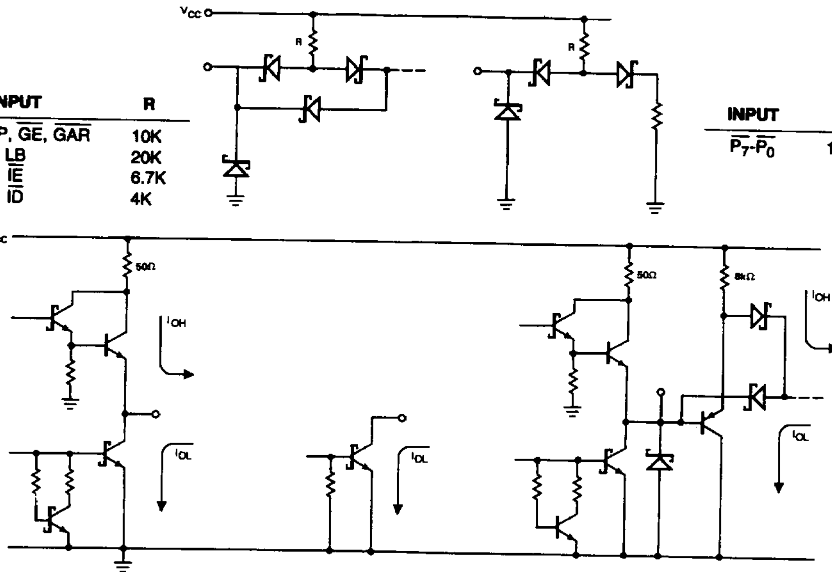
KS000010

Notes on Test Methods

The following points give the general philosophy that we apply to tests that must be properly engineered if they are to be implemented in an automatic environment. The specifics of what philosophies applied to which test are shown.

1. Ensure the part is adequately decoupled at the test head. Large changes in supply current when the device switches may cause function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5 – 8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins which may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0$ V and $V_{IH} \geqslant 3$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide actual Sentry programs, under license from Sentry.
7. Capacitive Loading for A.C. Testing
   Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another, but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters that call for a smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays" that measure the propagation delays into and out of the high impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is peformed at the higher load capacitance (typically 50 pF) and engineering correlations based on data taken with a bench set up are used to predict the result at the lower capacitance.
   Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench set up and the knowledge that certain D.C. measurements (I_{OH}, I_{OL}, for example) have already been taken and are within specification. In some cases, special D.C. tests are performed in order to facilitate this correlation.
8. Threshold Testing
   The noise associated with automatic testing, the long, inductive cables, and the high gain of bipolar devices when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and A.C. testing are performed at "hard" input levels rather than at V_{IL} max and V_{IH} min.
9. A.C. Testing
   Occasionally, parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other A.C. tests that have been performed. These correlations are arrived at by the cognizant engineer by using data from precise bench measurements in conjunction with the knowledge that certain D.C. parameters have already been measured and are within specification.
   In some cases, certain A.C. tests are redundant since they can be shown to be predicted by other tests that have already been performed. In these cases, the redundant tests are not performed.

INPUT/OUTPUT CURRENT DIAGRAM



INPUT	R
I_0-I_3, CP, $\overline{GE}$, $\overline{GAR}$	10K
$\overline{LB}$	20K
$\overline{IE}$	6.7K
$\overline{ID}$	4K

INPUT	R
$\overline{P_7}$-$\overline{P_0}$	10K

NORMAL OUTPUTS

V_0-V_3	$\overline{SO}$
$\overline{GAS}$	PD
$\overline{GS}$	$\overline{RD}$

OPEN COLLECTOR OUTPUT

$\overline{IR}$

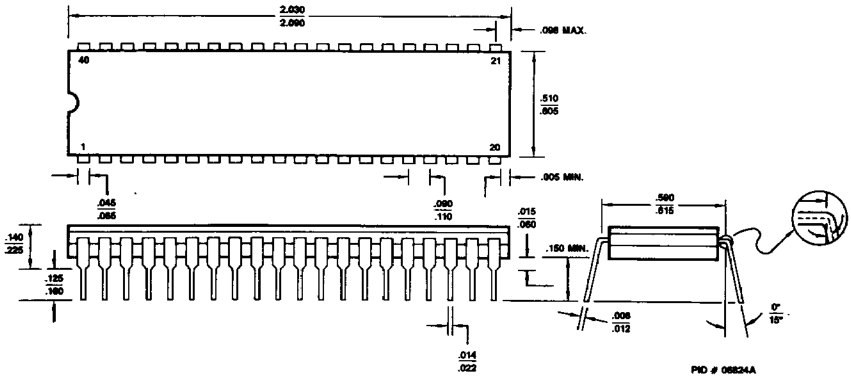
THREE-STATE OUTPUTS

M_0-M_7
S_0-S_2

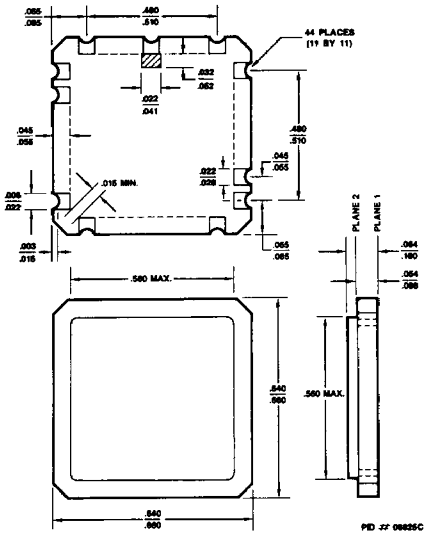
IC000451

PHYSICAL DIMENSIONS*

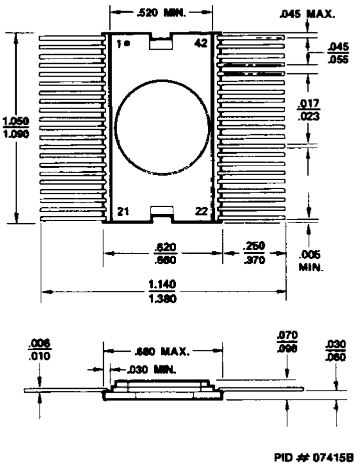
CD 040



CL 044



CFT042



*For Reference only

ADVANCED MICRO DEVICES
DOMESTIC SALES OFFICES

ALABAMA .... (205) 882-9122
ARIZONA,
Tempe .... (602) 242-4400
Tucson .... (602) 792-1200
CALIFORNIA,
El Segundo .... (213) 640-3210
Newport Beach .... (714) 752-6262
San Diego .... (619) 560-7030
Sunnyvale .... (408) 720-8811
Woodland Hills .... (818) 992-4155
COLORADO .... (303) 741-2900
CONNECTICUT, ... (203) 264-7800
FLORIDA,
Clearwater .... (813) 530-9971
Ft. Lauderdale .... (305) 484-8600
Melbourne .... (305) 729-0496
Orlando .... (305) 859-0831
GEORGIA .... (404) 449-7920
ILLINOIS .... (312) 773-4422
INDIANA .... (317) 244-7207
KANSAS .... (913) 451-3115
MARYLAND .... (301) 796-9310
MASSACHUSETTS .... (617) 273-3970
MINNESOTA .... (612) 938-0001
MISSOURI .... (314) 275-4415
NEW JERSEY .... (201) 299-0002
NEW YORK,
Liverpool .... (315) 457-5400
Poughkeepsie .... (914) 471-8180
Woodbury .... (516) 364-8020
NORTH CAROLINA, ... (919) 847-8471
OREGON .... (503) 245-0080
OHIO,
Columbus .... (614) 891-6455
PENNSYLVANIA,
Allentown .... (215) 398-8006
Willow Grove .... (215) 657-3101
TEXAS,
Austin .... (512) 346-7830
Dallas .... (214) 934-9099
Houston .... (713) 785-9001
WASHINGTON .... (206) 455-3600
WISCONSIN .... (414) 782-7748

INTERNATIONAL SALES OFFICES

BELGIUM,
Bruxelles .... TEL: .... (02) 771 99 93
FAX: .... (02) 762-3716
TLX: 61028
CANADA, Ontario,
Kanata .... TEL: .... (613) 592-0090
Willowdale .... TEL: .... (416) 224-5193
FAX: .... (416) 224-0056
FRANCE,
Paris .... TEL: .... (01) 45 60 00 55
FAX: .... (01) 46 86 21 85
TLX: 202053F
GERMANY,
Hannover area .... TEL: .... (05143) 50 55
FAX: .... (05143) 55 53
TLX: 925287
München .... TEL: .... (089) 41 14-0
FAX: .... (089) 406490
TLX: 523883
Stuttgart .... TEL: .... (0711) 62 33 77
FAX: .... (0711) 625187
TLX: 721882
HONG KONG,
Kowloon .... TEL: 3-695377
FAX: 1234276
TLX: 50426
ITALY, Milano .... TEL: .... (02) 3390541
FAX: .... (02) 3498000
TLX: 315286
JAPAN, Tokyo .... TEL: .... (03) 345-8241
FAX: 3425196
TLX: .... J24064 AMDTKOJ
LATIN AMERICA,
Ft. Lauderdale, ... TEL: .... (305) 484-8600
FAX: .... (305) 485-9736
TLX: .... 5109554261 AMDFTL
SWEDEN, Stockholm .... TEL: .... (08) 733 03 50
FAX: .... (08) 733 22 85
TLX: 11602
UNITED KINGDOM,
Manchester area .... TEL: .... (0925) 828008
FAX: .... (0925) 827693
TLX: 628524
London area .... TEL: .... (04862) 22121
FAX: .... (04862) 22179
TLX: 859103

NORTH AMERICAN REPRESENTATIVES

CALIFORNIA
I[2] INC .... OEM (408) 988-3400
DISTI (408) 496-6868
IDAHO
INTERMOUNTAIN TECH MKGT .... (208) 888-6071
INDIANA
SAI MARKETING CORP .... (317) 241-9276
IOWA
LORENZ SALES .... (319) 377-4666
MICHIGAN
SAI MARKETING CORP .... (313) 227-1786
NEBRASKA
LORENZ SALES .... (402) 475-4660
NEW MEXICO
THORSON DESERT STATES .... (505) 293-8555
NEW YORK
NYCOM, INC .... (315) 437-8343
OHIO
Dayton
DOLFUSS ROOT & CO .... (513) 433-6776
Strongsville
DOLFUSS ROOT & CO .... (216) 238-0300
PENNSYLVANIA
DOLFUSS ROOT & CO .... (412) 221-4420
UTAH
R[2] MARKETING .... (801) 595-0631

ADVANCED MICRO DEVICES 901 Thompson Pl., P.O. Box 3453, Sunnyvale, CA 94088, USA
TEL: (408) 732-2400 • TWX: 910-339-9280 • TELEX: 34-6306 • TOLL FREE: (800) 538-8450

Printed in U.S.A. AIS-WCP-2300-01/87-0