Am29LV640MU

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **25301** Revision **C** Amendment **+1** Issue Date **June 12, 2003**

ADVANCE INFORMATION

Am29LV640MU

64 Megabit (4 M x 16-Bit) MirrorBit™ 3.0 Volt-only Uniform Sector Flash Memory with

VersatileI/O™ Control

DISTINCTIVE CHARACTERISTICS

ARCHITECTURAL ADVANTAGES

- **Single power supply operation**
  - 3 V for read, erase, and program operations
- **VersatileI/O™ control**
  - Device generates data output voltages and tolerates data input voltages on the CE# and DQ inputs/outputs as determined by the voltage on the V_{IO} pin; operates from 1.65 to 3.6 V
- **Manufactured on 0.23 µm MirrorBit process technology**
- **SecSi™ (Secured Silicon) Sector region**
  - 128-word sector for permanent, secure identification through an 8-word random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked at the factory or by the customer
- **Flexible sector architecture**
  - One hundred twenty-eight 32 Kword sectors
- **Compatibility with JEDEC standards**
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- **Minimum 100,000 erase cycle guarantee per sector**
- **20-year data retention at 125°C**

PERFORMANCE CHARACTERISTICS

- **High performance**
  - 90 ns access time
  - 25 ns page read times
  - 0.5 s typical sector erase time
  - 22 µs typical effective write buffer word programming time: 16-word write buffer reduces overall programming time for multiple-word/byte updates
  - 4-word page read buffer
  - 16-word write buffer
- **Low power consumption (typical values at 3.0 V, 5 MHz)**
  - 30 mA typical active read current
  - 50 mA typical erase/program current
  - 1 µA typical standby mode current
- **Package options**
  - 63-ball Fine-Pitch BGA
  - 64-ball Fortified BGA

SOFTWARE & HARDWARE FEATURES

- **Software features**
  - Program Suspend & Resume: read other sectors before programming operation is completed
  - Erase Suspend & Resume: read/program other sectors before an erase operation is completed
  - Data# polling & toggle bits provide status
  - Unlock Bypass Program command reduces overall multiple-word programming time
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
- **Hardware features**
  - Sector Group Protection: hardware-level method of preventing write operations within a sector group
  - Temporary Sector Unprotect: V_{ID}-level method of changing code in locked sectors
  - ACC (high voltage) input accelerates programming time for higher throughput during system production
  - Hardware reset input (RESET#) resets device
  - Ready/Busy# output (RY/BY#) indicates program or erase cycle completion

Publication# **25301** Rev: **C** Amendment/**1**
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GENERAL DESCRIPTION

The Am29LV640MU is a 64 Mbit, 3.0 volt single power supply flash memory device organized as 4,194,304 words. The device has a 16-bit only data bus, and can be programmed either in the host system or in standard EPROM programmers.

An access time of 90, 100, 110, or 120 ns is available. Note that each access time has a specific operating voltage range (V_{CC}) and an I/O voltage range (V_{IO}), as specified in the Product Selector Guide and the Ordering Information sections. The device is offered in a 63-ball Fine-Pitch BGA or 64-ball Fortified BGA package. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0 volt power supply** for both read and write functions. In addition to a V_{CC} input, a high-voltage **accelerated program (ACC)** input provides shorter programming times through increased current. This feature is intended to facilitate factory throughput during system production, but may also be used in the field if desired.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation has begun, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

The **VersatileI/O™** (V_{IO}) control allows the host system to set the voltage levels that the device generates and tolerates on the CE# control input and DQ I/Os to the same voltage level that is asserted on the V_{IO} pin. Refer to the Ordering Information section for valid V_{IO} options.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses have been stable for a specified period of time.

The **SecSi™ (Secured Silicon) Sector** provides a 128-word area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

AMD MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

MIRRORBIT 64 MBIT DEVICE FAMILY

Device	Bus	Sector Architecture	Packages	V_{IO}	RY/BY#	WP#, ACC	WP# Protection
LV065MU	x8	Uniform (64 Kbyte)	48-pin TSOP (std. & rev. pinout), 63-ball FBGA	Yes	Yes	ACC only	No WP#
LV640MT/B	x8/x16	Boot (8 x 8 Kbyte at top & bottom)	48-pin TSOP, 63-ball Fine-pitch BGA, 64-ball Fortified BGA	No	Yes	WP#/ACC pin	2 x 8 Kbyte top or bottom
LV640MH/L	x8/x16	Uniform (64 Kbyte)	56-pin TSOP (std. & rev. pinout), 64 Fortified BGA	Yes	Yes	WP#/ACC pin	1 x 64 Kbyte high or low
LV641MH/L	x16	Uniform (32 Kword)	48-pin TSOP (std. & rev. pinout)	Yes	No	Separate WP# and ACC pins	1 x 32 Kword top or bottom
LV640MU	x16	Uniform (32 Kword)	63-ball Fine-pitch BGA, 64-ball Fortified BGA	Yes	Yes	ACC only	No WP#

RELATED DOCUMENTS

To download related documents, click on the following links or go to www.amd.com→Flash Memory→Product Information→MirrorBit→Flash Information→Technical Documentation.

MirrorBit™ Flash Memory Write Buffer Programming and Page Buffer Read

Implementing a Common Layout for AMD MirrorBit and Intel StrataFlash Memory Devices

AMD MirrorBit™ White Paper

Migrating from Single-byte to Three-byte Device IDs

Migration from Am29LV640DU to MirrorBit Am29LV640MU

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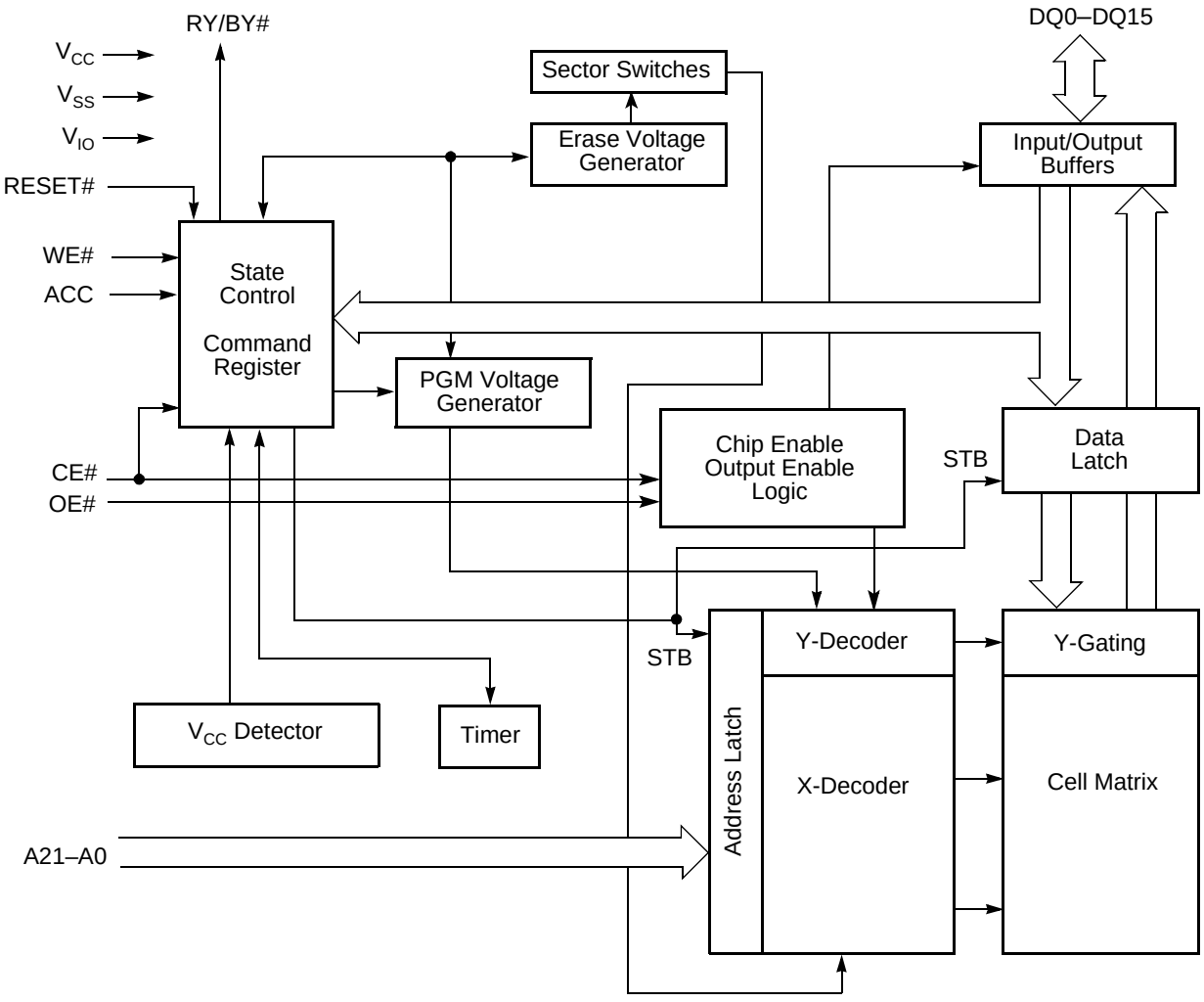
PRODUCT SELECTOR GUIDE

Part Number		Am29LV640MU					
Speed Option	V_{CC} = 3.0–3.6 V	**90R** (V_{IO} = 3.0–3.6 V)	**101R** (V_{IO} = 2.7–3.6 V)	**112R** (V_{IO} = 1.65–3.6 V)		**120R** (V_{IO} = 1.65–3.6 V)	
	V_{CC} = 2.7–3.6 V		**101** (V_{IO} = 2.7–3.6 V)		**112** (V_{IO} = 1.65–3.6 V)		**120** (V_{IO} = 1.65–3.6 V)
Max. Access Time (ns)		90	100	110		120	
Max. CE# Access Time (ns)		90	100	110		120	
Max. Page access time (t_{PACC})		25	30	30	40	30	40
Max. OE# Access Time (ns)		25	30	30	40	30	40

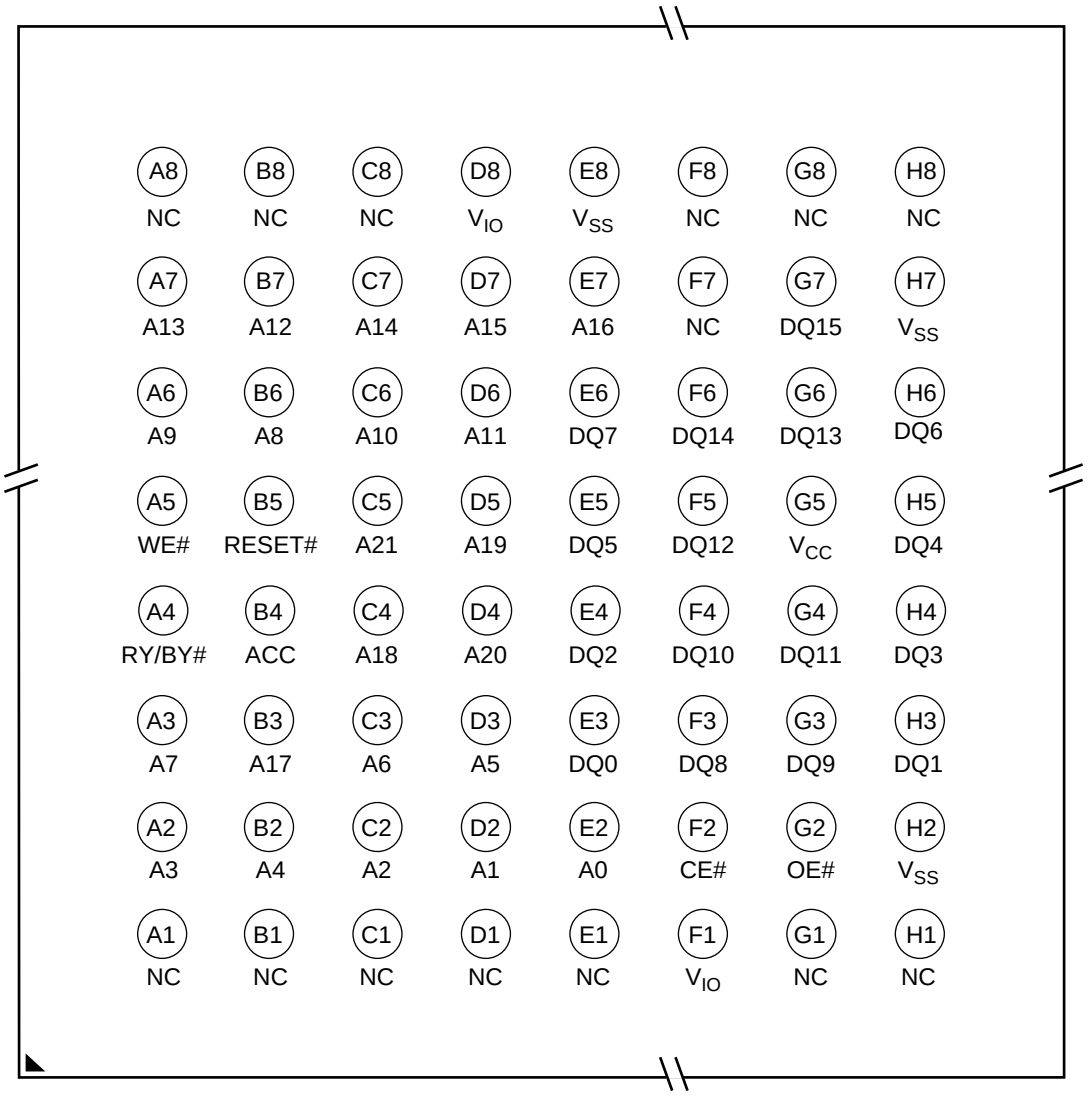
1. *See "AC Characteristics" for full specifications.*
2. *For the Am29LV640MU device, the last numeric digit in the speed option (e.g. 101, 112, 120) is used for internal purposes only. Please use OPNs as listed when placing orders.*

BLOCK DIAGRAM



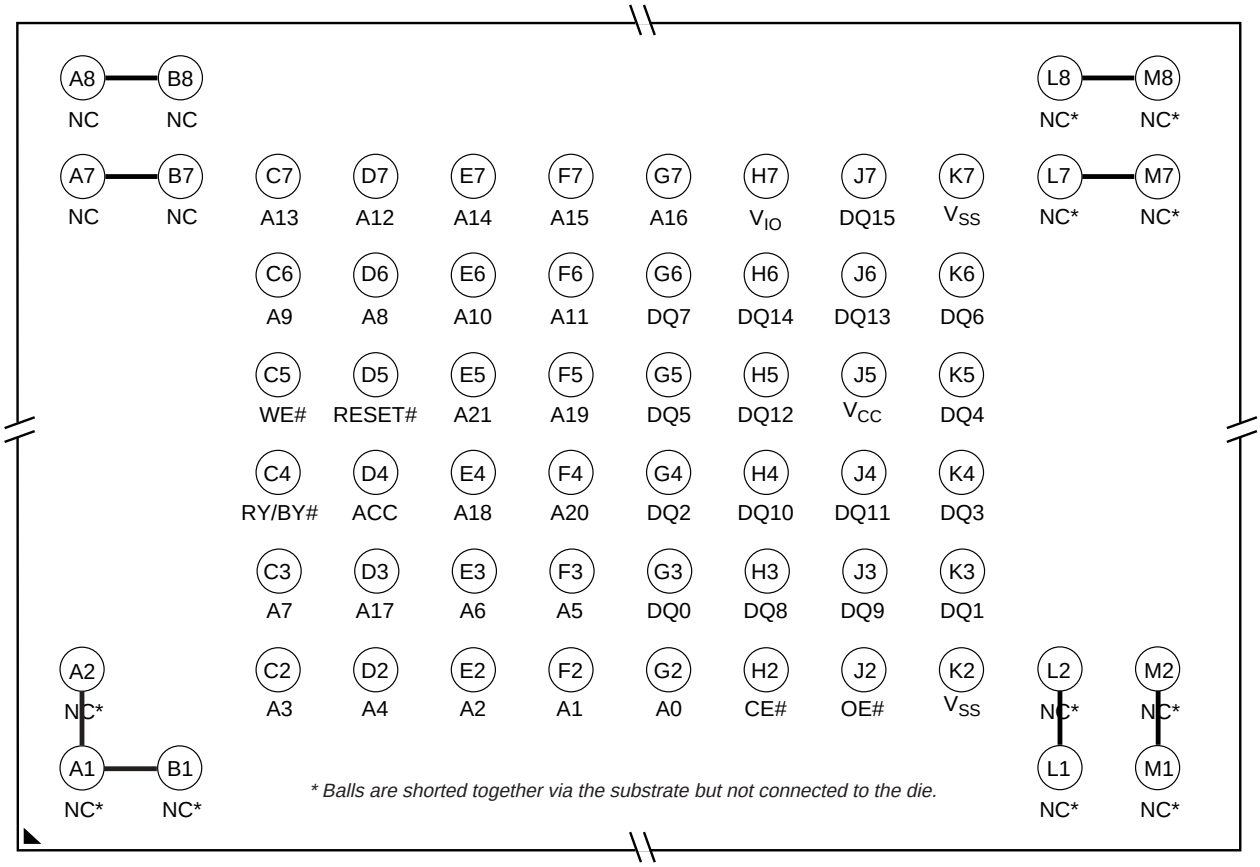
CONNECTION DIAGRAMS

64-Ball Fortified BGA
Top View, Balls Facing Down



CONNECTION DIAGRAMS

63-Ball Fine-Pitch BGA
Top View, Balls Facing Down



Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (TSOP, BGA, SSOP, PDIP, PLCC). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

A21–A0 = 22 Address inputs

DQ15–DQ0 = 15 Data inputs/outputs

CE# = Chip Enable input

OE# = Output Enable input

WE# = Write Enable input

ACC = Programming Acceleration input

RESET# = Hardware Reset Pin input

RY/BY# = Ready/Busy output

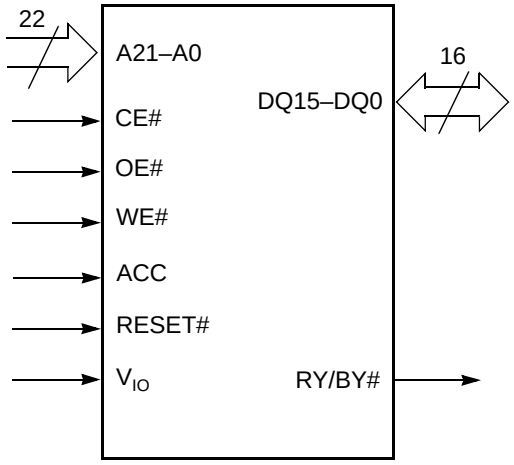
V_{CC} = 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)

V_{IO} = Output Buffer power

V_{SS} = Device Ground

NC = Pin Not Connected Internally

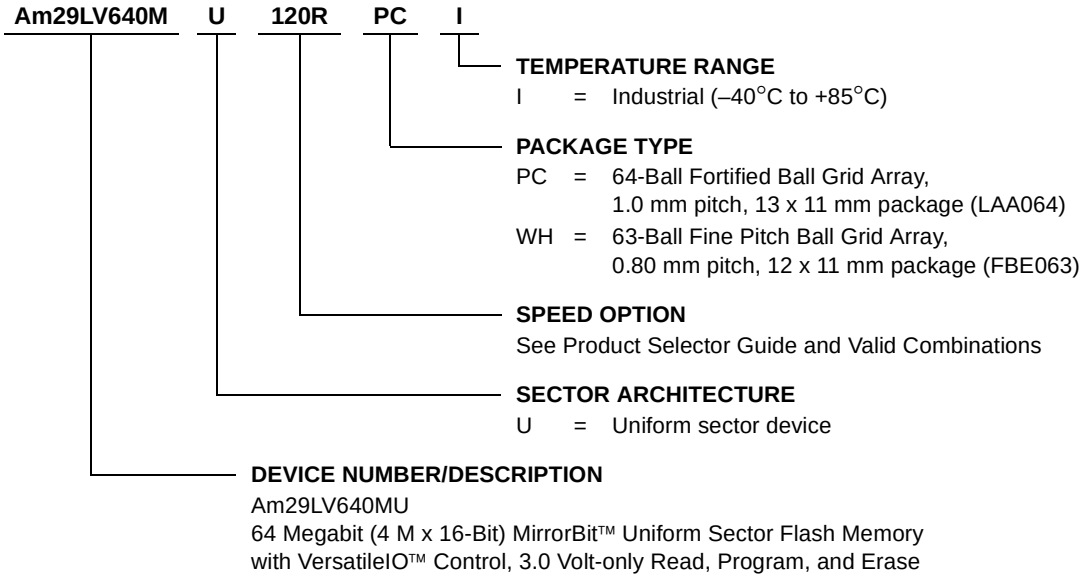
LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations for Fortified or Fine-Pitch BGA Package				Speed (ns)	V_{IO} Range	V_{CC} Range
Order Number		Package Marking				
Am29LV640MU90R	WHI	L640MU90R	I	90	3.0–3.6 V	3.0–3.6 V
	PCI	L640MU90N				
Am29LV640MU101	WHI	L640MU01V	I	100	2.7–3.6 V	2.7–3.6 V
	PCI	L640MU01P				
Am29LV640MU112	WHI	L640MU11V	I	110	1.65–3.6 V	
	PCI	L640MU11P				
Am29LV640MU120	WHI,	L640MU12V	I	120	1.65–3.6 V	
	PCI	L640MU12P				
Am29LV640MU101R	WHI,	L640MU01R	I	100	2.7–3.6 V	3.0–3.6 V
	PCI	L640MU01N				
Am29LV640MU112R	WHI,	L640MU11R	I	110	1.65–3.6 V	
	PCI	L640MU11N				
Am29LV640MU120R	WHI,	L640MU12R	I	120	1.65–3.6 V	
	PCI	L640MU12N				

Note:
For the Am29LV640MU device, the last numeric digit in the speed option (e.g. 101, 112, 120) is used for internal purposes only. Use OPNs as listed when placing orders.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	ACC	Addresses (Note 2)	DQ0–DQ15
Read	L	L	H	H	X	A_{IN}	D_{OUT}
Write (Program/Erase)	L	H	L	H	X	A_{IN}	(Note 3)
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 3)
Standby	$V_{CC} \pm 0.3$ V	X	X	$V_{CC} \pm 0.3$ V	H	X	High-Z
Output Disable	L	H	H	H	X	X	High-Z
Reset	X	X	X	L	X	X	High-Z
Sector Group Protect (Note 2)	L	H	L	V_{ID}	X	SA, A6=L, A3=L, A2=L, A1=H, A0=L	(Note 3)
Sector Group Unprotect (Note 2)	L	H	L	V_{ID}	X	SA, A6=H, A3=L, A2=L, A1=H, A0=L	(Note 3)
Temporary Sector Group Unprotect	X	X	X	V_{ID}	X	A_{IN}	(Note 3)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 11.5–12.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Addresses are A21:A0. Sector addresses are A21:A15.*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Unprotection" section.*
3. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm (see Figure 2).*

VersatileIO™ (V_{IO}) Control

The VersatileIO™ (V_{IO}) control allows the host system to set the voltage levels that the device generates and tolerates on CE# and DQ I/Os to the same voltage level that is asserted on V_{IO}. See "Ordering Information" on page 9 for V_{IO} options on this device.

For example, a $V_{I/O}$ of 1.65–3.6 volts allows for I/O at the 1.8 or 3 volt levels, driving and receiving signals to and from other 1.8 or 3 V devices on the same data bus.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 13 for the timing diagram.

Refer to the DC Characteristics table for the active current specification for reading array data.

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 4 words. The appropriate page is selected by the higher address bits A(max)–A2. Address bits A1–A0 determine the specific word within a page. This is an asynchronous operation; the microprocessor supplies the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the “read-page addresses” constant and changing the “intra-read page” addresses.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. The “Word Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2 indicates the address space that each sector occupies.

Refer to the DC Characteristics table for the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Write Buffer

Write Buffer Programming allows the system to write a maximum of 16 words in one programming operation. This results in faster effective programming time than the standard programming algorithms. See “Write Buffer” for more information.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput during system production.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the ACC pin returns the device to normal operation. *Note that the ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{IO} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{IO} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Refer to the DC Characteristics table for the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Refer to the DC Characteristics table for the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current. If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 15 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Sector Address Table

Sector	A21–A15							16-bit Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	0	000000–007FFF
SA1	0	0	0	0	0	0	1	008000–00FFFF
SA2	0	0	0	0	0	1	0	010000–017FFF
SA3	0	0	0	0	0	1	1	018000–01FFFF
SA4	0	0	0	0	1	0	0	020000–027FFF
SA5	0	0	0	0	1	0	1	028000–02FFFF
SA6	0	0	0	0	1	1	0	030000–037FFF
SA7	0	0	0	0	1	1	1	038000–03FFFF
SA8	0	0	0	1	0	0	0	040000–047FFF
SA9	0	0	0	1	0	0	1	048000–04FFFF
SA10	0	0	0	1	0	1	0	050000–057FFF
SA11	0	0	0	1	0	1	1	058000–05FFFF
SA12	0	0	0	1	1	0	0	060000–067FFF
SA13	0	0	0	1	1	0	1	068000–06FFFF
SA14	0	0	0	1	1	1	0	070000–077FFF
SA15	0	0	0	1	1	1	1	078000–07FFFF
SA16	0	0	1	0	0	0	0	080000–087FFF
SA17	0	0	1	0	0	0	1	088000–08FFFF
SA18	0	0	1	0	0	1	0	090000–097FFF
SA19	0	0	1	0	0	1	1	098000–09FFFF
SA20	0	0	1	0	1	0	0	0A0000–0A7FFF
SA21	0	0	1	0	1	0	1	0A8000–0AFFFF
SA22	0	0	1	0	1	1	0	0B0000–0B7FFF
SA23	0	0	1	0	1	1	1	0B8000–0BFFFF
SA24	0	0	1	1	0	0	0	0C0000–0C7FFF
SA25	0	0	1	1	0	0	1	0C8000–0CFFFF
SA26	0	0	1	1	0	1	0	0D0000–0D7FFF
SA27	0	0	1	1	0	1	1	0D8000–0DFFFF
SA28	0	0	1	1	1	0	0	0E0000–0E7FFF
SA29	0	0	1	1	1	0	1	0E8000–0EFFFF
SA30	0	0	1	1	1	1	0	0F0000–0F7FFF
SA31	0	0	1	1	1	1	1	0F8000–0FFFFF
SA64	1	0	0	0	0	0	0	200000–207FFF
SA65	1	0	0	0	0	0	1	208000–20FFFF
SA66	1	0	0	0	0	1	0	210000–217FFF
SA67	1	0	0	0	0	1	1	218000–21FFFF
SA68	1	0	0	0	1	0	0	220000–227FFF
SA69	1	0	0	0	1	0	1	228000–22FFFF
SA70	1	0	0	0	1	1	0	230000–237FFF
SA71	1	0	0	0	1	1	1	238000–23FFFF
SA72	1	0	0	1	0	0	0	240000–247FFF
SA73	1	0	0	1	0	0	1	248000–24FFFF
SA74	1	0	0	1	0	1	0	250000–257FFF
SA75	1	0	0	1	0	1	1	258000–25FFFF

Sector	A21–A15							16-bit Address Range (in hexadecimal)
SA32	0	1	0	0	0	0	0	100000–107FFF
SA33	0	1	0	0	0	0	1	108000–10FFFF
SA34	0	1	0	0	0	1	0	110000–117FFF
SA35	0	1	0	0	0	1	1	118000–11FFFF
SA36	0	1	0	0	1	0	0	120000–127FFF
SA37	0	1	0	0	1	0	1	128000–12FFFF
SA38	0	1	0	0	1	1	0	130000–137FFF
SA39	0	1	0	0	1	1	1	138000–13FFFF
SA40	0	1	0	1	0	0	0	140000–147FFF
SA41	0	1	0	1	0	0	1	148000–14FFFF
SA42	0	1	0	1	0	1	0	150000–157FFF
SA43	0	1	0	1	0	1	1	158000–15FFFF
SA44	0	1	0	1	1	0	0	160000–167FFF
SA45	0	1	0	1	1	0	1	168000–16FFFF
SA46	0	1	0	1	1	1	0	170000–177FFF
SA47	0	1	0	1	1	1	1	178000–17FFFF
SA48	0	1	1	0	0	0	0	180000–187FFF
SA49	0	1	1	0	0	0	1	188000–18FFFF
SA50	0	1	1	0	0	1	0	190000–197FFF
SA51	0	1	1	0	0	1	1	198000–19FFFF
SA52	0	1	1	0	1	0	0	1A0000–1A7FFF
SA53	0	1	1	0	1	0	1	1A8000–1AFFFF
SA54	0	1	1	0	1	1	0	1B0000–1B7FFF
SA55	0	1	1	0	1	1	1	1B8000–1BFFFF
SA56	0	1	1	1	0	0	0	1C0000–1C7FFF
SA57	0	1	1	1	0	0	1	1C8000–1CFFFF
SA58	0	1	1	1	0	1	0	1D0000–1D7FFF
SA59	0	1	1	1	0	1	1	1D8000–1DFFFF
SA60	0	1	1	1	1	0	0	1E0000–1E7FFF
SA61	0	1	1	1	1	0	1	1E8000–1EFFFF
SA62	0	1	1	1	1	1	0	1F0000–1F7FFF
SA63	0	1	1	1	1	1	1	1F8000–1FFFFF
SA96	1	1	0	0	0	0	0	300000–307FFF
SA97	1	1	0	0	0	0	1	308000–30FFFF
SA98	1	1	0	0	0	1	0	310000–317FFF
SA99	1	1	0	0	0	1	1	318000–31FFFF
SA100	1	1	0	0	1	0	0	320000–327FFF
SA101	1	1	0	0	1	0	1	328000–32FFFF
SA102	1	1	0	0	1	1	0	330000–337FFF
SA103	1	1	0	0	1	1	1	338000–33FFFF
SA104	1	1	0	1	0	0	0	340000–347FFF
SA105	1	1	0	1	0	0	1	348000–34FFFF
SA106	1	1	0	1	0	1	0	350000–357FFF
SA107	1	1	0	1	0	1	1	358000–35FFFF

Table 2. Sector Address Table (Continued)

Sector	A21–A15							16-bit Address Range (in hexadecimal)
SA76	1	0	0	1	1	0	0	260000–267FFF
SA77	1	0	0	1	1	0	1	268000–26FFFF
SA78	1	0	0	1	1	1	0	270000–277FFF
SA79	1	0	0	1	1	1	1	278000–27FFFF
SA80	1	0	1	0	0	0	0	280000–287FFF
SA81	1	0	1	0	0	0	1	288000–28FFFF
SA82	1	0	1	0	0	1	0	290000–297FFF
SA83	1	0	1	0	0	1	1	298000–29FFFF
SA84	1	0	1	0	1	0	0	2A0000–2A7FFF
SA85	1	0	1	0	1	0	1	2A8000–2AFFFF
SA86	1	0	1	0	1	1	0	2B0000–2B7FFF
SA87	1	0	1	0	1	1	1	2B8000–2BFFFF
SA88	1	0	1	1	0	0	0	2C0000–2C7FFF
SA89	1	0	1	1	0	0	1	2C8000–2CFFFF
SA90	1	0	1	1	0	1	0	2D0000–2D7FFF
SA91	1	0	1	1	0	1	1	2D8000–2DFFFF
SA92	1	0	1	1	1	0	0	2E0000–2E7FFF
SA93	1	0	1	1	1	0	1	2E8000–2EFFFF
SA94	1	0	1	1	1	1	0	2F0000–2F7FFF
SA95	1	0	1	1	1	1	1	2F8000–2FFFFF

Sector	A21–A15							16-bit Address Range (in hexadecimal)
SA108	1	1	0	1	1	0	0	360000–367FFF
SA109	1	1	0	1	1	0	1	368000–36FFFF
SA110	1	1	0	1	1	1	0	370000–377FFF
SA111	1	1	0	1	1	1	1	378000–37FFFF
SA112	1	1	1	0	0	0	0	380000–387FFF
SA113	1	1	1	0	0	0	1	388000–38FFFF
SA114	1	1	1	0	0	1	0	390000–397FFF
SA115	1	1	1	0	0	1	1	398000–39FFFF
SA116	1	1	1	0	1	0	0	3A0000–3A7FFF
SA117	1	1	1	0	1	0	1	3A8000–3AFFFF
SA118	1	1	1	0	1	1	0	3B0000–3B7FFF
SA119	1	1	1	0	1	1	1	3B8000–3BFFFF
SA120	1	1	1	1	0	0	0	3C0000–3C7FFF
SA121	1	1	1	1	0	0	1	3C8000–3CFFFF
SA122	1	1	1	1	0	1	0	3D0000–3D7FFF
SA123	1	1	1	1	0	1	1	3D8000–3DFFFF
SA124	1	1	1	1	1	0	0	3E0000–3E7FFF
SA125	1	1	1	1	1	0	1	3E8000–3EFFFF
SA126	1	1	1	1	1	1	0	3F0000–3F7FFF
SA127	1	1	1	1	1	1	1	3F8000–3FFFFF

Note: *All sectors are 32 Kwords in size.*

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires VID on address pin A9. Address pins A6, A3, A2, A1, and A0 must be as shown in Table 3.

In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 2). Table 3 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 10. This method does not require V_{ID}. Refer to the Autoselect Command Sequence section for more information.

Table 3. Autoselect Codes, (High Voltage Method)

Description		CE#	OE#	WE#	A21 to A15	A14 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ15 to DQ0
Manufacturer ID: AMD		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	0001h
Device ID	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	227Eh
	Cycle 2										H	H	L	2213h
	Cycle 3										H	H	H	2201h
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	XX01h (protected), XX00h (unprotected)
SecSi Sector Indicator Bit (DQ7)		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	XX98h (factory locked), XX18h (not factory locked)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.*

Sector Group Protection and Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector group. In this device, a sector group consists of four adjacent sectors that are protected or unprotected at the same time (see Table 4). The hardware sector group unprotection feature re-enables both program and erase operations in previously protected sector groups. Sector group protection/unprotection can be implemented via two methods.

Sector protection/unprotection requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 23 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector group unprotect, all unprotected sector groups must first be protected prior to the first sector group unprotect write cycle.

The device is shipped with all sector groups unprotected. AMD offers the option of programming and protecting sector groups at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector group is protected or unprotected. See the Autoselect Mode section for details.

Table 4. Sector Group Protection/Unprotection Address Table

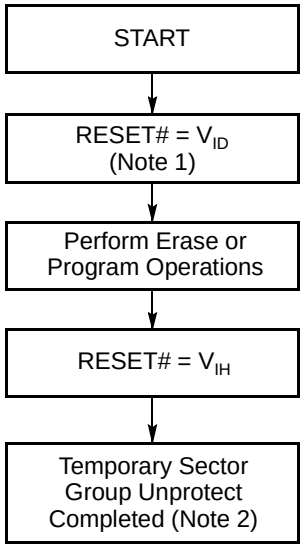
Sector Group	A21–A17
SA0–SA3	00000
SA4–SA7	00001
SA8–SA11	00010
SA12–SA15	00011
SA16–SA19	00100
SA20–SA23	00101
SA24–SA27	00110
SA28–SA31	00111
SA32–SA35	01000
SA36–SA39	01001
SA40–SA43	01010
SA44–SA47	01011
SA48–SA51	01100
SA52–SA55	01101
SA56–SA59	01110
SA60–SA63	01111
SA64–SA67	10000
SA68–SA71	10001
SA72–SA75	10010
SA76–SA79	10011
SA80–SA83	10100
SA84–SA87	10101
SA88–SA91	10110
SA92–SA95	10111
SA96–SA99	11000
SA100–SA103	11001
SA104–SA107	11010
SA108–SA111	11011
SA112–SA115	11100
SA116–SA119	11101
SA120–SA123	11110
SA124–SA127	11111

Note: *All sector groups are 128 Kwords in size.*

Temporary Sector Group Unprotect

*(**Note:** In this device, a sector group consists of four adjacent sectors that are protected or unprotected at the same time (see Table 4).*

This feature allows temporary unprotection of previously protected sector groups to change data in-system. The Sector Group Unprotect mode is activated by setting the RESET# pin to VID. During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sector groups are protected again. Figure 1 shows the algorithm, and Figure 22 shows the timing diagrams, for this feature.



Notes:

1. *All protected sector groups unprotected.*
2. *All previously protected sector groups are protected once again.*

Figure 1. Temporary Sector Group Unprotect Operation

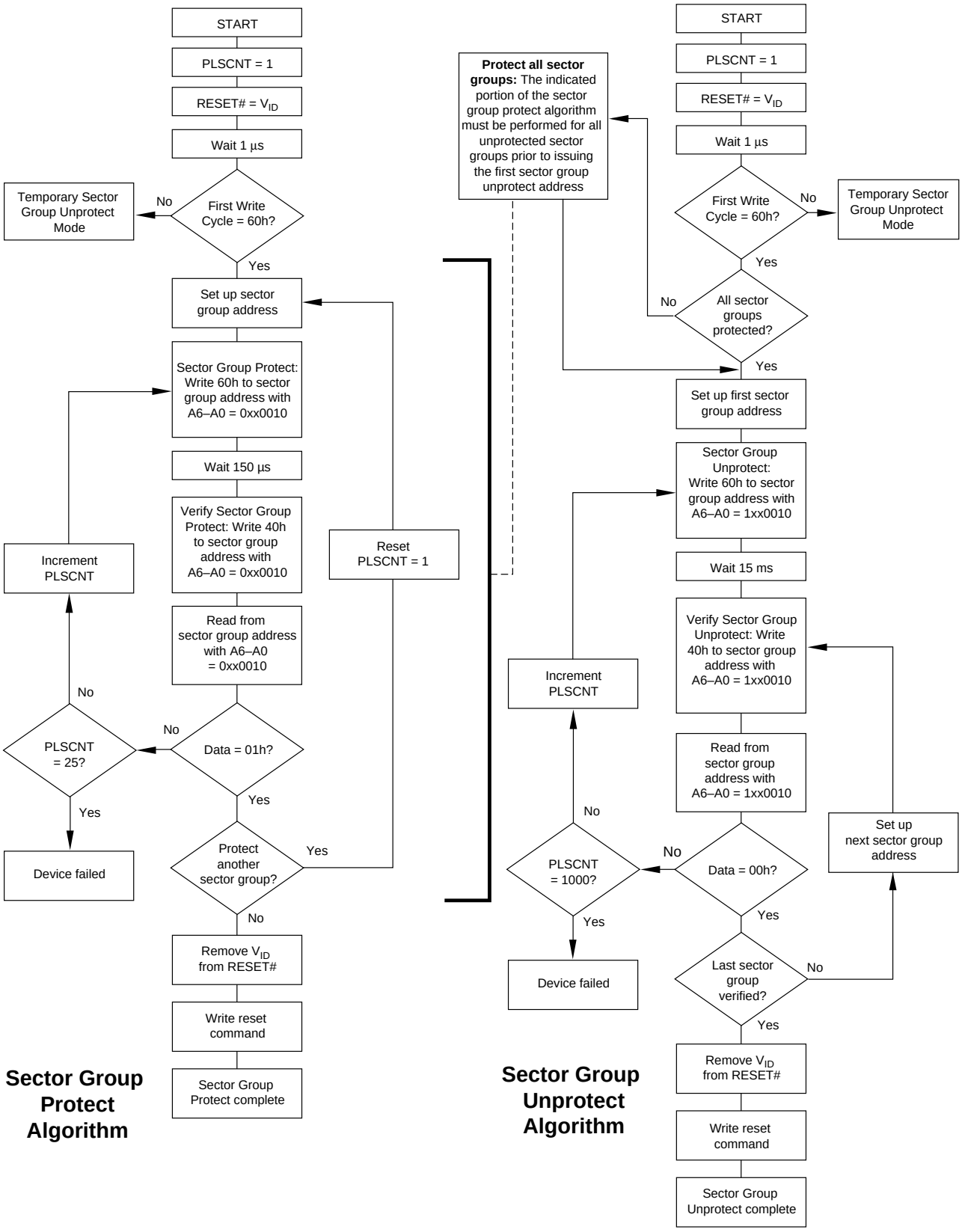


Figure 2. In-System Sector Group Protect/Unprotect Algorithms

SecSi (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is 128 words in length, and uses a SecSi Sector Indicator Bit (DQ7) to indicate whether or not the SecSi Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

AMD offers the device with the SecSi Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory, and has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a "1." The customer-lockable version is shipped with the SecSi Sector unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also has the SecSi Sector Indicator Bit permanently set to a "0." Thus, the SecSi Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The SecSi sector address space in this device is allocated as follows:

Table 5. SecSi Sector Contents

SecSi Sector Address Range	Standard Factory Locked	ExpressFlash Factory Locked	Customer Lockable
000000h–000007h	ESN	ESN or determined by customer	Determined by customer
000008h–00007Fh	Unavailable	Determined by customer	

The system accesses the SecSi Sector through a command sequence (see "Enter SecSi Sector/Exit SecSi Sector Command Sequence"). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

Factory Locked: SecSi Sector Programmed and Protected At the Factory

In devices with an ESN, the SecSi Sector is protected when the device is shipped from the factory. The SecSi Sector cannot be modified in any way. See Table 5 for SecSi Sector addressing.

Customers may opt to have their code programmed by AMD through the AMD ExpressFlash service. The devices are then shipped from AMD's factory with the SecSi Sector permanently locked. Contact an AMD representative for details on using AMD's ExpressFlash service.

Customer Lockable: SecSi Sector NOT Programmed or Protected At the Factory

As an alternative to the factory-locked version, the device may be ordered such that the customer may program and protect the 128-word SecSi sector.

The system may program the SecSi Sector using the write-buffer, accelerated and/or unlock bypass methods, in addition to the standard programming command sequence. See Command Definitions.

Programming and protecting the SecSi Sector must be used with caution since, once protected, there is no procedure available for unprotecting the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

The SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the SecSi Sector without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.
- To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 3.

Once the SecSi Sector is programmed, locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing within the remainder of the array.

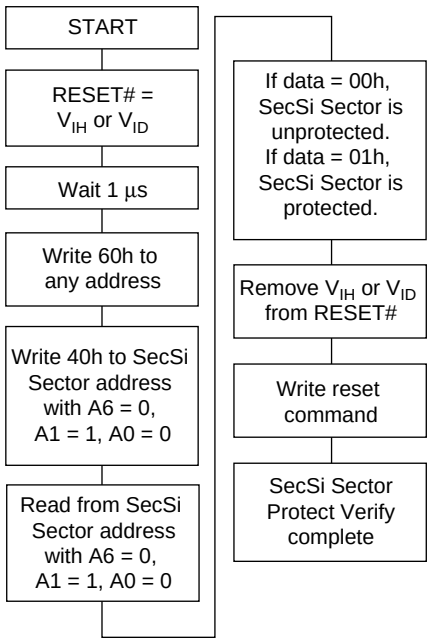


Figure 3. SecSi Sector Protect Verify

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 10 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 6–9. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 6–9. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact an AMD representative for copies of these documents.

Table 6. CFI Query Identification String

Addresses (x16)	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 7. System Interface String

Addresses (x16)	Data	Description
1Bh	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0007h	Typical timeout per single word write 2^N µs
20h	0007h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	000Ah	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0001h	Max. timeout for word write 2^N times typical
24h	0005h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 8. Device Geometry Definition

Addresses (x16)	Data	Description
27h	0017h	Device Size = 2^N byte
28h 29h	0001h 0000h	Flash Device Interface description (refer to CFI publication 100) (00h not supported)
2Ah 2Bh	0005h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0001h	Number of Erase Block Regions within device (01h = uniform device, 02h = boot device)
2Dh 2Eh 2Fh 30h	007Fh 0000h 0000h 0001h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	0000h 0000h 0000h 0000h	Erase Block Region 2 Information (refer to CFI publication 100)
35h 36h 37h 38h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to CFI publication 100)
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to CFI publication 100)

Table 9. Primary Vendor-Specific Extended Query

Addresses (x16)	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	0008h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Process Technology (Bits 7-2) 0010b = 0.23 µm MirrorBit
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0004h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0004h	Sector Protect/Unprotect scheme 04 = 29LV800 mode
4Ah	0000h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors in Bank
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0001h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0000h	Top/Bottom Boot Sector Flag 00h = Uniform Device without WP# protect, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Uniform sectors bottom WP# protect, 05h = Uniform sectors top WP# protect
50h	0001h	Program Suspend 00h = Not Supported, 01h = Supported

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 10 defines the valid register command sequences. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state.* A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Read-Only Operations table provides the read parameters, and Figure 13 shows the timing diagram.

Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Note that if DQ1 goes high during a Write Buffer Programming operation, the system must write the Write-to-Buffer-Abort Reset command sequence to reset the device for the next operation.

Autoselect Command Sequence

The autoselect command sequence allows the host system to read several identifier codes at specific addresses:

Identifier Code	A7:A0
Manufacturer ID	00h
Device ID, Cycle 1	01h
Device ID, Cycle 2	0Eh
Device ID, Cycle 3	0Fh
SecSi Sector Factory Protect	03h
Sector Protect Verify	(SA)02h

Note: *The device ID is read over three cycles. SA = Sector Address*

Table 10 shows the address and data requirements. This method is an alternative to that shown in Table 3, which is intended for PROM programmers and requires V_{ID} on address pin A9. The autoselect command sequence may be written to an address that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another autoselect command sequence.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

Enter SecSi Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing an 8-word random Electronic Serial Number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. Table 10 shows the address and data requirements for both command sequences. See also "SecSi (Secured Silicon) Sector Flash Memory Region" for further information.

Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 10 shows the address and data requirements for the word program command sequence.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 10 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h. The second cycle must contain the data 00h. The device then returns to the read mode.

Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 16 words in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming will occur. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system will program 6 unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort.

The fifth cycle writes the first address location and data to be programmed. A write-buffer-page is selected by address bits A_{MAX}–A_4. All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages. This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation will abort.

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter will be decremented for every data load operation. The host

system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Additionally, the last data loaded prior to the Program Buffer to Flash command will be programmed into the device. Note also that if an address location is loaded more than once into the buffer, the final data loaded for that address will be programmed.

Once the specified number of write buffer locations have been loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

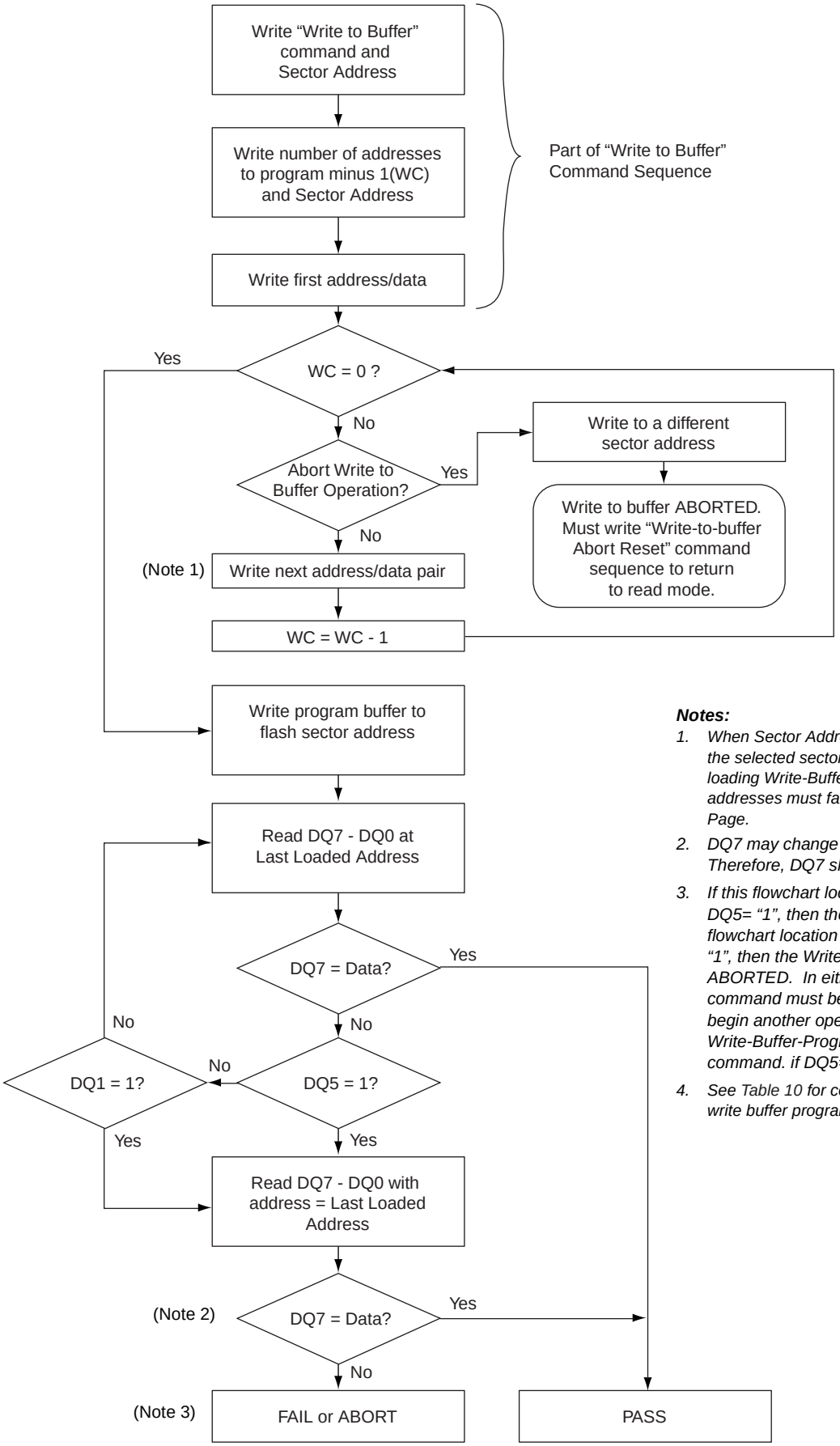
- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = 1, DQ7 = DATA# (for the last address location loaded), DQ6 = toggle, and DQ5=0. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

Accelerated Program

The device offers accelerated program operations through the ACC pin. When the system asserts V_{HH} on the ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the ACC pin to accelerate the operation. *Note that the ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result.*

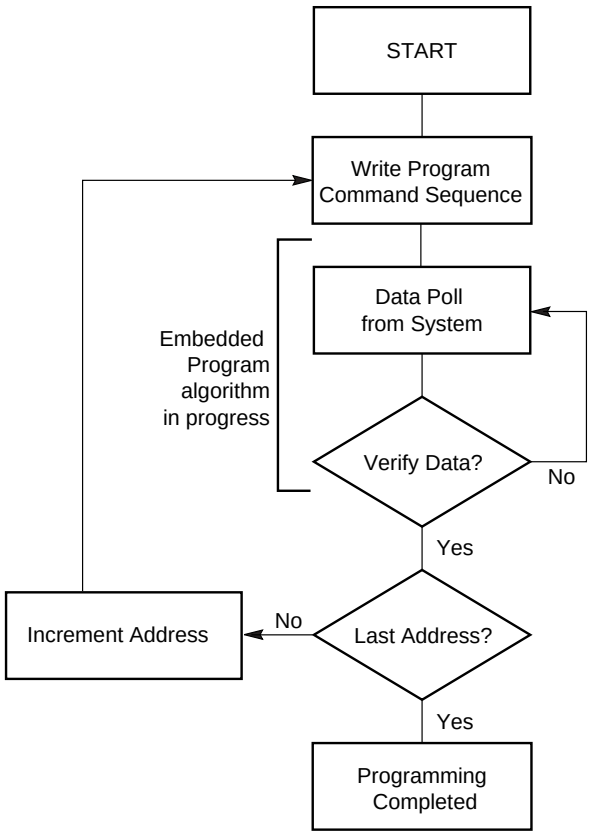
Figure 4 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 16 for timing diagrams.



Notes:

1. *When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.*
2. *DQ7 may change simultaneously with DQ5. Therefore, DQ7 should be verified.*
3. *If this flowchart location was reached because DQ5= "1", then the device FAILED. If this flowchart location was reached because DQ1= "1", then the Write to Buffer operation was ABORTED. In either case, the proper reset command must be written before the device can begin another operation. If DQ1=1, write the Write-Buffer-Programming-Abort-Reset command. if DQ5=1, write the Reset command.*
4. *See Table 10 for command sequences required for write buffer programming.*

Figure 4. Write Buffer Programming Operation



Note: *See Table 10 for program command sequence.*

Figure 5. Program Operation

Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15 µs maximum (5 µs typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the SecSi Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device has resume programming.

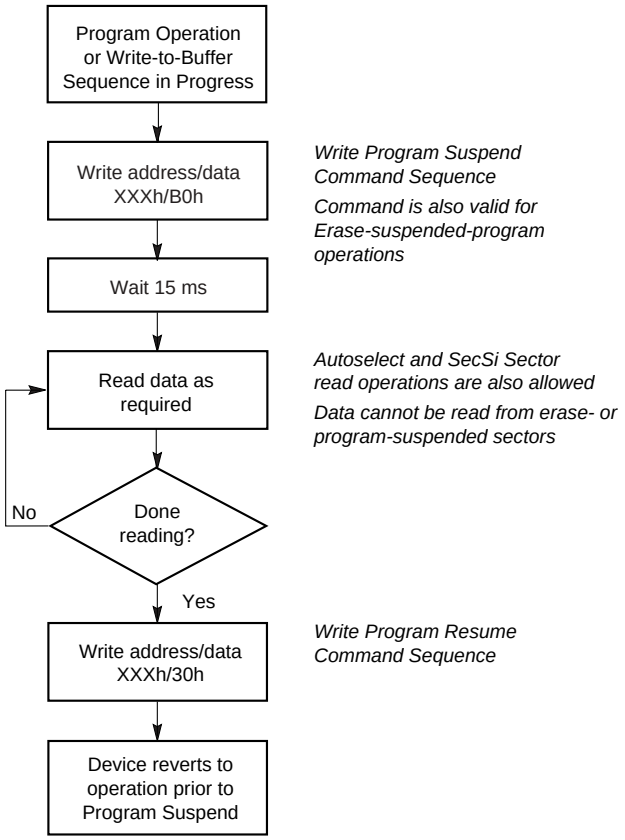


Figure 6. Program Suspend/Program Resume

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 10 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 6 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 10 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing sector. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 6 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 18 section for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

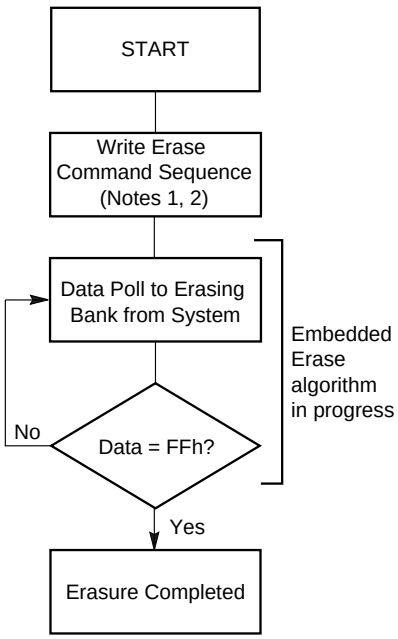
When the Erase Suspend command is written during the sector erase operation, the device requires a typical of 5 µs (maximum 20 µs) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard word program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Mode and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The address of the erase-suspended sector is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Notes:

1. *See Table 10 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 7. Erase Operation

Command Definitions

Table 10. Command Definitions

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	0001				
	Device ID (Note 9)	6	555	AA	2AA	55	555	90	X01	227E	X0E	2213	X0F	2201
	SecSi™ Sector Factory Protect (Note 10)	4	555	AA	2AA	55	555	90	X03	(Note 10)				
	Sector Group Protect Verify (Note 11)	4	555	AA	2AA	55	555	90	(SA)X02	00/01				
Enter SecSi Sector Region		3	555	AA	2AA	55	555	88						
Exit SecSi Sector Region		4	555	AA	2AA	55	555	90	XXX	00				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer (Note 12)		6	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
Program Buffer to Flash		1	SA	29										
Write to Buffer Abort Reset (Note 13)		3	555	AA	2AA	55	555	F0						
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 14)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 15)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (Note 16)		1	BA	B0										
Program/Erase Resume (Note 17)		1	BA	30										
CFI Query (Note 18)		1	55	98										

Legend:

X = Don't care

RA = Read Address of the memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address . Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A21–A15 uniquely select any sector.

WBL = Write Buffer Location. Address must be within the same write buffer page as PA.

WC = Word Count. Number of write buffer locations to load minus 1.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells indicate read cycles. All others are write cycles.*
4. *During unlock and command cycles, when lower address bits are 555 or 2AA as shown in table, address bits higher than A11 and data bits higher than DQ7 are don't care.*
5. *Unless otherwise noted, address bits A21–A11 are don't cares.*
6. *No unlock or command cycles required when device is in read mode.*
7. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the autoselect mode, or if DQ5 goes high (while the device is providing status information).*
8. *The fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care, except for RD, PD and WC. See the Autoselect Command Sequence section for more information.*
9. *The device ID must be read in three cycles.*
10. *The data is 98h for factory locked and 18h for not factory locked.*
11. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*
12. *The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 21.*
13. *Command sequence resets device for next command after aborted write-to-buffer operation.*
14. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
15. *The Unlock Bypass Reset command is required to return to the read mode when the device is in the unlock bypass mode.*
16. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
17. *The Erase Resume command is valid only during the Erase Suspend mode.*
18. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 11 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

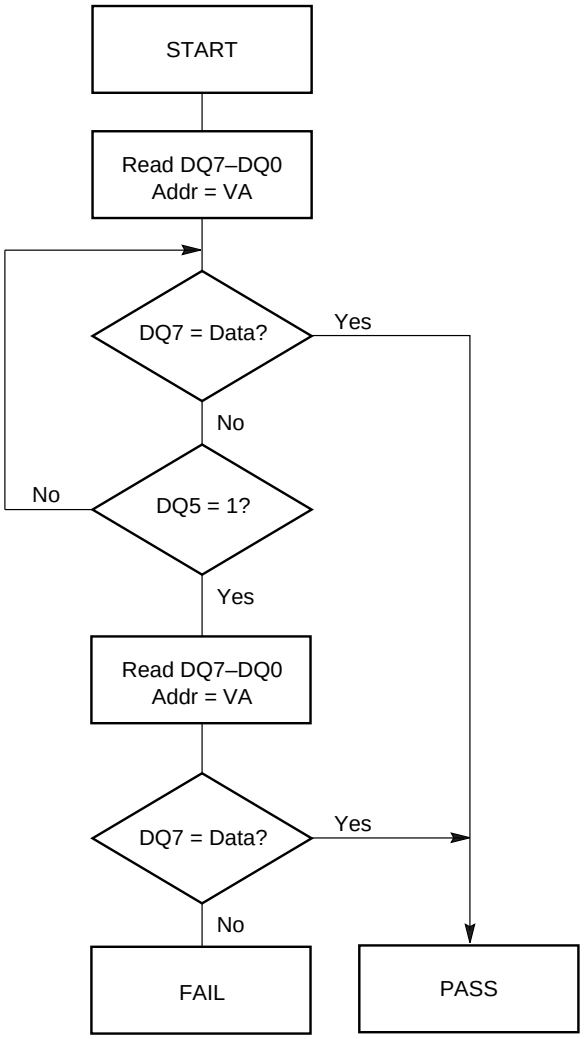
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 will appear on successive read cycles.

Table 11 shows the outputs for Data# Polling on DQ7. Figure 7 shows the Data# Polling algorithm. Figure 19 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 8. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or the device is in the erase-suspend-read mode.

Table 11 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

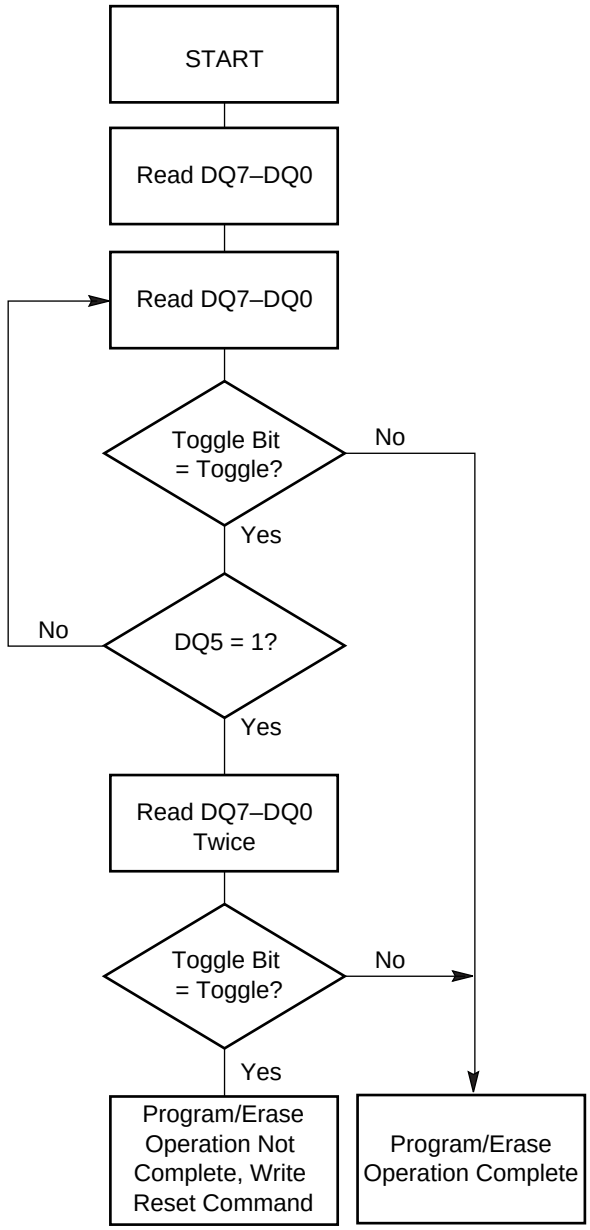
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 11 shows the outputs for Toggle Bit I on DQ6. Figure 8 shows the toggle bit algorithm. Figure 20 in the “AC Characteristics” section shows the toggle bit timing diagrams. Figure 21 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.



Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

Figure 9. Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 11 to compare outputs for DQ2 and DQ6.

Figure 8 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 20 shows the toggle bit timing diagram. Figure 21 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 8 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform

other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 8).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program, erase, or write-to-buffer time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

In all these cases, the system must write the reset command to return the device to the reading the array (or to erase-suspend-read if the device was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 11 shows the status of DQ3 relative to the other status bits.

DQ1: Write-to-Buffer Abort

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See Write Buffer

Table 11. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	DQ1	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A	0
Program Suspend Mode	Program-Suspend Read	Program-Suspended Sector	Invalid (not allowed)						1
		Non-Program Suspended Sector	Data						1
Erase Suspend Mode	Erase-Suspend Read	Erase-Suspended Sector	1	No toggle	0	N/A	Toggle	N/A	1
		Non-Erase Suspended Sector	Data						1
	Erase-Suspend-Program (Embedded Program)		DQ7#	Toggle	0	N/A	N/A	N/A	0
Write-to-Buffer	Busy (Note 3)		DQ7#	Toggle	0	N/A	N/A	0	0
	Abort (Note 4)		DQ7#	Toggle	0	N/A	N/A	1	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program, Embedded Erase, or Write-to-Buffer operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.*
4. *DQ1 switches to '1' when the device has aborted the write-to-buffer operation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

V_{IO} . . . . . –0.5 V to +4.0 V

A9, OE#, ACC, and RESET#
(Note 2) . . . . . –0.5 V to +12.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 9. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 10.*
2. *Minimum DC input voltage on pins A9, OE#, ACC, and RESET# is –0.5 V. During voltage transitions, A9, OE#, ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 9. Maximum DC input voltage on pin A9, OE#, ACC, and RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

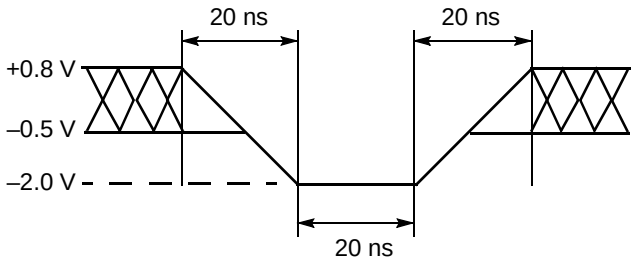


Figure 10. Maximum Negative Overshoot Waveform

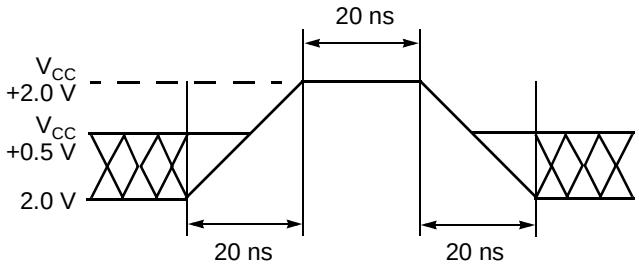


Figure 11. Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Supply Voltages

V_{CC} (regulated voltage range) . . . . . 3.0–3.6 V

V_{CC} (full voltage range) . . . . . 2.7–3.6 V

V_{IO} (Note 2) . . . . . 1.65–3.0 V

Notes:

1. *Operating ranges define those limits between which the functionality of the device is guaranteed.*
2. *See Ordering Information section for valid V_{CC}/V_{IO} range combinations. The I/Os cannot go to 3 V when V_{IO} = 1.8 V.*

DC CHARACTERISTICS

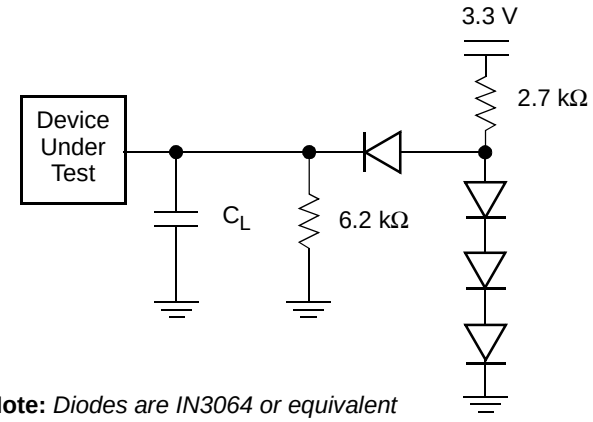
CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current (Note 1)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9, ACC Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LR}	Reset Leakage Current	$V_{CC} = V_{CC\ max}$; RESET# = 12.5 V				35	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}	5 MHz		15	20	mA
			1 MHz		15	20	
I_{CC2}	V_{CC} Initial Page Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}			30	50	mA
I_{CC3}	V_{CC} Intra-Page Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}			10	20	mA
I_{CC4}	V_{CC} Active Write Current (Notes 2, 3)	CE# = V_{IL}, OE# = V_{IH}			50	60	mA
I_{CC5}	V_{CC} Standby Current (Note 2)	CE#, RESET# = V_{CC} ± 0.3 V			1	5	µA
I_{CC6}	V_{CC} Reset Current (Note 2)	RESET# = V_{SS} ± 0.3 V			1	5	µA
I_{CC7}	Automatic Sleep Mode (Notes 2, 4)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V			1	5	µA
V_{IL1}	Input Low Voltage 1(Notes 5, 6)			–0.5		0.8	V
V_{IH1}	Input High Voltage 1 (Notes 5, 6)			0.7 x V_{CC}		V_{CC} + 0.5	V
V_{IL2}	Input Low Voltage 2 (Notes 5, 7)			–0.5		0.3 x V_{IO}	V
V_{IH2}	Input High Voltage 2 (Notes 5, 7)			0.7 x V_{IO}		V_{IO} + 0.5	V
V_{HH}	Voltage for ACC Program Acceleration	V_{CC} = 2.7 –3.6 V		11.5		12.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 2.7 –3.6 V		11.5		12.5	V
V_{OL}	Output Low Voltage (Note 9)	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min} = V_{IO}$				0.15 x V_{IO}	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min} = V_{IO}$		0.85 V_{IO}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min} = V_{IO}$		V_{IO}–0.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 8)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.*
5. *If $V_{IO} < V_{CC}$, maximum V_{IL} for CE# and DQ I/Os is 0.3 V_{IO}. If $V_{IO} < V_{CC}$, minimum V_{IH} for CE# and DQ I/Os is 0.7 V_{IO}. Maximum V_{IH} for these connections is V_{IO} + 0.3 V*
6. *V_{CC} voltage requirements.*
7. *V_{IO} voltage requirements. V_{CC} = 3 V and V_{IO} = 3 V or 1.8 V. When V_{IO} is at 1.8 V, I/Os cannot operate at 3 V.*
8. *Not 100% tested.*
9. *Includes RY/BY#.*

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

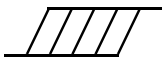
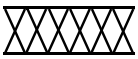
Figure 12. Test Setup

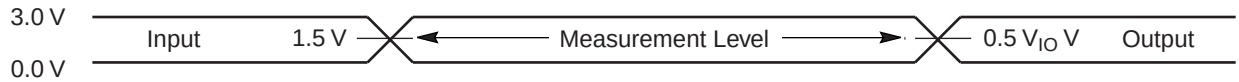
Table 12. Test Specifications

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–3.0	V
Input timing measurement reference levels (See Note)	1.5	V
Output timing measurement reference levels	0.5 V_{IO}	V

Note: *If $V_{IO} < V_{CC}$, the reference level is 0.5 V_{IO}.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)



Note: *If $V_{IO} < V_{CC}$, the input measurement reference level is 0.5 V_{IO}.*

Figure 13. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read-Only Operations

Parameter		Description		Test Setup		Speed Options						Unit
JEDEC	Std.					90R	101, 101R	112	112R	120	120R	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	90	100	110		120		ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	90	100	110		120		ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	90	100	110		120		ns
	t_{PACC}	Page Access Time			Max	25	30	30	40	30	40	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25	30	30	40	30	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	16						ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	16						ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0						ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0						ns
			Toggle and Data# Polling		Min	10						ns

Notes:

1. *Not 100% tested.*
2. *See Figure 11 and Table 12 for test specifications.*

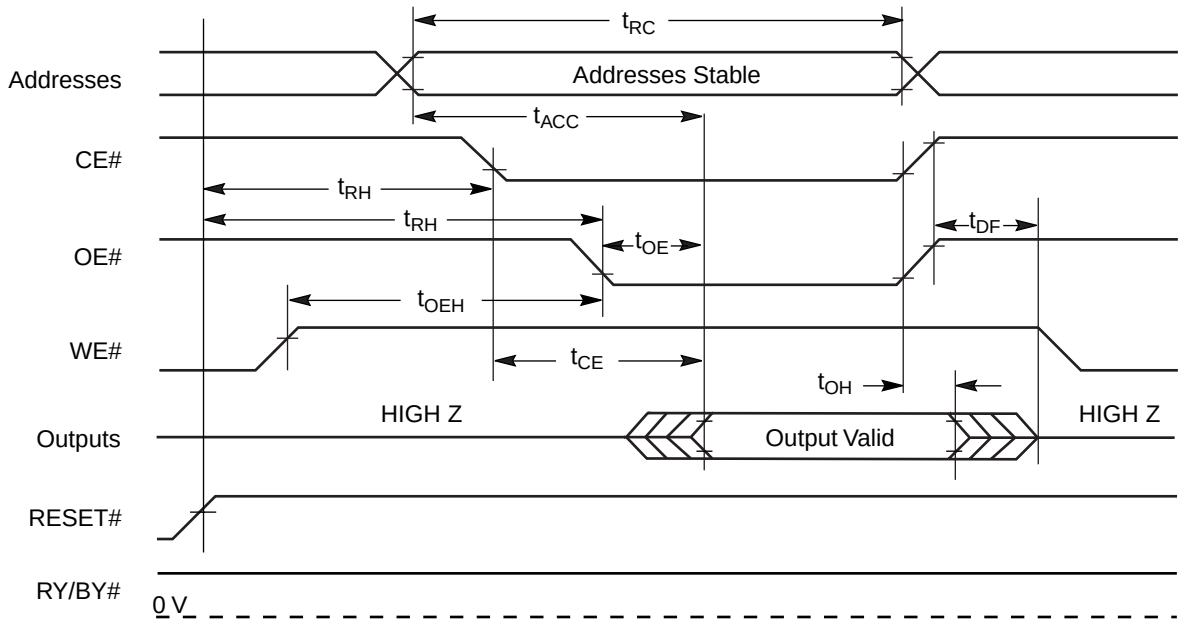
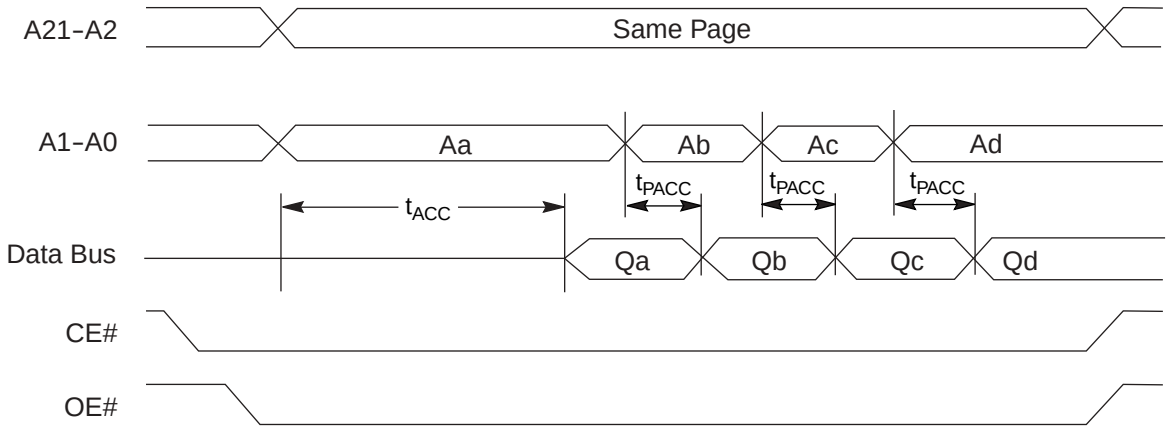


Figure 14. Read Operation Timings

AC CHARACTERISTICS



Note: *Toggle A0, A1, A2.*

Figure 15. Page Read Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: *Not 100% tested.*

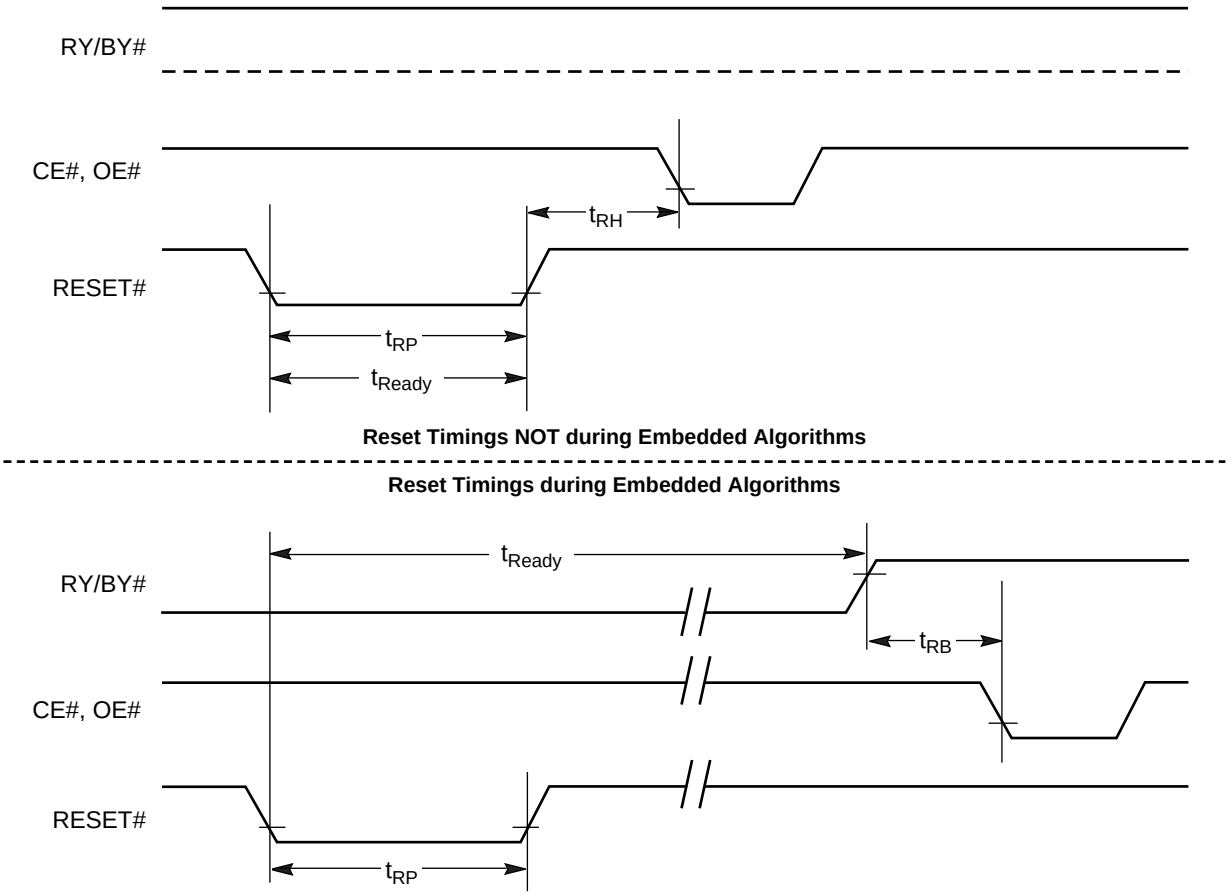


Figure 16. Reset Timings

AC CHARACTERISTICS

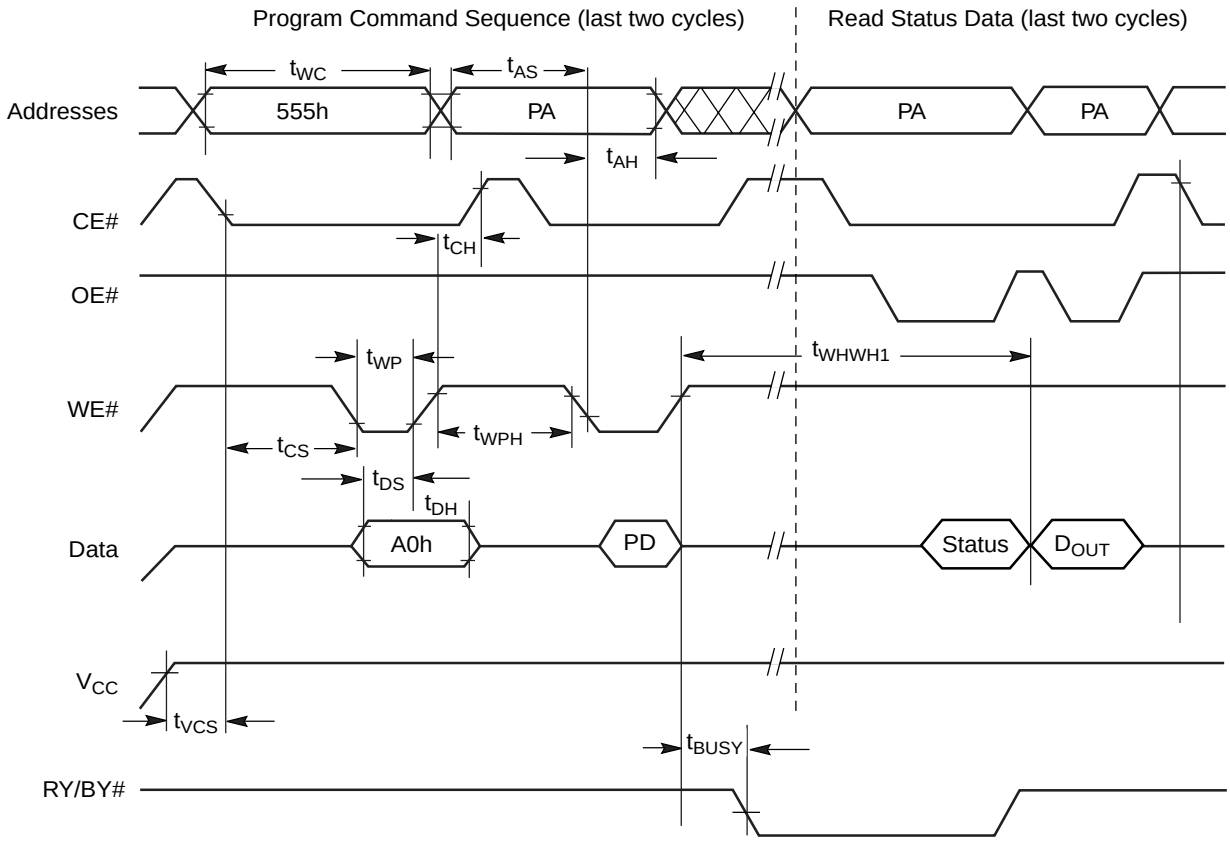
Erase and Program Operations

Parameter		Description		Speed Options				Unit
JEDEC	Std.			90R	101	112	120	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	90	100	110	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling	Min	15				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45				ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling	Min	0				ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	45				ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OEPH}	Output Enable High during toggle bit polling	Min	20				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35				ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	30				ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)	Typ	352				µs
		Effective Write Buffer Program Operation, Per Word (Notes 2, 4)	Typ	22				µs
		Accelerated Effective Write Buffer Program Operation, Per Word (Notes 2, 4)	Typ	17.6				µs
		Single Word Program Operation (Note 2, 5)	Typ	100				µs
		Accelerated Single Word Programming Operation (Note 2, 5)	Typ	90				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5				sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)	Min	250				ns
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50				µs
	t_{RB}	Write Recovery Time from RY/BY#	Min	0				ns
	t_{BUSY}	WE# High to RY/BY# Low	Min	90	100	110	120	ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*
3. *For 1–16 words programmed.*
4. *Effective write buffer specification is based upon a 16-word write buffer operation.*
5. *Word programming specification is based upon a single word programming operation not utilizing the write buffer.*
6. *AC specifications listed are tested with $V_{IO} = V_{CC}$. Contact AMD for information on AC operation with $V_{IO} \neq V_{CC}$.*

AC CHARACTERISTICS



Note: *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*

Figure 17. Program Operation Timings

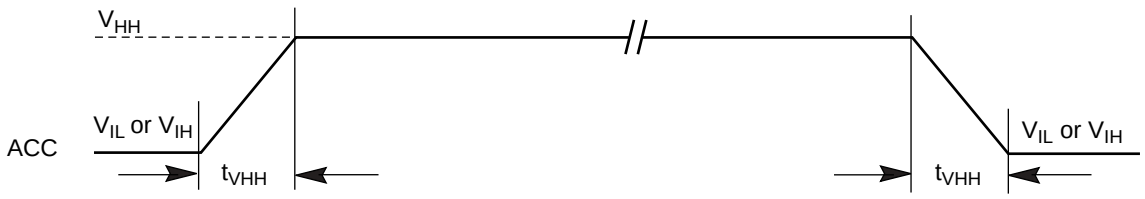
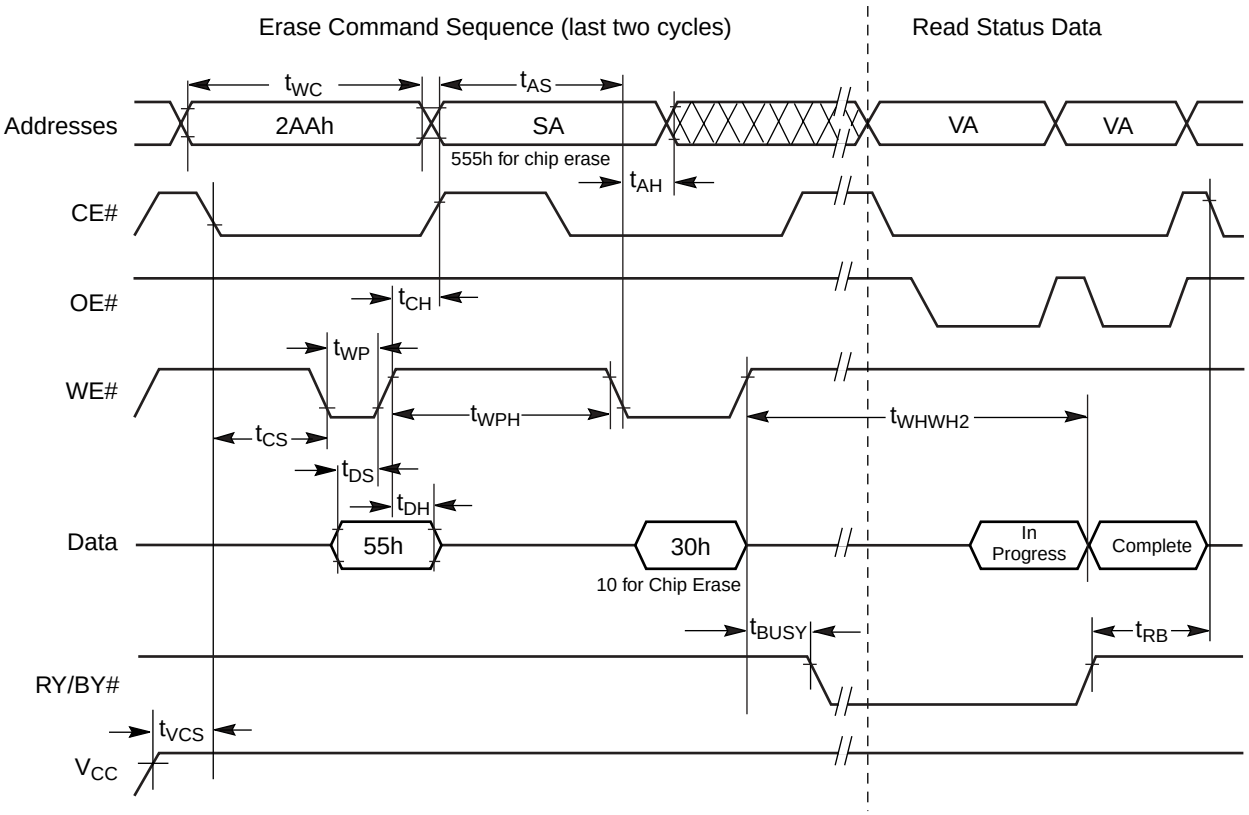


Figure 18. Accelerated Program Timing Diagram

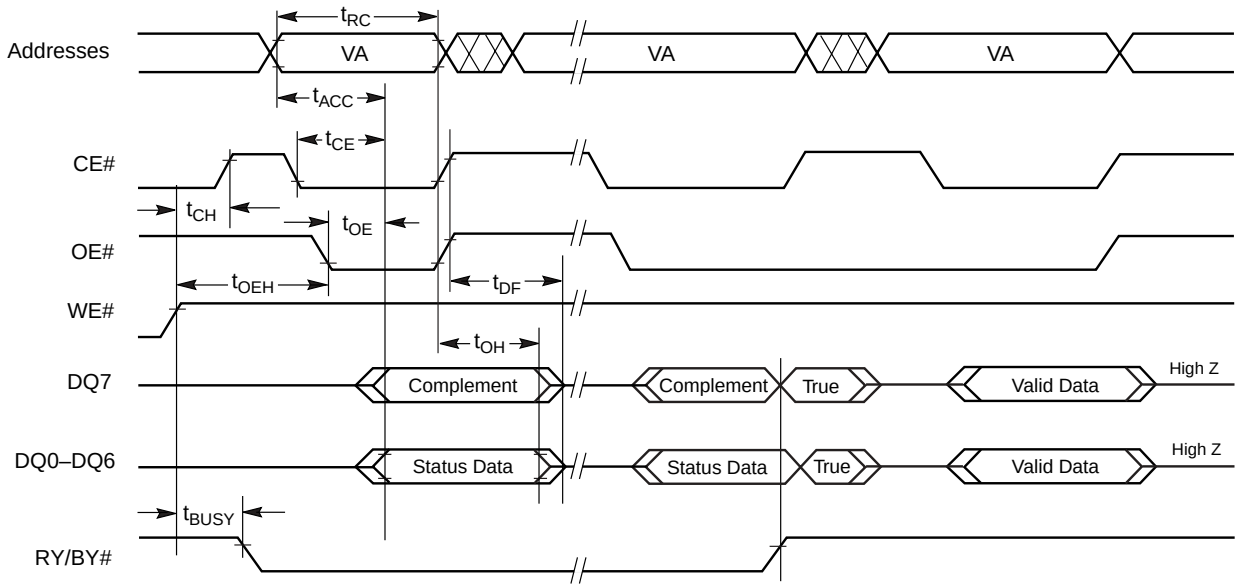
AC CHARACTERISTICS



Note:
SA= sector address (for Sector Erase), VA= Valid Address for reading status data (see "Write Operation Status").

Figure 19. Chip/Sector Erase Operation Timings

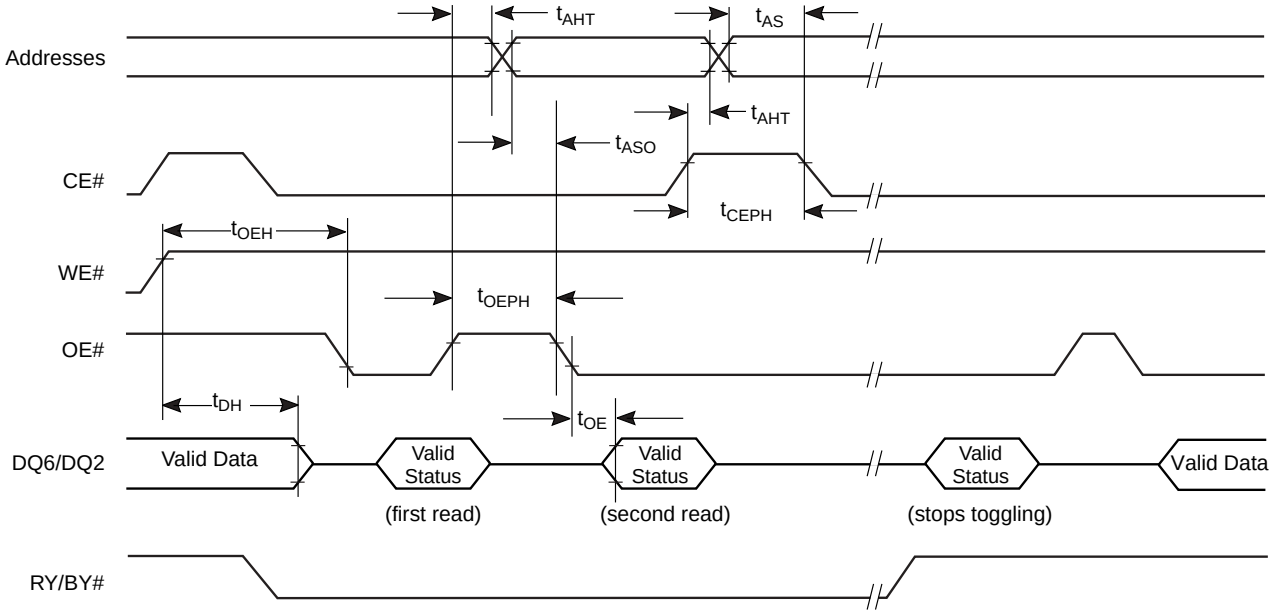
AC CHARACTERISTICS



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

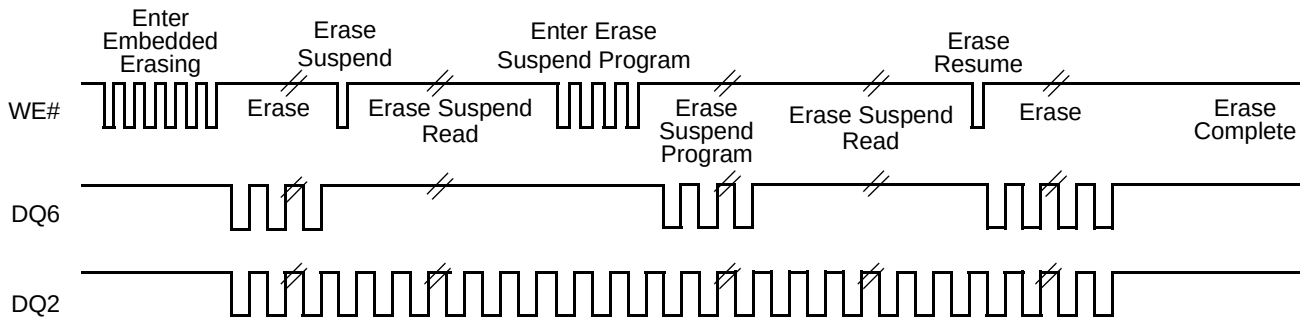
Figure 20. Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 21. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 22. DQ2 vs. DQ6

AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter					
JEDEC	Std	Description		All Speed Options	Unit
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Group Unprotect	Min	4	µs

Note: *Not 100% tested.*

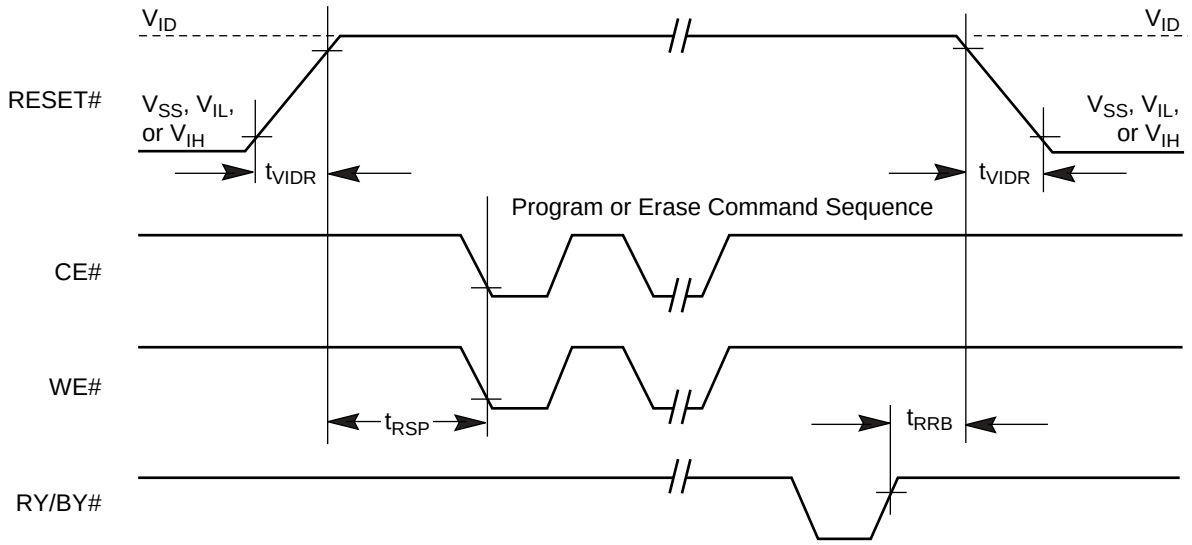
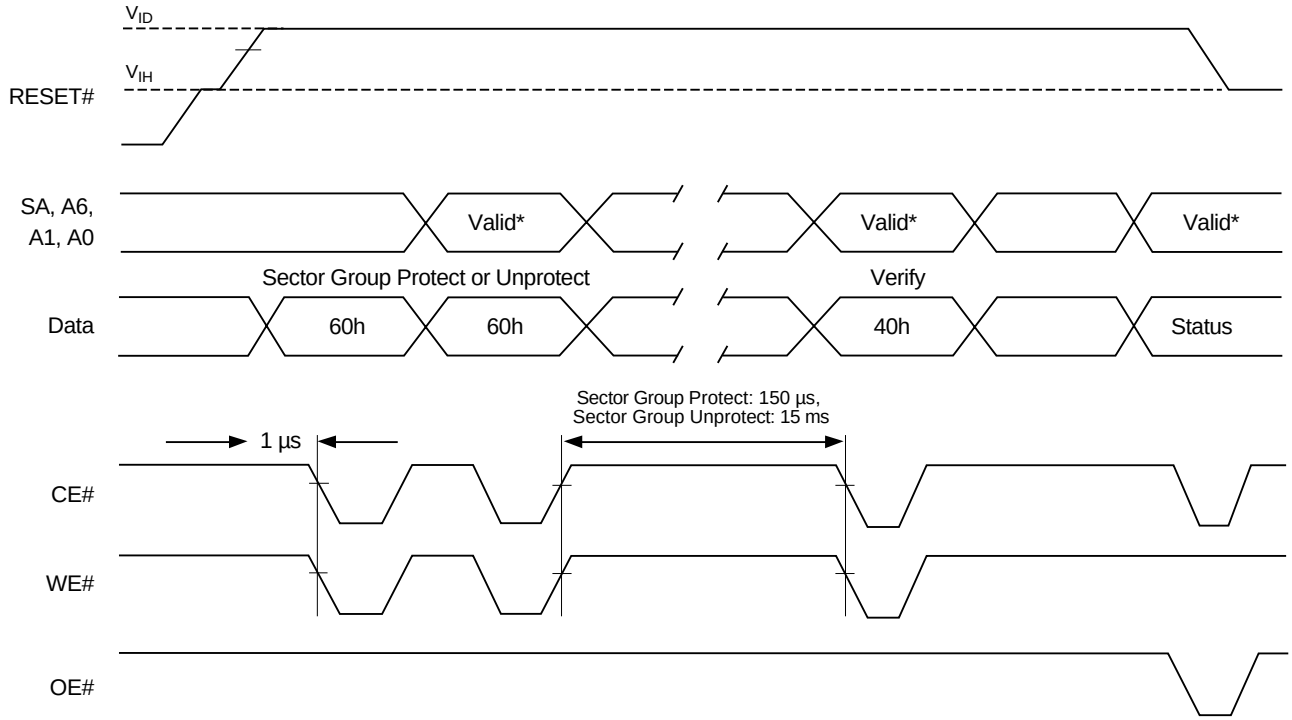


Figure 23. Temporary Sector Group Unprotect Timing Diagram

AC CHARACTERISTICS



* *For sector group protect, A6:A0 = 0xx0010. For sector group unprotect, A6:A0 = 1xx0010.*

Figure 24. Sector Group Protect and Unprotect Timing Diagram

AC CHARACTERISTICS

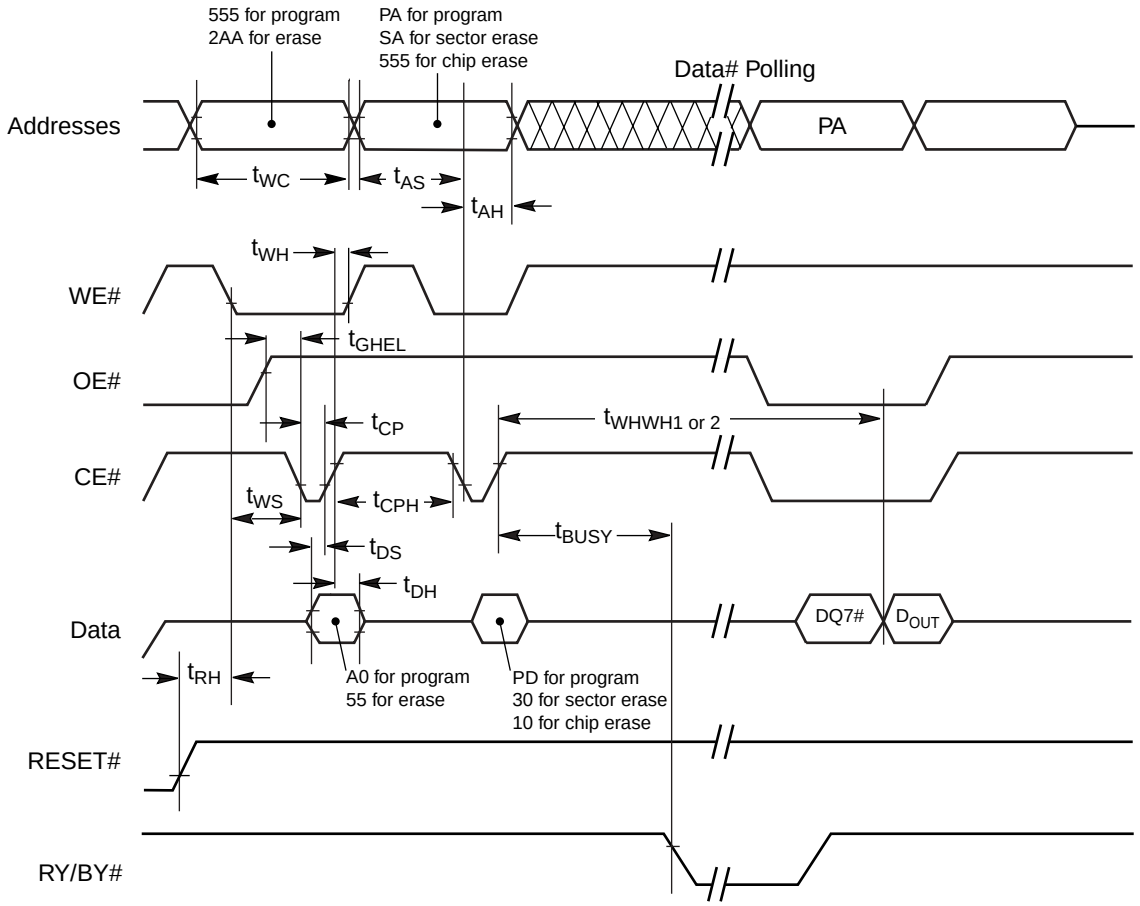
Alternate CE# Controlled Erase and Program Operations

Parameter		Description		Speed Options				Unit
JEDEC	Std.			90R	101, 101R	112, 112R	120, 120R	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	90	100	110	120	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45				ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	45				ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	45				ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	30				ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)	Typ	352				µs
		Effective Write Buffer Program Operation, Per Word (Notes 2, 4)	Typ	22				µs
		Accelerated Effective Write Buffer Program Operation, Per Word (Notes 2, 4)	Typ	17.6				µs
		Single Word Program (Note 2, 5)	Typ	100				µs
		Accelerated Single Word Programming Operation (Note 2, 5)	Typ	90				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5				sec
	t_{RH}	RESET # High Time Before Write (Note 1)	Min	50				ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information. Write buffer program is typical per word.*
3. *For 1–16 words programmed.*
4. *Effective write buffer specification is based upon a 16-word write buffer operation.*
5. *Word programming specification is based upon a single word programming operation not utilizing the write buffer.*
6. *AC specifications listed are tested with $V_{IO} = V_{CC}$. Contact AMD for information on AC operation with $V_{IO} \neq V_{CC}$.*

AC CHARACTERISTICS



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*

Figure 25. Alternate CE# Controlled Write (Erase/Program) Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	15	sec	
Chip Erase Time		32	128	sec	
Single Word/Byte Program Time (Note 3)	Byte	100	**TBD**	µs	
	Word	100	**TBD**	µs	
Accelerated Single Word/Byte Program Time (Note 3)	Byte	90	**TBD**	µs	
	Word	90	**TBD**	µs	
Total Write Buffer Program Time (Note 4)		352	**TBD**	µs	
Effective Write Buffer Program Time (Note 5)	Per Byte	11	**TBD**	µs	
	Per Word	22	**TBD**	µs	
Total Accelerated Effective Write Buffer Program Time (Note 4)		282	**TBD**	µs	
Effective Accelerated Write Buffer PRogram Time (Note 4)	Byte	8.8	**TBD**	µs	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}. Programming specifications assume that all bits are programmed to 00h.*
2. *Maximum values are measured at V_{CC} = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.*
3. *Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.*
4. *For 1-16 words or 1-32 bytes programmed ina single write buffer programming operation.*
5. *Effective write buffer specification is calculated on a per-word/per-byte basis for a 16-word/32-byte write buffer operation.*
6. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
7. *System-level overhead is the time required to execute the command sequence(s) for the program command. See Tables 12 and 11 for further information on command definitions.*
8. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.*

TSOP PIN AND FINE-PITCH BGA PACKAGE CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup		Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TSOP	6	7.5	pF
			Fine-pitch BGA	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TSOP	8.5	12	pF
			Fine-pitch BGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TSOP	7.5	9	pF
			Fine-pitch BGA	3.9	4.7	pF

Notes:

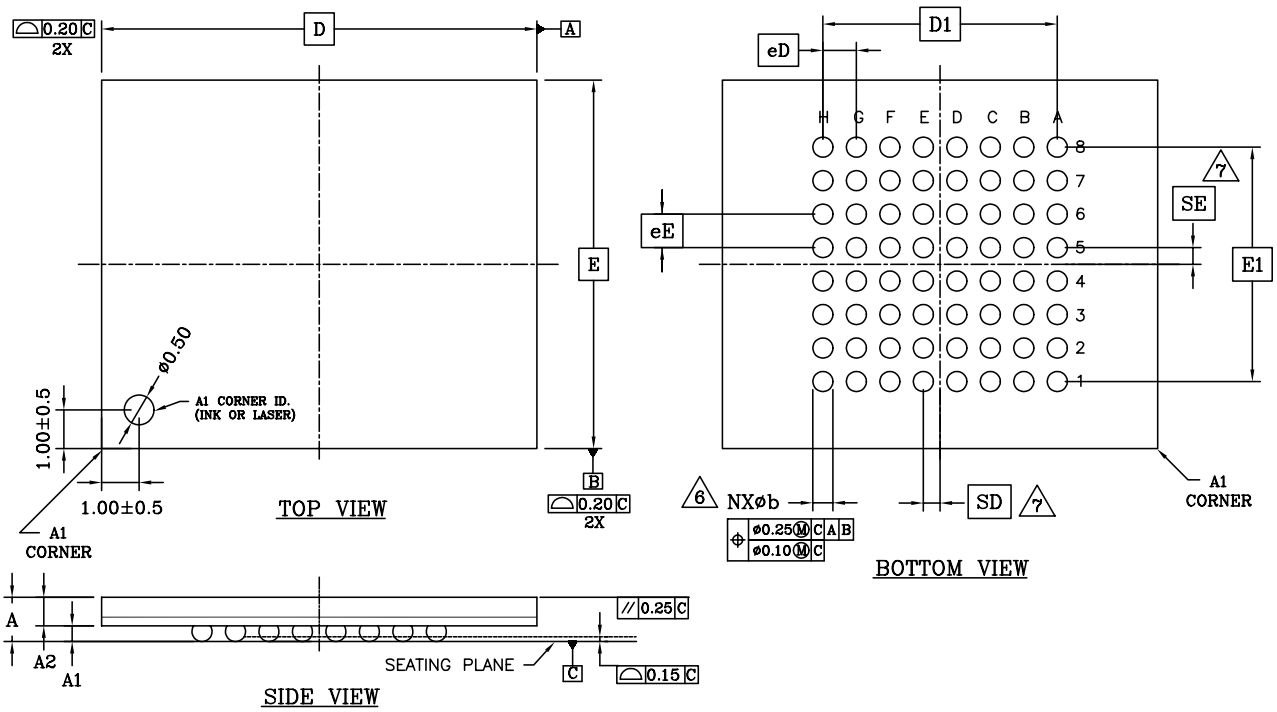
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS

LAA064—64-Ball Fortified Ball Grid Array (FBGA) 13 x 11 mm Package



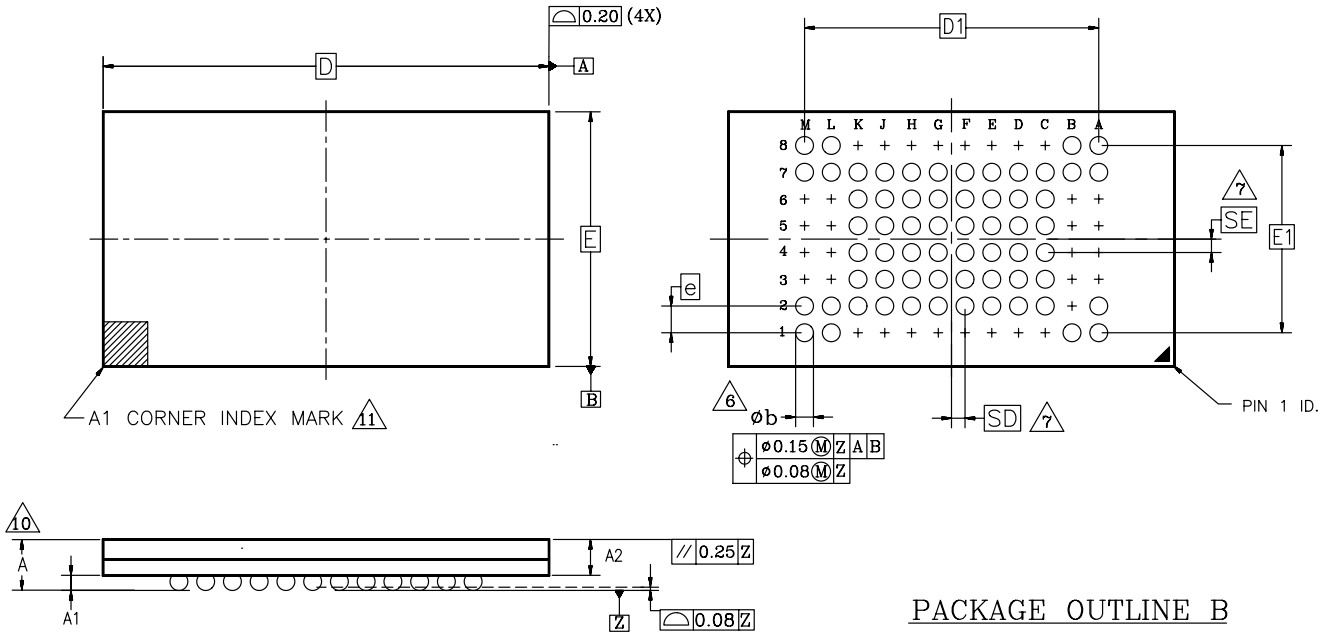
PACKAGE	LAA 064			
JEDEC	N/A			
	13.00x11.00 mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	NOTE
A	–	–	1.40	PROFILE HEIGHT
A1	0.40	–	–	STANDOFF
A2	0.60	–	–	BODY THICKNESS
D	13.00 BSC.			BODY SIZE
E	11.00 BSC.			BODY SIZE
D1	7.00 BSC.			MATRIX FOOTPRINT
E1	7.00 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
N	64			BALL COUNT
øb	0.50	0.60	0.70	BALL DIAMETER
eD	1.00 BSC.			BALL PITCH – D DIRECTION
eE	1.00 BSC.			BALL PITCH – E DIRECTION
SD/SE	0.50 BSC.			SOLDER BALL PLACEMENT
	A1–A8, K1–K8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M–1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM "C".
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

PHYSICAL DIMENSIONS

FBE063—63-Ball Fine-Pitch Ball Grid Array (FBGA) 12 x 11 mm Package



PACKAGE OUTLINE B

Dwg rev AF; 10/99

PACKAGE	xFBE 063			
JEDEC	N/A			
	12.00mmx11.00mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	OVERALL THICKNESS
A1	0.20	—	—	BALL HEIGHT
A2	0.84	—	0.94	BODY THICKNESS
D	12.00 BSC			BODY SIZE
E	11.00 BSC			BODY SIZE
D1	8.80 BSC			BALL FOOTPRINT
E1	5.60 BSC			BALL FOOTPRINT
MD	12			ROW MATRIX SIZE D DIRECTION
ME	8			ROW MATRIX SIZE E DIRECTION
N	63			TOTAL BALL COUNT
b	0.25	0.30	0.35	BALL DIAMETER
e	0.80 BSC			BALL PITCH
SD/SE	0.40 BSC			SOLDER BALL PLACEMENT
	A3–A6,B2–B6 L3–L6, M3–M6 C1–K1,C8–K8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE MD x ME.

6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM Z.

7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000 WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" IN THE PACKAGE DRAWING INDICATE THE THEORETICAL CENTER OF DEPOPULATED BALLS.

10 FOR PACKAGE THICKNESS A IS THE CONTROLING DIMENSION.

11 A1 CORNER TO BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKINGS INDENTION OR OTHER MEANS.

REVISION SUMMARY

Revision A (August 3, 2001)

Initial release as abbreviated Advance Information data sheet.

Revision A+1 (September 12, 2001)

Global

Changed description of chip-scale package from 63-ball FBGA to 64-ball Fortified BGA.

Ordering Information

Changed package part number designation from WH to PC.

Physical Dimensions

Added the TS056 and LAA064 packages.

Revision A+2 (October 3, 2001)

Global

Added information for WP# protected devices (LV640MH/L). Clarified V_{CC} and V_{IO} ranges.

Connection Diagrams

Changed RFU (reserved for future use) to NC (no connection). Added 63-ball FBGA drawing.

Ordering Information

Added H and L valid combinations for WP# protected devices. Changed voltage operating range for 90 ns device.

Revision B (March 19, 2002)

Global

Expanded data sheet to full specification version. Starting with this revision, the data sheet will only contain specifications for the Am29LV640MU part number. For Am29LV640MH/L part number specifications, refer to publication number 26191.

Revision B+1 (April 26, 2002)

Global

Deleted references to word mode.

MirrorBit 64 Mbit Device Family

Deleted Am29LV641MT/B.

Figure 2, In-System Sector Group Protect/Unprotect Algorithms

Modified to show A2, A3 address requirements.

Sector Protection/Unprotection

Deleted references to alternate method of sector protection.

Autoselect Command

Substituted text with ID code table for easier reference.

Table 10, Command Definitions

Combined Notes 4 and 5 from Revision B. Corrected number of cycles indicated for Write-to-Buffer and Autoselect Device ID command sequences.

Revision B+2 (August 5, 2002)

MIRRORBIT 64 MBIT Device Family

Added 64 Fortified BGA to LV640MU device.

Alternate CE# Controlled Erase and Program Operations

Added t_{RH} parameter to table.

Erase and Program Operations

Added t_{BUSY} parameter to table.

Figure 16. Program Operation Timings

Added RY/BY# to waveform.

TSOP and BGA PIN Capacitance

Added the FBGA package.

Program Suspend/Program Resume Command Sequence

Changed 15 µs typical to maximum and added 5 µs typical.

Erase Suspend/Erase Resume Commands

Changed typical from 20 µs to 5 µs and added a maximum of 20 µs.

Revision B+3 (September 10, 2002)

Product Selector Guide

Added Note 2.

Ordering Information

Added Note 1.

Connection Diagram

Deleted A-1 from Pin G7.

Sector Erase Command Sequence

Deleted statement that describes the outcome of when the Embedded Erase operation is in progress.

Revision B+4 (February 16, 2003)

Distinctive Characteristics

Corrected performance characteristics.

Product Selector Guide

Added note 2.

Ordering Information

Corrected Valid Combination to reflect speed option changes.

Added Note.

AC Characteristics

Removed 90R speed option.

Added Note

Input values in the $t_{WHWH}1$ and $t_{WHWH}2$ parameters in the Erase and Program Options table that were previously TBD. Also added notes 5 and 6.

Input values in the $t_{WHWH}1$ and $t_{WHWH}2$ parameters in the Alternate CE# Controlled Erase and Program Options table that were previously TBD. Also added notes 5 and 6.

Erase and Programming Performance

Input values into table that were previously TBD.

Added note 4.

Revision C (March 11, 2003)

Product Selector Guide and AC Characteristics, Read Only Operations Table

Added seperate values for the 112 and 120 ns speed options in the Page access times and OE# access time.

Ordering Information

Removed note from sector architecture.

Table 3. Autoselect Codes, (High Voltage Method)

Updated DQ15 to DQ0 for Sector Protection Verification and SecSi Sector Indicator Bit.

SecSi (Secured Silicon) Sector Flash Memory Region

Updated second bullet in Customer Lockable section.

Added Figure 3.

Command Definitions

Updated first paragraph.

Table 3. Autoselect Codes, (High Voltage Method) Table 10. Command Definitions

Corrected Note #10 to read 98h for factory locked and 18h for not factory locked.

Operating Ranges

Added a V_{CC} for regulated voltage and added standard voltage range title for remaining $V_{CC.}$

CMOS Compatible

Added I_{LR} parameter symbol.

Updated I_{CC} parameter symbol.

Revision C+1 (June 12, 2003)

Ordering Information

Added 90R speed grade, modified note.

Erase and Programming Performance

Modified table, inserted values for Typical.

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