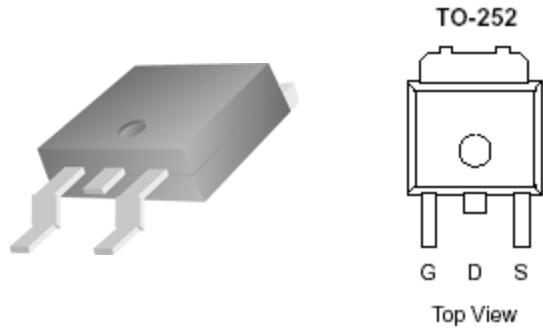


N-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature TO-252 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} m(Ω)	I _D (A)
20	29 @ V _{GS} = 4.5V	34
	43 @ V _{GS} = 2.5V	22



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V _{DS}	20	V
Gate-Source Voltage		V _{GS}	±12	
Continuous Drain Current ^a	T _C =25°C	I _D	34	A
Pulsed Drain Current ^b		I _{DM}	40	
Continuous Source Current (Diode Conduction) ^a		I _S	30	A
Power Dissipation ^a	T _C =25°C	P _D	50.0	W
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 175	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	R _{θJA}	50	°C/W
Maximum Junction-to-Case	R _{θJC}	3.0	°C/W

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

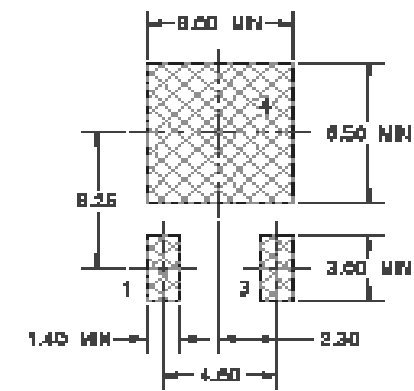
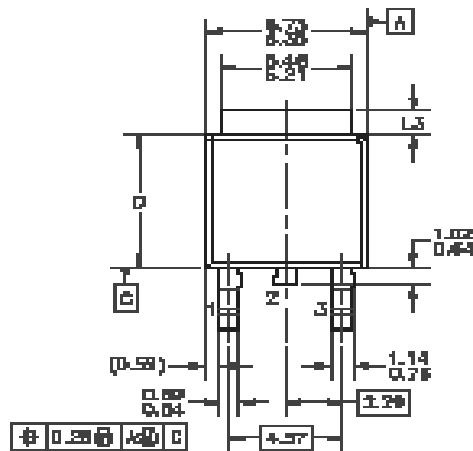
SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.7			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
		$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	34			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 17 \text{ A}$			29	m Ω
		$V_{GS} = 2.5 \text{ V}, I_D = 11 \text{ A}$			43	
Forward Transconductance ^A	g_{fs}	$V_{DS} = 10 \text{ V}, I_D = 17 \text{ A}$		22		S
Diode Forward Voltage	V_{SD}	$I_S = 34 \text{ A}, V_{GS} = 0 \text{ V}$		1.1		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 11 \text{ A}$		13.4		nC
Gate-Source Charge	Q_{gs}			0.9		
Gate-Drain Charge	Q_{gd}			2.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10 \text{ V}, R_L = 25 \Omega, I_D = 34 \text{ A},$ $V_{GEN} = 10 \text{ V}$		16		nS
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(off)}$			23		
Fall-Time	t_f			3		

Notes

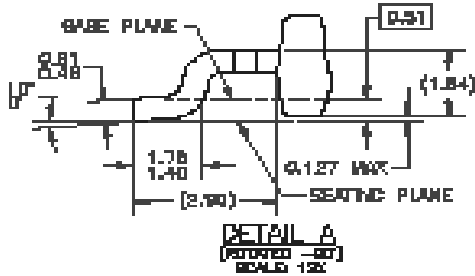
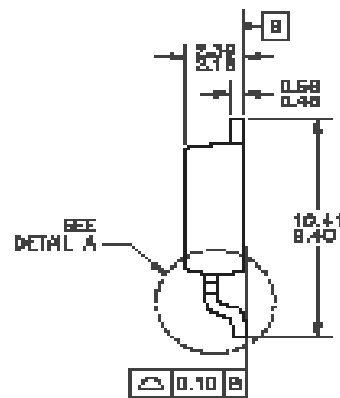
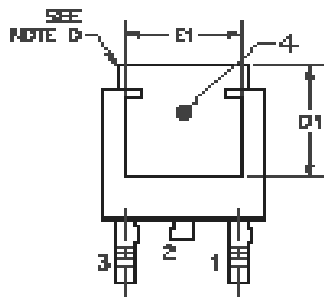
- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-262, ISSUE C, VARIATION AA, 30 DE, DATED NOV. 1999.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.04M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3,D,E1 AND 1 TABLE:

	OPTION A1	OPTION A2
L3	0.68-1.27	1.62-2.52
D	0.92-0.92	0.43-0.43
E1	4.32 MIN	3.81 MIN
D1	3.41 MIN	4.37 MIN