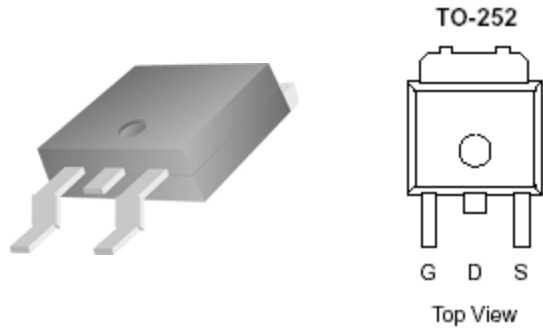


**N-Channel 20-V (D-S) MOSFET**

These miniature surface mount MOSFETs utilize High Cell Density process. Low  $r_{DS(on)}$  assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low  $r_{DS(on)}$  Provides Higher Efficiency and Extends Battery Life
- Miniature TO-252 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ m( $\Omega$ )	$I_D$ (A)
20	59 @ $V_{GS} = 4.5V$	24
	88 @ $V_{GS} = 2.5V$	20



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		$V_{DS}$	20	V
Gate-Source Voltage		$V_{GS}$	$\pm 12$	
Continuous Drain Current <sup>a</sup>	$T_C = 25^\circ C$	$I_D$	24	A
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	40	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	30	A
Power Dissipation <sup>a</sup>	$T_C = 25^\circ C$	$P_D$	50	W
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 175	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	50	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

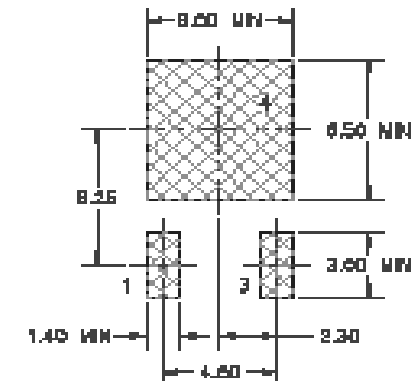
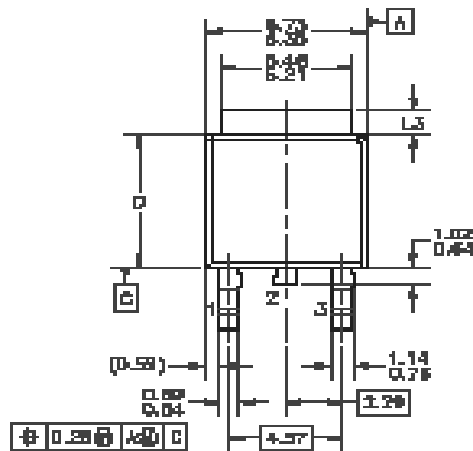
SPECIFICATIONS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
<b>Static</b>						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.7			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
		$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current <sup>A</sup>	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	34			A
Drain-Source On-Resistance <sup>A</sup>	$r_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 12 \text{ A}$			59	m $\Omega$
		$V_{GS} = 2.5 \text{ V}, I_D = 10 \text{ A}$			88	
Forward Transconductance <sup>A</sup>	$g_{fs}$	$V_{DS} = 10 \text{ V}, I_D = 12 \text{ A}$		22		S
Diode Forward Voltage	$V_{SD}$	$I_S = 24 \text{ A}, V_{GS} = 0 \text{ V}$		1.1		V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 10 \text{ A}$		7.5		nC
Gate-Source Charge	$Q_{gs}$			0.6		
Gate-Drain Charge	$Q_{gd}$			1.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10 \text{ V}, R_L = 25 \Omega, I_D = 24 \text{ A},$ $V_{GEN} = 10 \text{ V}$		16		nS
Rise Time	$t_r$			5		
Turn-Off Delay Time	$t_{d(off)}$			23		
Fall-Time	$t_f$			3		

## Notes

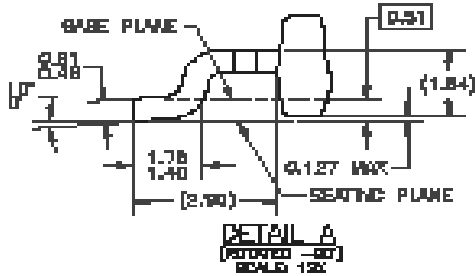
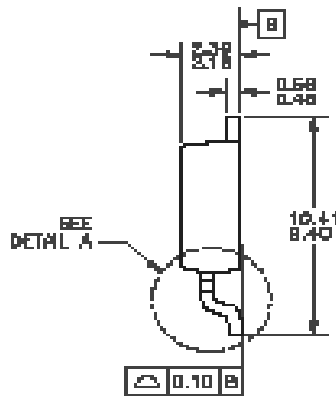
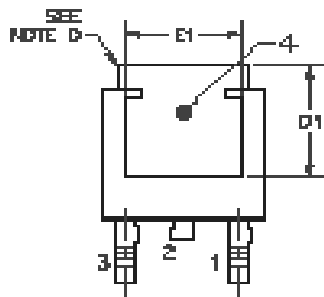
- Pulse test:  $PW \leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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# Package Information



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) THIS PACKAGE CONFORMS TO JEDEC, TO-262, ISSUE C, VARIATION AA, 30 DE, DATED NOV. 1999.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.00M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.68-1.27	1.62-2.52
D	0.92-0.92	0.43-0.49
E1	4.32 MIN	3.81 MIN
D1	3.41 MIN	4.57 MIN