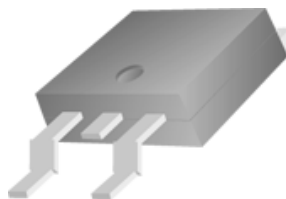


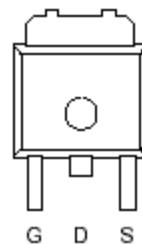
N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



TO-252



Top View

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_C = 25^\circ\text{C}$	I_D	24	A
Pulsed Drain Current ^b		I_{DM}	75	
Continuous Source Current (Diode Conduction) ^a		I_S	30	A
Power Dissipation ^a	$T_C = 25^\circ\text{C}$	P_D	50	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ\text{C}/\text{W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1		2.3	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
		$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	34			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$			59	m Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$			88	
Forward Transconductance ^A	g_s	$V_{DS} = 15 \text{ V}, I_D = 12 \text{ A}$		22		S
Diode Forward Voltage	V_{SD}	$I_S = 24 \text{ A}, V_{GS} = 0 \text{ V}$		1.1		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 10 \text{ A}$		2.2		nC
Gate-Source Charge	Q_{gs}			0.5		
Gate-Drain Charge	Q_{gd}			0.8		
Input Capacitance	C_{iss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1\text{MHz}$		720		pF
Output Capacitance	C_{oss}			165		
Reverse Transfer Capacitance	C_{rss}			60		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25 \text{ V}, R_L = 25 \Omega, I_D = 24 \text{ A},$ $V_{GEN} = 10 \text{ V}$		16		nS
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(off)}$			23		
Fall-Time	t_f			3		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Typical Electrical Characteristics (N-Channel)

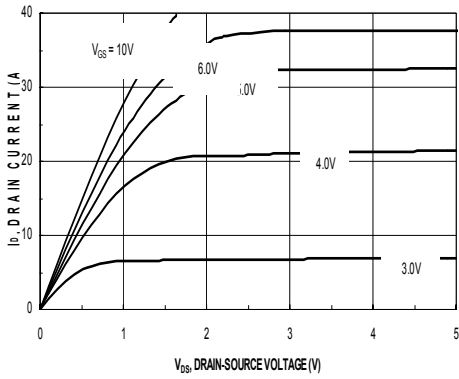


Figure 1. On-Region Characteristics

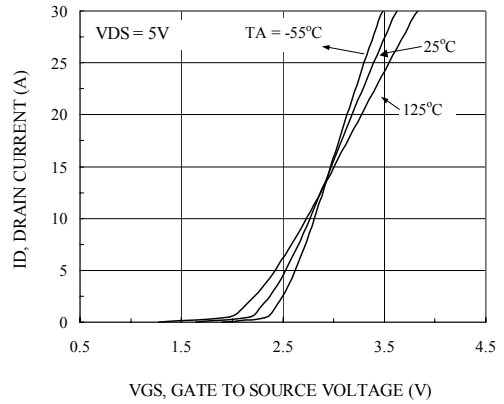


Figure 2. Body Diode Forward Voltage Variation with Source Current and Temperature

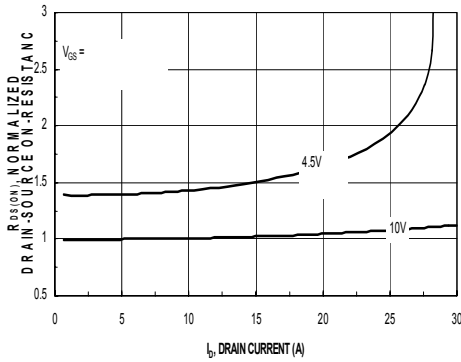


Figure 3. On Resistance Vs Vgs Voltage

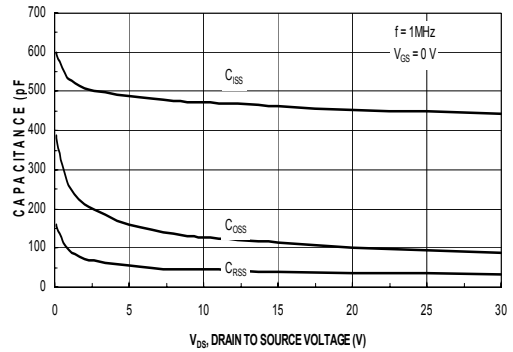


Figure 4. Capacitance Characteristics

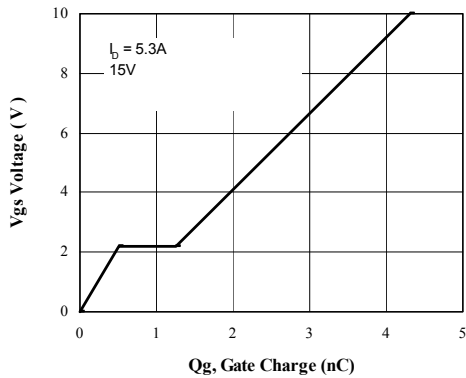


Figure 5. Gate Charge Characteristics

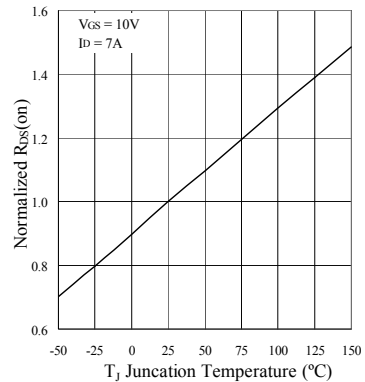


Figure 6. On-Resistance Variation with Temperature

Typical Electrical Characteristics (N-Channel)

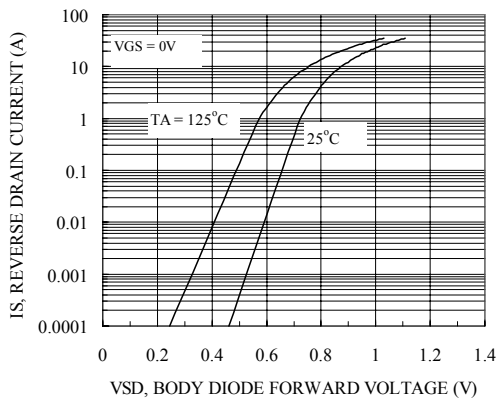


Figure 7. Transfer Characteristics

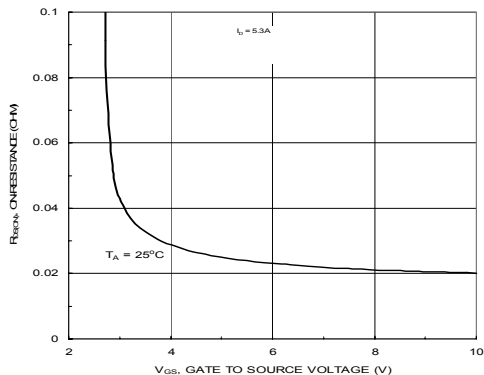


Figure 8. On-Resistance with Gate to Source Voltage

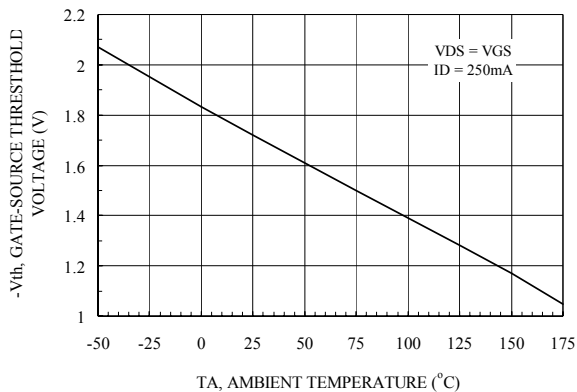


Figure 9. V_{th} Gate to Source Voltage Vs Temperature

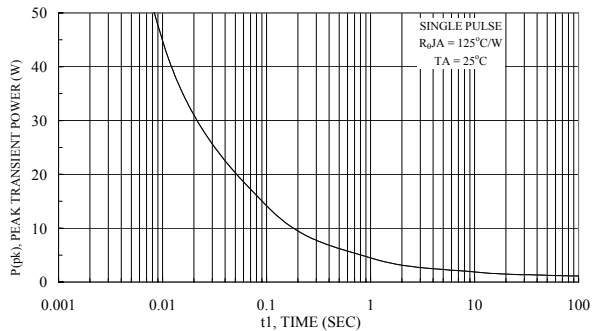


Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

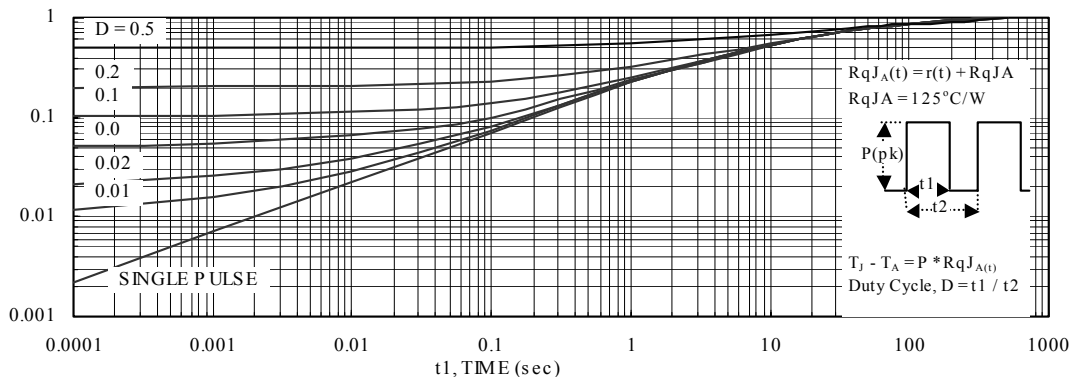
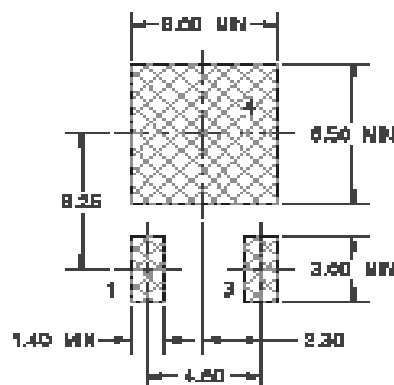
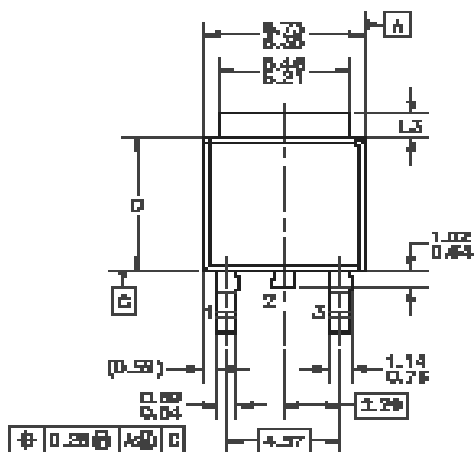
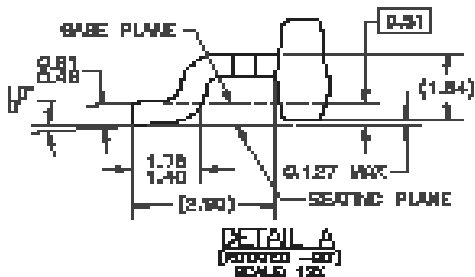
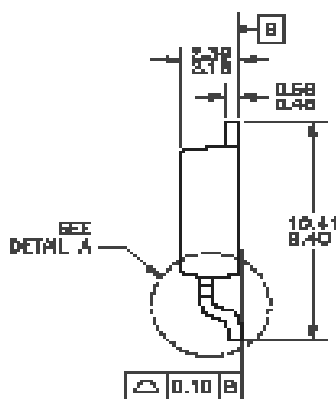
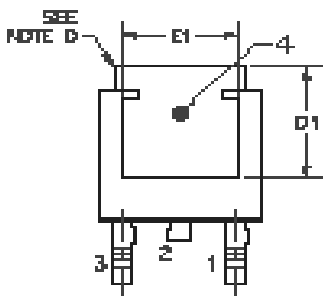


Figure 11. Transient Thermal Response Curve

Package Information



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-262, ISSUE C, VARIATION AA, 31 DEJ, DATED NOV. 1989.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.00M-1984.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3, D, E1 & D1 TABLE:

	SECTION AA	SECTION AB
L3	0.68-1.27	1.62-2.54
D	0.97-0.99	0.93-0.99
E1	4.32 MIN	3.81 MIN
D1	3.81 MIN	4.37 MIN