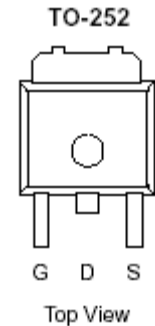
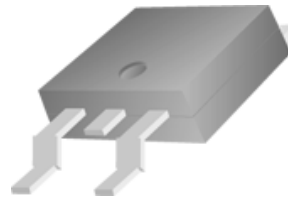


N-Channel 100-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
100	50 @ $V_{GS} = 10V$	26
	59 @ $V_{GS} = 4.5V$	24

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	$T_C = 25^\circ C$ I_D	20	A
Pulsed Drain Current ^b	I_{DM}	36	
Continuous Source Current (Diode Conduction) ^a	I_S	30	A
Power Dissipation ^a	$T_C = 25^\circ C$ P_D	50	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ C/W$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

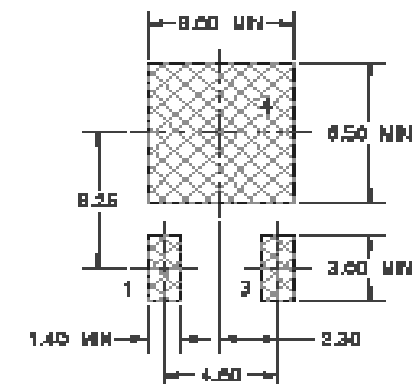
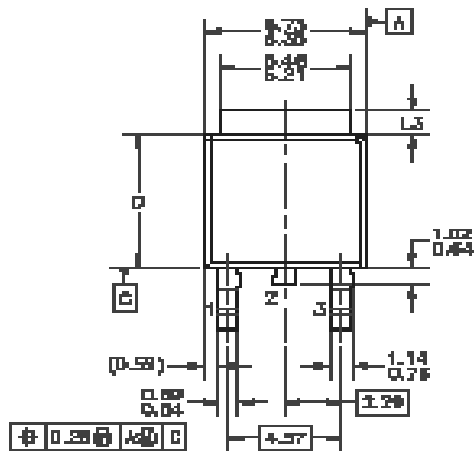
SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 uA	1.0			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	uA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 55°C			25	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	34			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 9.2 A			50	mΩ
		V _{GS} = 4.5 V, I _D = 6.1 A			59	
Forward Transconductance ^A	g _{fs}	V _{DS} = 40 V, I _D = 5.5 A		4.4		S
Diode Forward Voltage	V _{SD}	I _S = 9 A, V _{GS} = 0 V		1.1		V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 25 V, V _{GS} = 10 V, I _D = 9 A		25		nC
Gate-Source Charge	Q _{gs}			5		
Gate-Drain Charge	Q _{gd}			19		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 100 V, R _L = 25 Ω, I _D = 9 A, V _{GEN} = 10 V		9		nS
Rise Time	t _r			15		
Turn-Off Delay Time	t _{d(off)}			45		
Fall-Time	t _f			39		

Notes

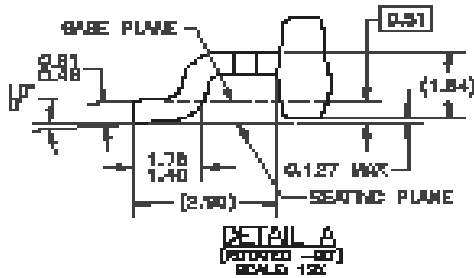
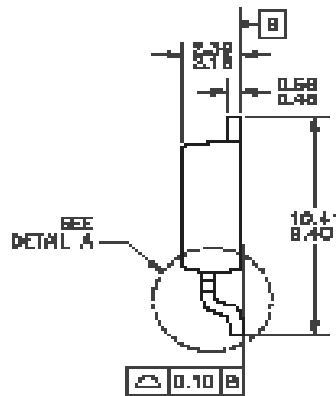
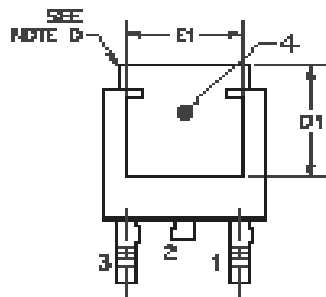
- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

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Package Information



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-262, ISSUE C, VARIATION AA, 31 DEJ, DATED NOV. 1999.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.00M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3, D, E1 & D1 TABLE:

	OPTION A0	OPTION A0
L3	0.68-1.27	1.02-2.54
D	0.97-0.99	0.93-0.99
E1	4.32 MIN	3.81 MIN
D1	3.41 MIN	4.37 MIN