

P-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSOP-6 saves board space
- Fast switching speed
- High performance trench technology

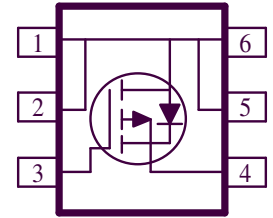
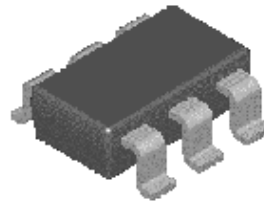
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.042 @ $V_{GS} = -4.5V$	-5.7
	0.057 @ $V_{GS} = -2.5V$	-4.9



RoHS COMPLIANT HALOGEN FREE



Protected



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ^a	I_D	$T_A=25^\circ C$	-5.7
		$T_A=70^\circ C$	-4.7
Pulsed Drain Current ^b	I_{DM}	± 20	A
Continuous Source Current (Diode Conduction) ^a	I_S	-1.7	A
Power Dissipation ^a	P_D	$T_A=25^\circ C$	2.0
		$T_A=70^\circ C$	1.3
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	R_{THJA}	t <= 5 sec	62.5
		Steady state	110

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	-0.3			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uA
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-5	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-20			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = -10 \text{ V}, I_D = -1 \text{ A}$			42	m Ω
		$V_{GS} = -4.5 \text{ V}, I_D = -1 \text{ A}$			57	
Forward Transconductance ^A	g_{fs}	$V_{DS} = -5 \text{ V}, I_D = -1 \text{ A}$		10		S
Diode Forward Voltage	V_{SD}	$I_S = 1 \text{ A}, V_{GS} = 0 \text{ V}$		-0.8		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -20 \text{ V}, V_{GS} = -5 \text{ V},$ $I_D = -1 \text{ A}$		7		nC
Gate-Source Charge	Q_{gs}			1		
Gate-Drain Charge	Q_{gd}			2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -20 \text{ V}, R_L = 6 \Omega, I_D = -1 \text{ A},$ $V_{GEN} = -10 \text{ V}$		10		ns
Rise Time	t_r			20		
Turn-Off Delay Time	$t_{d(off)}$			60		
Fall-Time	t_f			20		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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