N-Channel 40-V (D-S) MOSFET

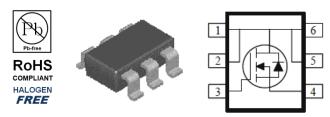
Key Features:

- Low r_{DS(on)} trench technology
- · Low thermal impedance
- Fast switching speed

Typical Applications:

- White LED boost converters
- Automotive Systems
- Industrial DC/DC Conversion Circuits

PRODUCT SUMMARY				
Vds (V)	$r_{DS(on)}(m\Omega)$	I⊳(A)		
40	32 @ V _{GS} = 10V	6.5		
	44 @ V _{GS} = 4.5V	5.6		



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}C$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Limit	Units	
Drain-Source Voltage			40	V	
Gate-Source Voltage	V _{GS}	±20	v		
Continuous Drain Current ^a	T _A =25°C	1	6.5	A	
Continuous Drain Current	T _A =70°C	I _D	5.3		
Pulsed Drain Current ^b	I _{DM}	20			
Continuous Source Current (Diode Conduction) ^a		I _S	2.6	А	
Device Discipation ^a	T _A =25°C	P _D	2	w	
Power Dissipation ^a	T _A =70°C	' D	1.3	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Maximum	Units		
Maximum Junction-to-Ambient ^a	t <= 10 sec	R_{\thetaJA}	62.5	°C/W		
	Steady State	ιν _θ ιΑ	110	C/VV		

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \text{ uA}$	1			V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA	
Zero Gate Voltage Drain Current		$V_{DS} = 32 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA	
	IDSS	$V_{DS} = 32 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			25	uA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = 5 V, V_{GS} = 10 V$	10			Α	
	r	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 5 \text{ A}$			32	mΩ	
Drain-Source On-Resistance ^a	r _{DS(on)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 4 \text{ A}$			44		
Forward Transconductance ^a	g _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 5 \text{ A}$		20		S	
Diode Forward Voltage ^a	V_{SD}	$I_{\rm S} = 1.3$ A, $V_{\rm GS} = 0$ V		0.77		V	
		Dynamic ^b					
Total Gate Charge	Qg			3.4		nC	
Gate-Source Charge	Q _{gs}	$V_{DS} = 20 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V},$ $I_{D} = 5 \text{ A}$		0.7			
Gate-Drain Charge	Q _{gd}	$D = 3 \Lambda$		1.7		1	
Turn-On Delay Time	t _{d(on)}	$V_{DS} = 20 \text{ V}, \text{ R}_{L} = 4 \Omega,$		2			
Rise Time	t _r	$v_{DS} = 20 v, R_L - 4 \Omega,$ $I_D = 5 A,$		7			
Turn-Off Delay Time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$		17		ns	
Fall Time	t _f	$v_{\text{GEN}} = 10^{\circ} v$, $N_{\text{GEN}} = 0.22$		5			
Input Capacitance	C _{iss}			287			
Output Capacitance	C _{oss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		42		pF	
Reverse Transfer Capacitance	C _{rss}			34			

Notes

- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.

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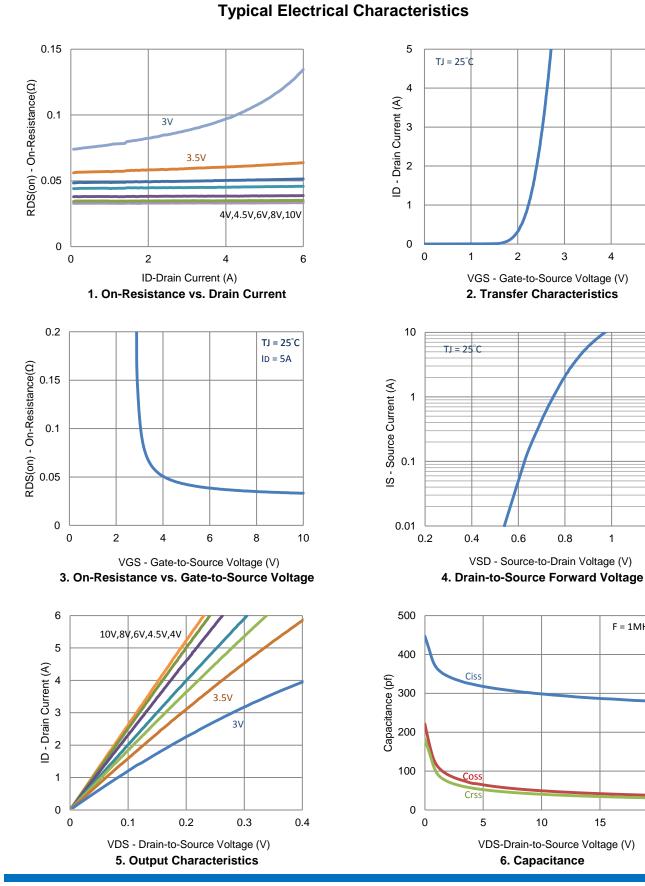
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F = 1MHz

1.2

20

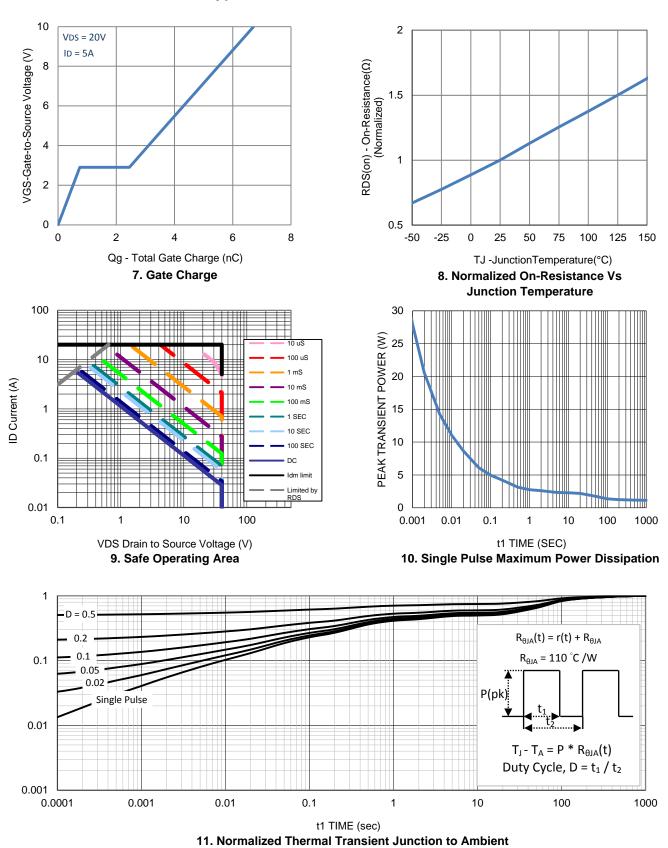
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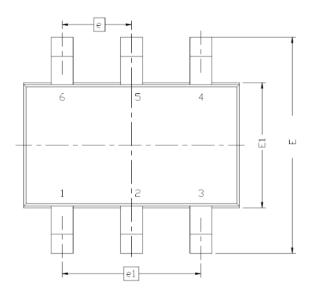
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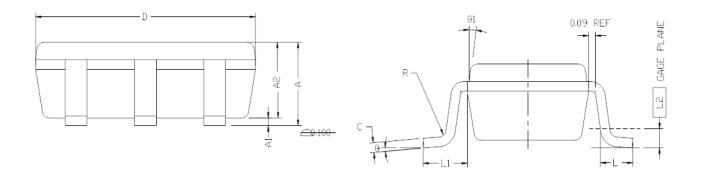


Typical Electrical Characteristics

Package Information



DIM.	MILLIMETERS				
DIM.	MIN	NDM	MAX		
Α	0.935		1.10		
A1	0.01		0.10		
A2	0.70		1.00		
b	0.25	0.32	0.40		
\subset	0.10	0.15	0.20		
D	2.95	3.05	3.10		
Ε	2.70	2.85	2.98		
E1	1.55	1.65	1.70		
е	0.95 BSC				
L	0.30		0.60		
L1	0.60REF				
L2	0.25BSC				
R	0.10				
θ	0?	4?	8?		
θ1	7? NOM				



Note:

- 1. All Dimension Are In mm.
- 2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- 3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
- 4. The Package Top May Be Smaller Than The Package Bottom.
- Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.