Analog Power AM3446N

# N-Channel 20-V (D-S) MOSFET

## **Key Features:**

- Low r<sub>DS(on)</sub> trench technology
- · Low thermal impedance
- · Fast switching speed

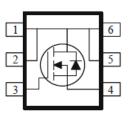
<b>Typical</b>	Дþ	plica	atior	ıs:
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- Power Routing
- Li Ion Battery Packs
- · Level Shifting and Driver Circuits

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$r_{DS(on)}(m\Omega)$	I□ (A)		
20	$32 @ V_{GS} = 4.5V$	6.5		
	44 @ V <sub>GS</sub> = 2.5V	5.6		







ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^{\circ}$ C UNLESS OTHERWISE NOTED)					
Parameter			Limit	Units	
Drain-Source Voltage		$V_{DS}$	20	V	
Gate-Source Voltage	$V_{GS}$	±12	V		
Continuous Drain Current <sup>a</sup>	T <sub>A</sub> =25°C	· I <sub>D</sub>	6.5		
Continuous Diain Curient	T <sub>A</sub> =70°C	טי	5.3	Α	
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	30			
Continuous Source Current (Diode Conduction) a	I <sub>S</sub>	2.9	Α		
Dower Dissipation <sup>a</sup>	T <sub>A</sub> =25°C	$P_{D}$	2	W	
Power Dissipation <sup>a</sup>	T <sub>A</sub> =70°C	' D	1.3	VV	
Operating Junction and Storage Temperature Range			-55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter			Maximum	Units		
Maximum Junction-to-Ambient <sup>a</sup>	t <= 10 sec	$R_{\theta JA}$	62.5	°C/W		
Maximum Junction-to-Ambient	Steady State	IXOJA	110	C/VV		

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#### Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

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### **Electrical Characteristics**

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \text{ uA}$				V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			±100	nA	
Zara Cata Valtaga Drain Current	1	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	10			Α	
Drain Cauras On Basistanas a	r	$V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A}$			32	mΩ	
Drain-Source On-Resistance <sup>a</sup>	r <sub>DS(on)</sub>	$V_{GS} = 2.5 \text{ V}, I_D = 1.6 \text{ A}$			44	11122	
Forward Transconductance a	g <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_{D} = 2 \text{ A}$		9		S	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_{S} = 1.5 \text{ A}, V_{GS} = 0 \text{ V}$		0.67		V	
		Dynamic <sup>b</sup>					
Total Gate Charge	$Q_g$	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V},$		12			
Gate-Source Charge	$Q_{gs}$	$I_D = 2 A$		2.1		nC	
Gate-Drain Charge	$Q_gd$	10 - 2 A		2.8			
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DS} = 10 \text{ V}, R_{L} = 5 \Omega,$		8			
Rise Time	t <sub>r</sub>	$V_{DS} = 10 \text{ V}, K_L - 3 \Omega,$ $I_D = 2 \text{ A},$		19		ne	
Turn-Off Delay Time	$t_{d(off)}$	$V_{GEN} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$		60		ns	
Fall Time	t <sub>f</sub>	VGEN - 4.5 V, NGEN - 0 12		17			
Input Capacitance	C <sub>iss</sub>			727			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ Mhz}$		74		pF	
Reverse Transfer Capacitance	$C_{rss}$			69			

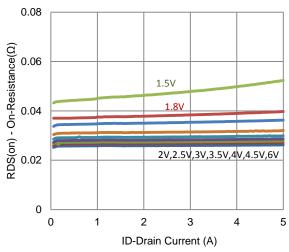
#### Notes

- Pulse test: PW <= 300us duty cycle <= 2%.
- Guaranteed by design, not subject to production testing. b.

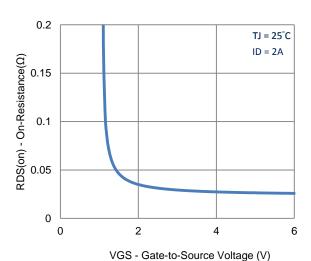
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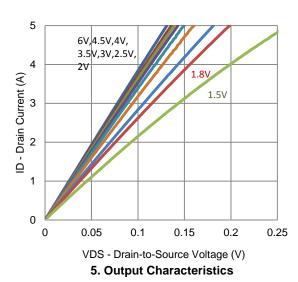
## **Typical Electrical Characteristics**



#### 1. On-Resistance vs. Drain Current

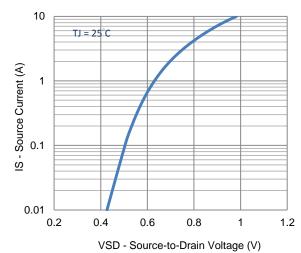


3. On-Resistance vs. Gate-to-Source Voltage

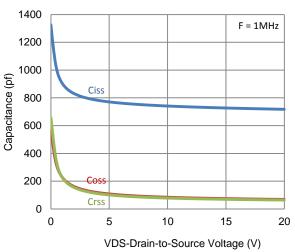


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2. Transfer Characteristics



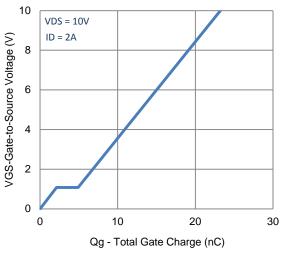
4. Drain-to-Source Forward Voltage



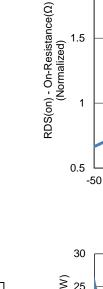
6. Capacitance

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## **Typical Electrical Characteristics**



7. Gate Charge



-25

0

25

2

TJ -JunctionTemperature(°C) 8. Normalized On-Resistance Vs **Junction Temperature** 

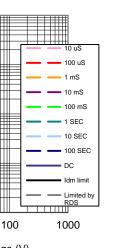
50

75

100

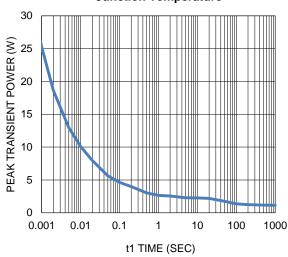
125

150

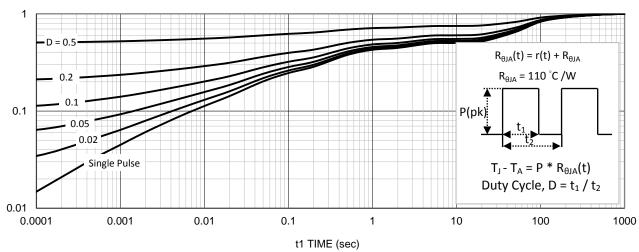


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10. Single Pulse Maximum Power Dissipation



11. Normalized Thermal Transient Junction to Ambient

100

10

0.1

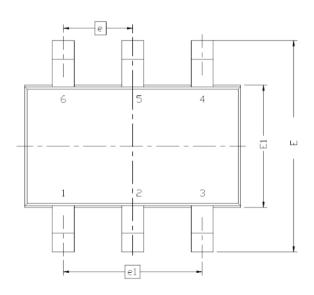
0.01

0.1

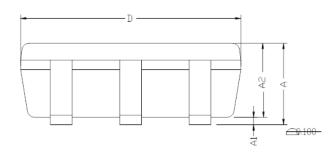
ID Current (A)

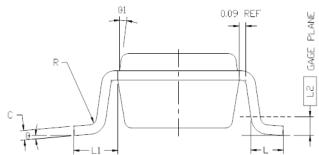
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## **Package Information**



DIM.	MILLIMETERS				
	MIN	NDM	MAX		
Α	0.935		1.10		
A1	0.01		0.10		
A2	0.70		1.00		
b	0.25	0.32	0.40		
C	0.10	0.15	0.20		
D	2.95	3.05	3.10		
Ε	2.70	2.85	2.98		
E1	1.55	1.65	1.70		
6	0.95 BSC				
L	0.30		0.60		
L1	0.60REF				
L2	0.25BSC				
R	0.10				
θ	0?	4?	8?		
θ1	7? N□M				





#### Note:

- 1. All Dimension Are In mm.
- Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
- 4. The Package Top May Be Smaller Than The Package Bottom.
- Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.