

Am3448A

IEEE-488 Quad Bidirectional Transceiver

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DISTINCTIVE CHARACTERISTICS

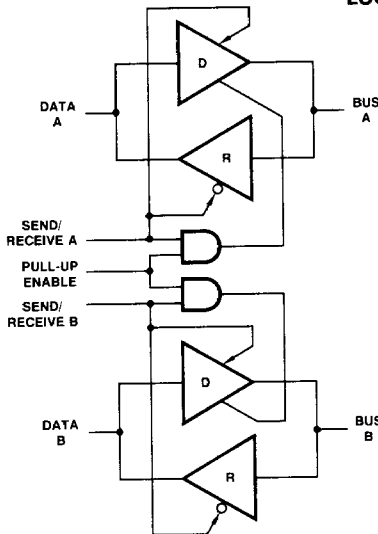
- Four independent driver/receiver pairs
- Three-state outputs
- High impedance inputs
- Receiver hysteresis – 600mV (Typ.)
- Fast Propagation Times – 15-20ns (Typ.)
- TTL compatible receiver outputs
- Single +5 volt supply
- Open collector driver output option with internal passive pull up
- Power up/power down protection (No invalid information transmitted to bus)
- No bus loading when power is removed from device
- Required termination characteristics provided
- Advanced Schottky processing
- 100% product assurance screening to MIL-STD-883 requirements

GENERAL DESCRIPTION

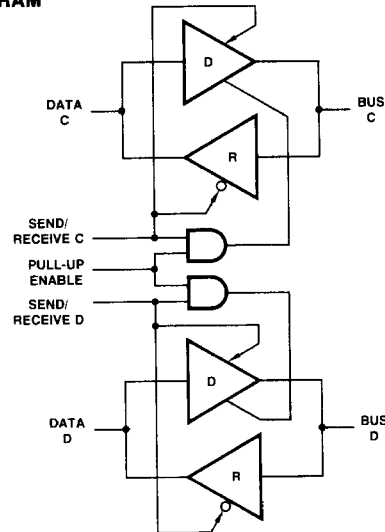
The Am3448A is a quad bidirectional transceiver meeting the requirement of IEEE-488 standard digital interface for programmable instrumentation for the driver, receiver, and composite device load. One pull-up enable input is provided for each pair of transceivers which controls the operating mode of the driver outputs as either an open collector or active pull-up configuration.

The receivers feature input hysteresis for improved noise immunity in system applications. The device bus (receiver input) changes from standard bus loading to a high impedance load when power is removed. In addition no spurious noise is generated on the bus during power-up or power-down.

LOGIC DIAGRAM



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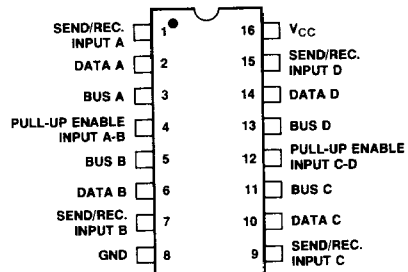


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ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +70°C	MC3448AL
Molded DIP	0°C to +70°C	MC3448AP
Dice	0°C to +70°C	AM3448AX

CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

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ABSOLUTE MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	-65°C to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Driver Output Current	150mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am3448A $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ $V_{CC \text{ MIN.}} = 4.75\text{V}$ $V_{CC \text{ MAX.}} = 5.25\text{V}$ **DC ELECTRICAL CHARACTERISTICS** over operating temperature range

Parameters	Description	Test Conditions	Typ. (Note 1)		Units		
			Min.	Max.			
Bus Characteristics							
$V_{(BUS)}$	Bus Voltage	Bus Pin Open, $V_{I(S/R)} = 0.8\text{V}$	2.75		3.7	Volts	
$V_{I(C)(BUS)}$		$I_{(BUS)} = -12\text{mA}$			-1.5		
$I_{(BUS)}$	Bus Current	$5.0\text{V} \leq V_{(BUS)} \leq 5.5\text{V}$	0.7		2.5	mA	
		$V_{(BUS)} = 0.5\text{V}$	-1.3		-3.2		
		$V_{CC} = 0\text{V}, 0\text{V} \leq V_{(BUS)} \leq 2.75\text{V}$			0.04		
Driver Characteristics							
$V_{I(C)(D)}$	Driver Input Clamp Voltage	$V_{I(S/R)} = 2.0\text{V}, I_{I(C)(D)} = -18\text{mA}$			-1.5	Volts	
$V_{OH(D)}$	Driver Output Voltage – High Logic State	$V_{I(S/R)} = 2.0\text{V}, V_{IH(D)} = 2.0\text{V}, V_{IH(E)} = 2.0\text{V}, I_{OH} = -5.2\text{mA}$	2.5			Volts	
$V_{OL(D)}$	Driver Output Voltage – Low Logic State	$V_{I(S/R)} = 2.0\text{V}, I_{OL(D)} = 48\text{mA}$			0.5	Volts	
$I_{OS(D)}$	Output Short Circuit Current	$V_{I(S/R)} = 2.0\text{V}, V_{IH(D)} = 2.0\text{V}, V_{IH(E)} = 2.0\text{V}$	-30		-120	mA	
$V_{IH(D)}$	Driver Input Voltage – High Logic State	$V_{I(S/R)} = 2.0\text{V}$	2.0			Volts	
$V_{IL(D)}$	Driver Input Voltage – Low Logic State	$V_{I(S/R)} = 2.0\text{V}$			0.8	Volts	
$I_{I(D)}$	Driver Input Current – Data Pins	$V_{I(S/R)} = V_{I(E)} = 2.0\text{V}$	-200		$0.5 \leq V_{I(D)} \leq 2.7\text{V}$	40	μA
$I_{IB(D)}$					$V_{I(D)} = 5.5\text{V}$	200	
Receiver Characteristics							
$V_{HYS(R)}$	Receiver Input Hysteresis	$V_{I(S/R)} = 0.8\text{V}$	400	600		mV	
$V_{ILH(R)}$	Receiver Input Threshold	$V_{I(S/R)} = 0.8\text{V}$, Low to High		1.6	1.8	Volts	
$V_{IHL(R)}$		$V_{I(S/R)} = 0.8\text{V}$, High to Low	0.8	1.0			
$V_{OH(R)}$	Receiver Output Voltage – High Logic State	$V_{I(S/R)} = 0.8\text{V}, I_{OH(R)} = -800\mu\text{A}, V_{(BUS)} = 2.0\text{V}$	2.7			Volts	
$V_{OL(R)}$	Receiver Output Voltage – Low Logic State	$V_{I(S/R)} = 0.8\text{V}, I_{OL(R)} = 16\text{mA}, V_{(BUS)} = 0.8\text{V}$			0.5	Volts	
$I_{OS(R)}$	Receiver Output Short Circuit Current	$V_{I(S/R)} = 0.8\text{V}, V_{(BUS)} = 2.0\text{V}$	-15		-75	mA	
Enable, Send/Receive Characteristics							
$I_{I(S/R)}$	Input Current – Send/Receive	$0.5 \leq V_{I(S/R)} \leq 2.7\text{V}$	-100		20	μA	
$I_{IB(S/R)}$		$V_{I(S/R)} = 5.5\text{V}$			100		
$I_{I(E)}$	Input Current – Enable	$0.5 \leq V_{I(E)} \leq 2.7\text{V}$	-200		20	μA	
$I_{IB(E)}$		$V_{I(E)} = 5.5\text{V}$			100		
Power Supply Current							
I_{CCL}	Power Supply Current	Listening Mode – All Receivers On		63	85	mA	
I_{CCH}		Talking Mode – All Drivers On		106	125		

Note 1. Typical limits are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading.

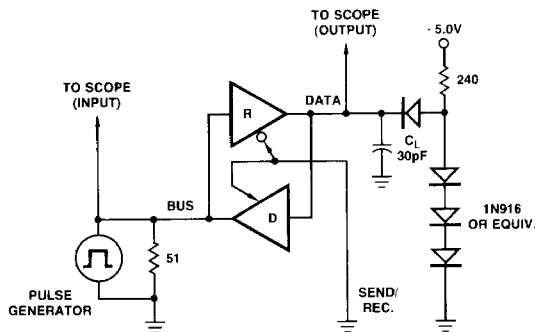
SWITCHING CHARACTERISTICS ($V_{CC} = 5.0V$, $T_A = 25^\circ C$ unless otherwise noted)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$t_{PLH(D)}$	Propagation Delay of Driver (Fig. 2)	Output Low to High	—		15	ns
$t_{PHL(D)}$		Output High to Low			17	
$t_{PLH(R)}$	Propagation Delay of Receiver (Fig. 1)	Output Low to High	—		25	ns
$t_{PHL(R)}$		Output High to Low			23	
$t_{PHZ(R)}$	Propagation Delay Time – Send/Receiver to Data (Fig. 4)	Logic High to Third State	—		30	ns
$t_{PZH(R)}$		Third State to Logic High			30	
$t_{PLZ(R)}$		Logic Low to Third State			30	
$t_{PZL(R)}$		Third State to Logic Low			30	
$t_{PHZ(D)}$	Propagation Delay Time – Send/Receiver to Bus (Fig. 3)	Logic High to Third State	—		30	ns
$t_{PZH(D)}$		Third State to Logic High			30	
$t_{PLZ(D)}$		Logic Low to Third State			30	
$t_{PZL(D)}$		Third State to Logic Low			30	
$t_{POFF(E)}$	Turn-On Time – Enable to Bus (Fig. 5)	Pull-Up Enable to Open Collector	—		30	ns
$t_{PON(E)}$		Open Collector to Pull-Up Enable			20	

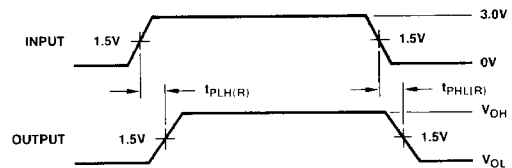
TRUTH TABLE

Send/Rec.	Enable	Into Flow	Comments
0	X	Bus → Data	
1	1	Data → Bus	Active Pull-Up
1	0	Data → Bus	Open Collector

X = Don't Care

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS


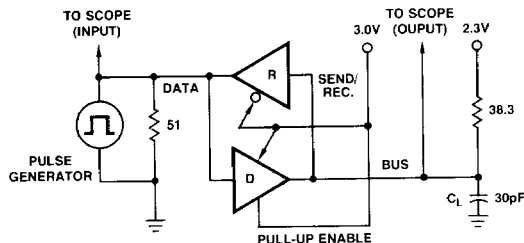
*Includes Jig and Probe Capacitance.


 $f = 1.0MHz$
 $t_{TLH} = t_{THL} \leq 5.0ns$ (10-90%)
 Duty Cycle = 50%

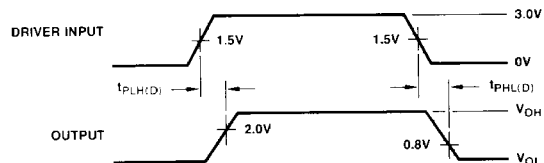
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Figure 1. Bus Input to Data Output (Receiver).

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*Includes Jig and Probe Capacitance.


 $f = 1.0MHz$
 $t_{TLH} = t_{THL} \leq 5.0ns$ (10-90%)
 Duty Cycle = 50%

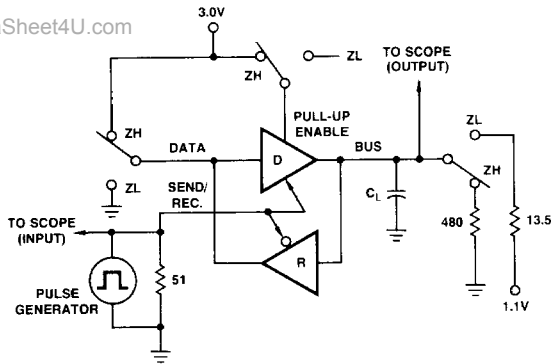
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Figure 2. Data Input to Bus Output (Driver).

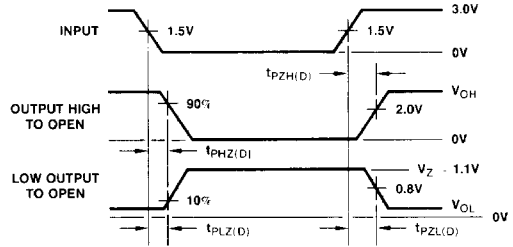
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PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS (Cont.)

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C_L = 15pF (Includes Jig and Probe Capacitance)

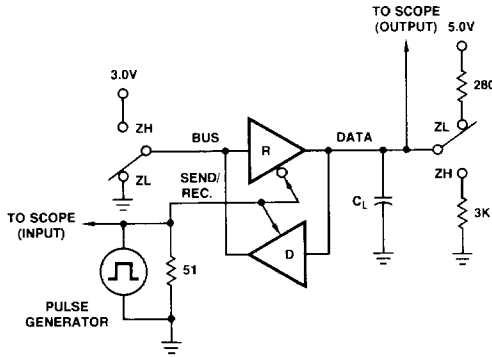


f = 1.0MHz
 t_{TLH} = t_{THL} ≤ 5.0ns (10-90%)
 Duty Cycle = 50%

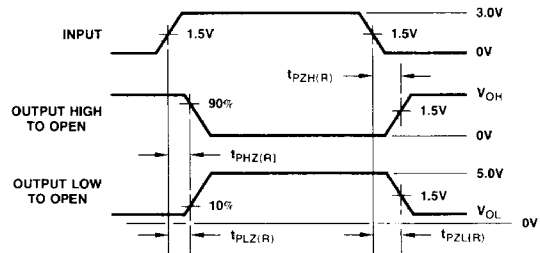
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Figure 3. Send/Receive Input to Bus Output (Driver).

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C_L = 15pF (Includes Jig and Probe Capacitance)

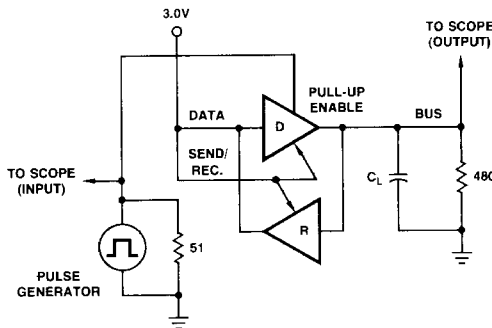


f = 1.0MHz
 t_{TLH} = t_{THL} ≤ 5.0ns (10-90%)
 Duty Cycle = 50%

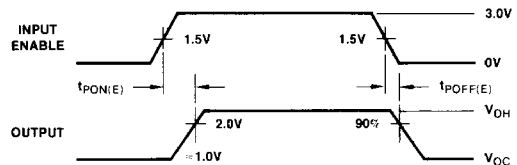
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Figure 4. Send/Receive Input to Data Output (Receiver).

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C_L = 15pF (Includes Jig and Probe Capacitance)



f = 1.0MHz
 t_{TLH} = t_{THL} ≤ 5.0ns (10-90%)
 Duty Cycle = 50%

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Figure 5. Enable Input to Bus Output (Driver).

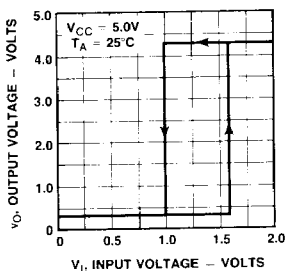
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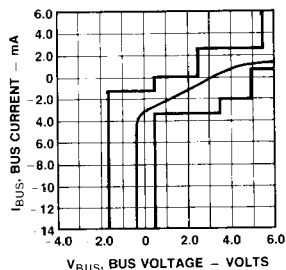
PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS (Cont.)

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TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

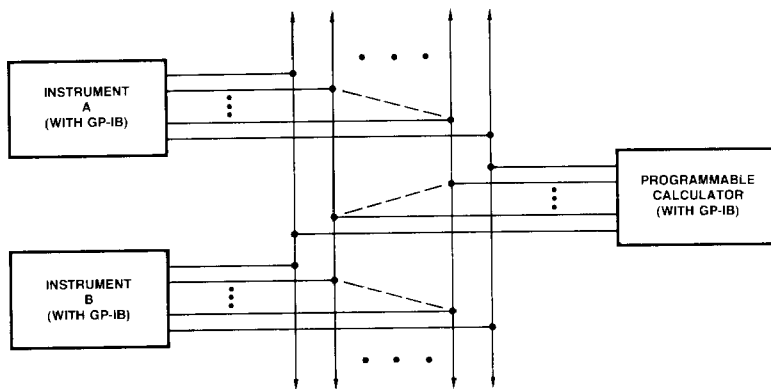


TYPICAL BUS LOAD LINE



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TYPICAL APPLICATION

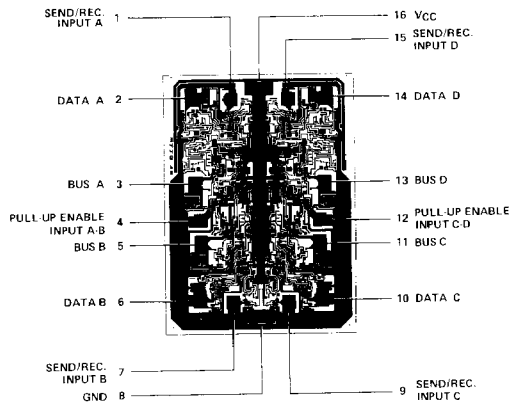


16 LINES TOTAL
(FOUR Am3448A'S FOR EACH BUS INTERFACE)

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TYPICAL MEASUREMENT SYSTEM APPLICATION

Metallization and Pad Layout



DIE SIZE .063" X .087"

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