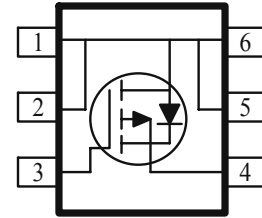
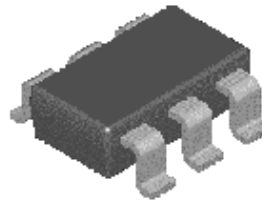


**P-Channel 60-V (D-S) MOSFET**

These miniature surface mount MOSFETs utilize High Cell Density process. Low  $r_{DS(on)}$  assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low  $r_{DS(on)}$  Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Extended VGS range ( $\pm 25$ ) for battery pack applications



PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
-60	0.310 @ $V_{GS} = -10V$	2.1
	0.465 @ $V_{GS} = -4.5V$	1.7

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		$V_{DS}$	-60	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$T_A = 25^\circ C$	$I_D$	2.1	A
	$T_A = 70^\circ C$		1.7	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	$\pm 15$	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	-1.7	A
Power Dissipation <sup>a</sup>	$T_A = 25^\circ C$	$P_D$	2.0	W
	$T_A = 70^\circ C$		1.3	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 5$ sec	$R_{\theta JA}$	62.5	$^\circ C/W$
			110	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
<b>Static</b>						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-1			
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -48 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uA
		$V_{DS} = -48 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-10	
On-State Drain Current <sup>A</sup>	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-20			A
Drain-Source On-Resistance <sup>A</sup>	$r_{DS(on)}$	$V_{GS} = -10 \text{ V}, I_D = -2.1 \text{ A}$			310	m $\Omega$
		$V_{GS} = -4.5 \text{ V}, I_D = -1.7 \text{ A}$			465	
Forward Transconductance <sup>A</sup>	$g_{fs}$	$V_{DS} = -15 \text{ V}, I_D = -2.1 \text{ A}$		8		S
Diode Forward Voltage	$V_{SD}$	$I_S = -2.5 \text{ A}, V_{GS} = 0 \text{ V}$			-1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -30 \text{ V}, V_{GS} = -4.5 \text{ V},$ $I_D = -2.1 \text{ A}$		18		nC
Gate-Source Charge	$Q_{gs}$			5		
Gate-Drain Charge	$Q_{gd}$			2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30 \text{ V}, R_L = 30 \Omega, I_D = -1 \text{ A},$ $V_{GEN} = -10 \text{ V}, R_G = 6\Omega$		8		nS
Rise Time	$t_r$			10		
Turn-Off Delay Time	$t_{d(off)}$			35		
Fall-Time	$t_f$			12		

## Notes

- Pulse test:  $PW \leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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