Analog Power

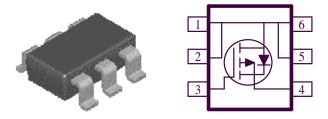
AM3471P

P-Channel 100-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSOP-6 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY			
V _{DS} (V)	$V_{DS}(V)$ $r_{DS(on)}(\Omega)$ I_D		
-100	$0.350 @ V_{GS} = -10V$	2.0	
	$0.450 @ V_{GS} = -4.5V$	1.8	



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V _{DS}	-100	V	
Gate-Source Voltage		V _{GS}	±20	v	
Continuous Drain Current ^a	T _A =25°C	ID	2.0		
	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	тр	1.6	А	
Pulsed Drain Current ^b		I _{DM}	±8		
Continuous Source Current (Diode Conduction) ^a		Is	-2.1	А	
Derver Dissignation ^a	$T_A=25^{\circ}C$	D_	2.0	W	
Power Dissipation ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	гD	1.3	٧V	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
	t <= 5 sec	$R_{\theta JA}$	62.5	°C/W	
Maximum Junction-to-Ambient ^a			110	°C/W	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^{\circ}C$ UNLESS OTHERWISE NOTED)							
Parame te r	S-maked	Test Conditions	Limits			TT *4	
	Symbol		Min	Тур	Max	Unit	
Static							
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \text{ uA}$	-1				
Gate-Body Leakage	Igss	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			±100	nA	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -80 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uA	
Zero Gate voltage Dialit Current	IDSS	$V_{DS} = -80 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			-10	uA	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = -5 V, V_{GS} = -10 V$	-20			А	
- · · · · · · · · · · · · · · · · · · ·		$V_{GS} = -10 \text{ V}, I_D = -1.4 \text{ A}$			350	mΩ	
Drain-Source On-Resistance ^A	r _{DS(on)}	$V_{GS} = -4.5 \text{ V}, I_D = -1.2 \text{ A}$			450		
Forward Tranconductance ^A	g _{fs}	$V_{DS} = -15 \text{ V}, \text{ I}_D = -1.4 \text{ A}$		2.8		S	
Diode Forward Voltage	V _{SD}	$I_S = -1.4 A, V_{GS} = 0 V$			-1	V	
Dynamic ^b							
Total Gate Charge	Qg			6			
Gate-Source Charge	Qgs	$V_{DS} = -30 \text{ V}, \text{ V}_{GS} = -4.5 \text{ V},$		10		nC	
Gate-Drain Charge	Qgd	$I_{\rm D} = -1.4 {\rm A}$		3			
Turn-On Delay Time	t _{d(on)}			3			
Rise Time	tr	$V_{DD} = -30 \text{ V}, R_L = 30 \Omega$, $ID = -1 \text{ A},$ $VGEN = -10 \text{ V}, RG = 6\Omega$		3		nS	
Turn-Off Delay Time	$t_{d(off)}$			13			
Fall-Time	tf			7			

Notes

- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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