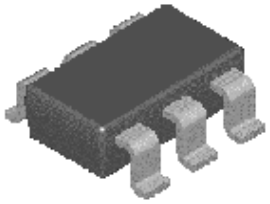
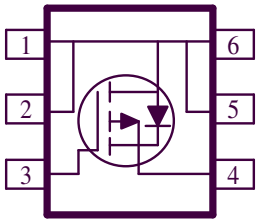
P-Channel 100-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-100	0.350 @ V_{GS} = -10V	2.0
	0.450 @ V_{GS} = -4.5V	1.8

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSOP-6 saves board space
- Fast switching speed
- High performance trench technology





ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	-100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[a]	T_A=25°C	I_D	2.0	A
	T_A=70°C		1.6	
Pulsed Drain Current[b]		I_{DM}	±8	
Continuous Source Current (Diode Conduction)[a]		I_S	-2.1	A
Power Dissipation[a]	T_A=25°C	P_D	2.0	W
	T_A=70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Ambient[a]	t <= 5 sec	$R_{\theta JA}$	62.5	°C/W
			110	°C/W

Notes

a. Surface Mounted on 1” x 1” FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Limits**			**Unit**
			Min	**Typ**	**Max**	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 uA	-1			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V, V_{GS} = 0 V			-1	uA
		V_{DS} = -80 V, V_{GS} = 0 V, T_J = 55°C			-10	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = -5 V, V_{GS} = -10 V	-20			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = -10 V, I_D = -1.4 A			350	mΩ
		V_{GS} = -4.5 V, I_D = -1.2 A			450	
Forward Tranconductance[A]	g_{fs}	V_{DS} = -15 V, I_D = -1.4 A		2.8		S
Diode Forward Voltage	V_{SD}	I_S = -1.4 A, V_{GS} = 0 V			-1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = -30 V, V_{GS} = -4.5 V, I_D = -1.4 A		6		nC
Gate-Source Charge	Q_{gs}			10		
Gate-Drain Charge	Q_{gd}			3		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -30 V, R_L = 30 Ω , ID = -1 A, VGEN = -10 V, RG = 6Ω		3		nS
Rise Time	t_r			3		
Turn-Off Delay Time	$t_{d(off)}$			13		
Fall-Time	t_f			7		

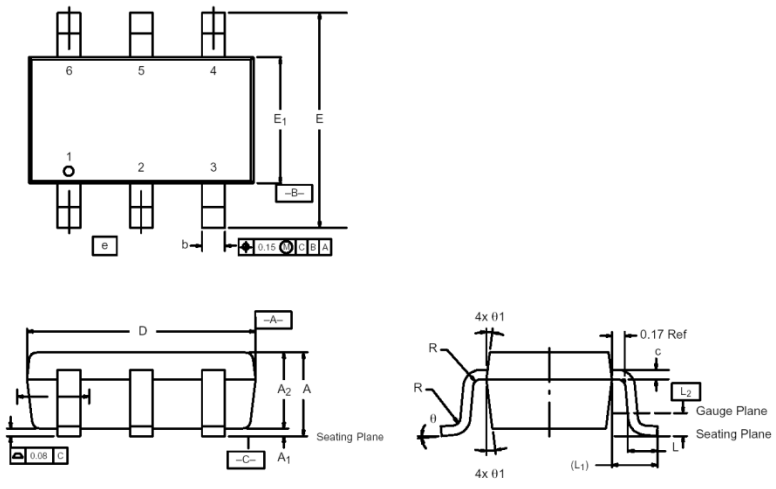
Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information

TSOP-6: 6LEAD



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	–	1.10	0.036	–	0.043
A_1	0.01	–	0.10	0.0004	–	0.004
A_2	0.84	–	1.00	0.033	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	1.00 BSC			0.0394 BSC		
L	0.35	–	0.50	0.014	–	0.020
L_1	0.60 Ref			0.024 Ref		
L_2	0.25 BSC			0.010 BSC		
R	0.10	–	–	0.004	–	–
θ	0°	4°	8°	0°	4°	8°
θ_1	7° Nom			7° Nom		