#### AM3904N

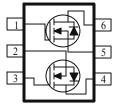
### **Dual N-Channel Logic Level MOSFET**

These miniature surface mount MOSFETs utilize High Cell Density process. Low  $r_{DS(on)}$  assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are logic switch control, power management in portable and batterypowered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r<sub>DS(on)</sub> Provides Higher Efficiency and Extends Battery Life
- Miniature TSOP-6 Surface Mount Package Saves Board Space
- Very fast switching
- Gate to Source Zener Diode ESD Protect

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (OHM)	I <sub>D</sub> (A)	
25	$0.45 @ V_{GS} = 4.5 V$	0.5	
	$0.63 @ V_{GS} = 2.5V$	0.2	





ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C UNLESS OTHERWISE NOTED)						
Parameter			Maximum	Units		
Drain-Source Voltage		$V_{DS}$	25	V		
Gate-Source Voltage		V <sub>GS</sub>	8			
Continuous Drain Current <sup>a</sup>	$T_A=25^{\circ}C$	I.	0.7			
Continuous Drain Current	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	ID	0.58	А		
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	2			
Continuous Source Current (Diode Conduction) <sup>a</sup>		Is	±0.3	А		
	$T_A=25^{\circ}C$	D	0.9	W		
Power Dissipation <sup>a</sup>	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	РD	0.7	vv		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Maximum	Units			
Movimum lunction to Ambient <sup>a</sup>	t <= 5 sec	D	140	°C/W			
Maximum Junction-to-Ambient <sup>a</sup>	Steady-State	R <sub>THJA</sub>	180	C/VV			

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

			Limits			<b>T</b> T •4	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Drain-Source Breakdown Voltage	V(BR)DSS	$V_{GS} = 0 V, I_D = 250 uA$	25			v	
Gate-Threshold Voltage	VGS(th)	$V_{DS} = V_{GS}, I_D = -250 \text{ uA}$	0.67	0.85	1.5		
Gate-Body Leakage	Igss	$V_{DS} = 20 V, V_{GS} = 0 V$			100	nA	
Zara Cata Valtaga Drain Current	T	$V_{DS} = 20 V, V_{GS} = 0 V$			1	11 A	
Zero Gate Voltage Drain Current	Idss	$V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55^{\circ}C$			10	uA	
On-State Drain Current <sup>A</sup>	ID(on)	$V_{DS} = 5 V, V_{GS} = 2.5 V$	0.5			Α	
		$V_{GS} = 4.5 V$ , $I_D = 0.5 A$		0.33	0.45	Ω	
Drain-Source On-Resistance <sup>A</sup>	rDS(on)	$V_{GS} = 4.5 \text{ V}, I_D = 0.5 \text{ A} \text{ TJ} = 55^{\circ} \text{C}$		0.36	0.49		
		$V_{GS} = 2.5 V$ , $I_D = 0.2 A$		0.45	0.63	1	
Forward Tranconductance <sup>A</sup>	g <sub>fs</sub>	$V_{DS} = 5 V$ , $I_D = 0.5 A$		1.5		S	
Diode Forward Voltage	Vsd	$I_{S} = 0.5 A, V_{GS} = 0 V$		0.85	1.20	V	
Dynamic <sup>b</sup>						•	
Total Gate Charge	Qg	$V_{DS} = 5 V, V_{GS} = 4.5 V, I_D = 0.5 A$		1.7	2.3	nC	
Gate-Source Charge	Qgs			0.38	0.72		
Gate-Drain Charge	Qgd			0.47	0.87		
Switching							
Turn-On Delay Time	td(on)			6.5	13		
Rise Time	tr	$V_{DD} = 6 V$ , $I_D = 0.5 A$ , $V_{GEN} = 4.5 V$ , $R_G = 50 \Omega$		11	19	ns	
Turn-Off Delay Time	td(off)			13	24		
Fall-Time	tſ			3	7	1	

Notes

a. Pulse test:  $PW \le 300$ us duty cycle  $\le 2\%$ .

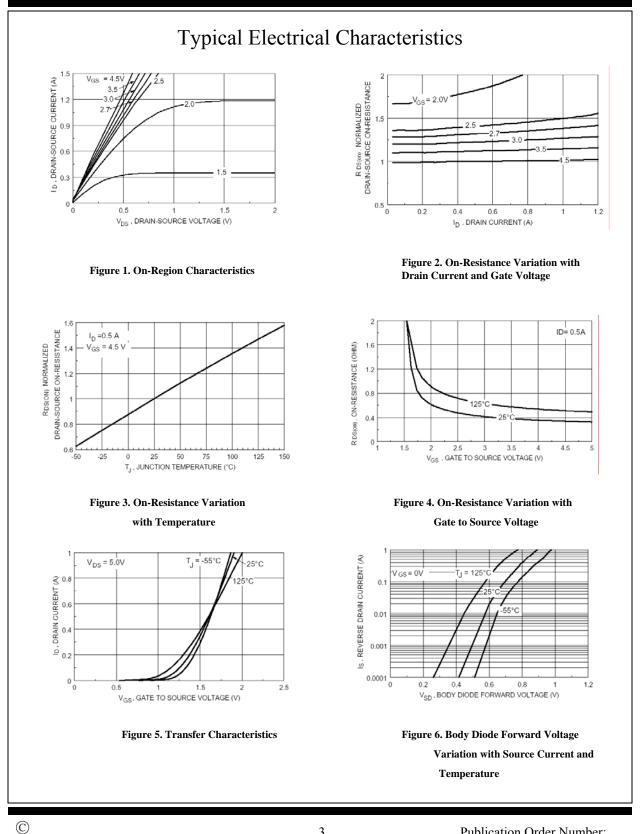
b. Guaranteed by design, not subject to production testing.

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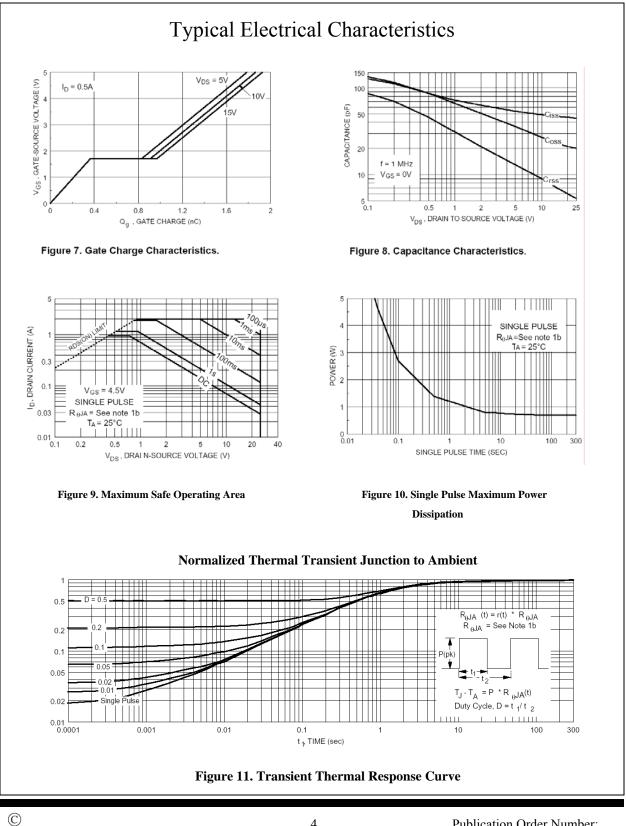
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