Analog Power AM3925P

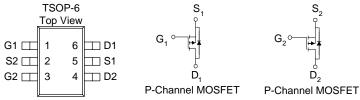
## P-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

•	Low r <sub>DS(on)</sub> provides higher efficiency and
	extends battery life

- Low thermal impedance copper leadframe TSOP-6 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY						
$V_{DS}(V)$	$r_{DS(on)}$ (OHM)	$I_{D}(A)$				
-20	$0.079 @ V_{GS} = -4.5V$	-3.2				
-20	$0.110 @ V_{GS} = -2.5V$	-2.7				



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C UNLESS OTHERWISE NOTED)						
Parame te r	Symbol	Maximum	Units			
Drain-Source Voltage	Drain-Source Voltage			V		
Gate-Source Voltage			±8	V		
Continuous Drain Current <sup>a</sup>	$T_A=25^{\circ}C$	Τ	-3.2	A		
Continuous Drain Current	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	ъ	-2.6			
Pulsed Drain Current <sup>b</sup>			-10			
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	±1.6	Α		
Power Dissipation <sup>a</sup>	$T_A=25^{\circ}C$		1.15	w		
Power Dissipation	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	1 D	0.7	**		
Operating Junction and Storage Temperature Range	· ·	$T_{J}, T_{stg}$	-55 to 150	°C		

THERMAL RESISTANCE RATINGS								
Parameter	Symbol	Тур	Max					
Mariana Innation to Analisata	t <= 10 sec	<b>R</b>	93	110	0C/W			
Maximum Junction-to-Ambient <sup>a</sup>	Steady State	$R_{thJA}$	130	150	°C/W			

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## Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)								
Downwatan	Cl1	T4 C 14	Limits			TT *4		
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit		
Static			<u> </u>					
Gate-Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = -250 \text{ uA}$	-0.40					
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V$ , $V_{GS} = +/-8 V$			±100	nA		
Zara Cata Valtaga Prain Current	IDSS	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uA		
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			-10			
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-3			A		
D i G G D i A		$V_{GS} = -4.5 \text{ V}, I_D = -3.2 \text{ A}$			0.079			
Drain-Source On-Resistance <sup>A</sup>	rDS(on)	$V_{GS} = -2.5 \text{ V}, I_D = -2.7 \text{ A}$			0.110	Ω		
Forward Tranconductance <sup>A</sup>	gs	$V_{DS} = -5 \text{ V}, I_D = -3.2 \text{ A}$		3		S		
Diode Forward Voltage	$V_{\mathrm{SD}}$	$I_S = -1.6 \text{ A}, V_{GS} = 0 \text{ V}$		-0.70		V		
Dynamic <sup>b</sup>	, ,				•	•		
Total Gate Charge	Qg	V 5 V V 4 5 V		12.2				
Gate-Source Charge	Qgs	$V_{DS} = -5 \text{ V}, V_{GS} = -4.5 \text{ V},$ $I_{D} = -3.2 \text{ A}$		1.1		пC		
Gate-Drain Charge	Qgd	ID – -3.2 A		1.5				
Turn-On Delay Time	t <sub>d(on)</sub>			6.5				
Rise Time	t <sub>r</sub>	$V_{DD} = -5 \text{ V}, R_L = 5 \text{ OHM},$		20		l no		
Turn-Off Delay Time	td(off)	$V_{GEN} = -4.5 \text{ V}, R_G = 6 \text{ OHM}$		31		ns		
Fall-Time	tf			21				

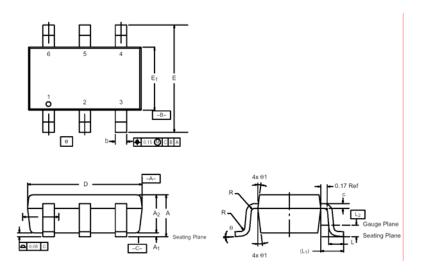
## Notes

- a. Pulse test:  $PW \le 300us duty cycle \le 2\%$ .
- b. Guaranteed by design, not subject to production testing.

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## Package Information

TSOP-6: 6LEAD



	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
Α	0.91	-	1.10	0.036	-	0.043
A <sub>1</sub>	0.01	_	0.10	0.0004	_	0.004
A <sub>2</sub>	0.84	-	1.00	0.033	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
С	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
Е	2.70	2.85	2.98	0.106	0.112	0.117
E <sub>1</sub>	1.55	1.65	1.70	0.061	0.065	0.067
е	1.00 BSC			0.0394 BSC		
L	0.35	_	0.50	0.014	_	0.020
L <sub>1</sub>	0.60 Ref				0.024 Ref	
L <sub>2</sub>	0.25 BSC 0.010 BSC					
R	0.10	_	_	0.004	_	_
θ	0°	4°	8°	0°	4°	8°
$\theta_1$	7° Nom 7° Nom					