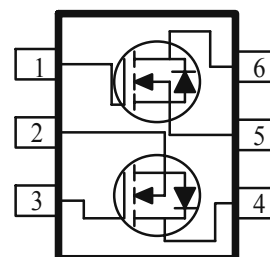
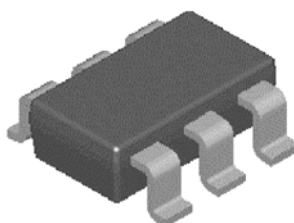


Dual N-Channel Logical Level MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSOP-6 saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (OHM)	I_D (A)
20	0.058 @ $V_{GS} = 4.5$ V	3.7
	0.082 @ $V_{GS} = 2.5$ V	3.1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current ^a	$T_A=25$ °C	I_D	3.7	A
	$T_A=70$ °C		2.9	
Pulsed Drain Current ^b		I_{DM}	8	
Continuous Source Current (Diode Conduction) ^a		I_S	1.05	A
Power Dissipation ^a	$T_A=25$ °C	P_D	1.15	W
	$T_A=70$ °C		0.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typ	Max	
Maximum Junction-to-Ambient ^a	t ≤ 10 sec	R_{thJA}	93	110	°C/W
	Steady State		130	150	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions				Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	0.7			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 12 \text{ V}$			1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$			0.1	μA
		$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			1	μA
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	30			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 3.7 \text{ A}$			0.058	Ω
		$V_{GS} = 2.5 \text{ V}, I_D = 2.7 \text{ A}$			0.082	
Forward Transconductance ^A	g_{fs}	$V_{DS} = 10 \text{ V}, I_D = 6.8 \text{ A}$		10		S
Diode Forward Voltage ^A	V_{SD}	$I_S = 1.05 \text{ A}, V_{GS} = 0 \text{ V}$		0.80		S
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=3.7\text{A}$		7.5		nC
Gate-Source Charge	Q_{gs}			0.6		
Gate-Drain Charge	Q_{gd}			1.0		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=1\text{A}, R_{GEN}=15\Omega$		5		nS
Rise Time	t_r			12		
Turn-Off Delay Time	$t_{d(off)}$			13		
Fall-Time	t_f			7		

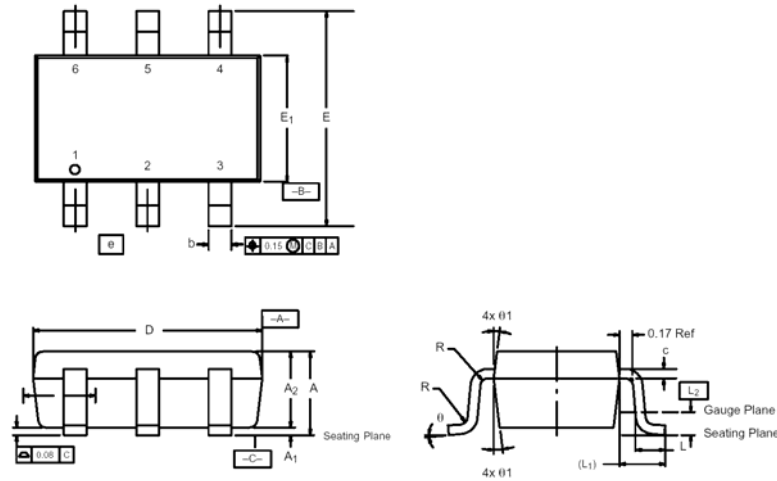
Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information

TSOP-6: 6LEAD



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	—	1.10	0.036	—	0.043
A ₁	0.01	—	0.10	0.0004	—	0.004
A ₂	0.84	—	1.00	0.033	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	1.00 BSC			0.0394 BSC		
L	0.35	—	0.50	0.014	—	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		