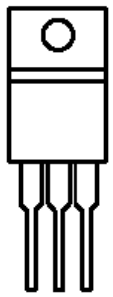
## P-Channel 60-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TO-220 saves board space
- Fast switching speed
- High performance trench technology

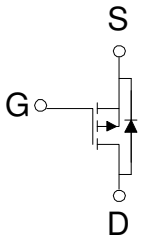
| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | $r_{DS(on)}$ m(Ω) | $I_D$ (A) |
| -60 | 135 @ $V_{GS}$ = -10V | -39[a] |
| | 150 @ $V_{GS}$ = -4.5V | |

TO-220AB




Top View

DRAIN connected to TAB




P-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C UNLESS OTHERWISE NOTED) | | | | |
|---|---|---|---|---|
| Parameter | | Symbol | Limit | Units |
| Drain-Source Voltage | | $V_{DS}$ | -60 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | |
| Continuous Drain Current[a] | $T_C$=25°C | $I_D$ | -90 | A |
| Pulsed Drain Current[b] | | $I_{DM}$ | -390 | |
| Continuous Source Current (Diode Conduction)[a] | | $I_S$ | -110 | A |
| Power Dissipation[a] | $T_C$=25°C | $P_D$ | 300 | W |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to 175 | °C |

| THERMAL RESISTANCE RATINGS | | | |
|---|---|---|---|
| Parameter | Symbol | Maximum | Units |
| Maximum Junction-to-Ambient[a] | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Junction-to-Case | $R_{\theta JC}$ | 0.5 | °C/W |

Notes

a. Package Limited

b. Pulse width limited by maximum junction temperature

## SPECIFICATIONS ($T_A$ = 25°C UNLESS OTHERWISE NOTED)

| Parameter | Symbol | Test Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **Static** | | | | | | |
| Gate-Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = -250 uA | -1 | | | V |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = -20 V | | | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = -48 V, $V_{GS}$ = 0 V | | | -1 | uA |
| | | $V_{DS}$ = -48 V, $V_{GS}$ = 0 V, $T_J$ = 55°C | | | -25 | |
| On-State Drain Current[A] | $I_{D(on)}$ | $V_{DS}$ = -5 V, $V_{GS}$ = -10 V | -120 | | | A |
| Drain-Source On-Resistance[A] | $r_{DS(on)}$ | $V_{GS}$ = -10 V, $I_D$ = -1 A | | | 135 | mΩ |
| | | $V_{GS}$ = -4.5 V, $I_D$ = -1 A | | | 150 | |
| Forward Tranconductance[A] | $g_{fs}$ | $V_{DS}$ = -15 V, $I_D$ = -1 A | | 30 | | S |
| Diode Forward Voltage | $V_{SD}$ | $I_S$ = -1 A, $V_{GS}$ = 0 V | | -1.1 | | V |
| **Dynamic[b]** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = -15 V, $V_{GS}$ = -4.5 V, $I_D$ = -1 A | | 19 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 4 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 7 | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = -25 V, $R_L$ = 25 Ω , $I_D$ = -1 A, $V_{GEN}$ = -10 V | | 14 | | nS |
| Rise Time | $t_r$ | | | 9 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 90 | | |
| Fall-Time | $t_f$ | | | 30 | | |

Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

# Package Information