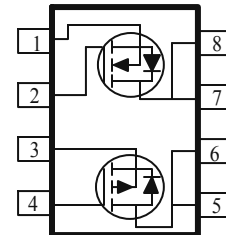


P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} m(Ω)	I _D (A)
30	40 @ V _{GS} = 4.5V	6.0
	28 @ V _{GS} = 10V	7.0
-26.5	80 @ V _{GS} = -2.5V	-4.0
	52 @ V _{GS} = -4.5V	-5.2



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V _{DS}	30	-26.5	V
Gate-Source Voltage		V _{GS}	±20	±12	
Continuous Drain Current ^a	T _A =25°C	I _D	7	-5.2	A
	T _A =70°C		5.6	-6.8	
Pulsed Drain Current ^b		I _{DM}	20	-20	
Continuous Source Current (Diode Conduction) ^a		I _S	1.3	-1.3	A
Power Dissipation ^a	T _A =25°C	P _D	2.1	2.1	W
	T _A =70°C		1.3	1.3	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Case ^a	t ≤ 5 sec	R _{θJC}	40	°C/W
Maximum Junction-to-Ambient ^a	t ≤ 5 sec	R _{θJA}	60	°C/W

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Conditions	Limits				Unit
			Ch	Min	Typ	Max	
Static							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 uA	N	30			V
		V _{GS} = 0 V, I _D = -250 uA	P	-26			
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 uA	N	1			V
		V _{GS} = V _{DS} , I _D = -250 uA	P	-1			
Gate-Body Leakage	I _{GSS}	V _{GS} = -12 V, V _{DS} = 0 V	P			±100	nA
		V _{GS} = 20 V, V _{DS} = 0 V	N			±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -21.2 V, V _{GS} = 0 V	P			-1	uA
		V _{DS} = 24 V, V _{GS} = 0 V	N			1	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N	20			A
		V _{DS} = -5 V, V _{GS} = -4.5 V	P	-20			
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 7 A	N			28	mΩ
		V _{GS} = 4.5 V, I _D = 6 A				40	
		V _{GS} = -4.5 V, I _D = -5 A	P			52	
		V _{GS} = -2.5 V, I _D = -4 A				80	
Forward Transconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 7 A	N		25		S
		V _{DS} = -15 V, I _D = -5 A	P		10		
Dynamic							
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, V _{GS} =10V, I _D =7A P-Channel V _{DS} =-15V, V _{GS} =-4.5V, I _D =-5A	N		4		nC
			P		25		
Gate-Source Charge	Q _{gs}		N		1.1		
			P		2.4		
Gate-Drain Charge	Q _{gd}		N		1.4		
			P		3.9		
Switching							
Turn-On Delay Time	t _{d(on)}	N-Channeel V _{DD} =15V, V _{GS} =10V, I _D =1A , R _{GEN} =6Ω, P-Channel V _{DD} =-15V, V _{GS} =-4.5V, I _D =-1A RGEN=6Ω	N		8		nS
			P		7		
Rise Time	t _r		N		5		
			P		13		
Turn-Off Delay Time	t _{d(off)}		N		23		
			P		14		
Fall-Time	t _f		N		3		
			P		9		

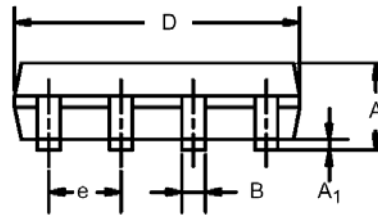
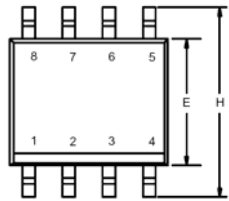
Notes

- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

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Package Information

SO-8: 8LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°

