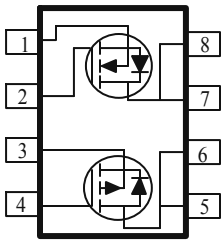
P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	40 @ V_{GS} = 4.5V	6.0
	28 @ V_{GS} = 10V	7.0
-26.5	80 @ V_{GS} = -2.5V	-4.0
	52 @ V_{GS} = -4.5V	-5.2

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		**Symbol**	**N-Channel**	**P-Channel**	**Units**
Drain-Source Voltage		V_{DS}	30	-26.5	V
Gate-Source Voltage		V_{GS}	±20	±12	
Continuous Drain Current[a]	T_A=25°C	I_D	7	-5.2	A
	T_A=70°C		5.6	-6.8	
Pulsed Drain Current[b]		I_{DM}	20	-20	
Continuous Source Current (Diode Conduction)[a]		I_S	1.3	-1.3	A
Power Dissipation[a]	T_A=25°C	P_D	2.1	2.1	W
	T_A=70°C		1.3	1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Case[a]	t <= 5 sec	$R_{\theta JC}$	40	°C/W
Maximum Junction-to-Ambient[a]	t <= 5 sec	$R_{\theta JA}$	60	°C/W

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

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PRELIMINARY

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SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)							
Parameter	**Symbol**	**Test Conditions**	**Limits**				**Unit**
			Ch	**Min**	**Typ**	**Max**	
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 uA	N	30			V
		V_{GS} = 0 V, I_D = -250 uA	P	-26			
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 uA	N	1			V
		V_{GS} = V_{DS}, I_D = -250 uA	P	-1			
Gate-Body Leakage	I_{GSS}	V_{GS} = -12 V, V_{DS} = 0 V	P			±100	nA
		V_{GS} = 20 V, V_{DS} = 0 V	N			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -21.2 V, V_{GS} = 0 V	P			-1	uA
		V_{DS} = 24 V, V_{GS} = 0 V	N			1	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	N	20			A
		V_{DS} = -5 V, V_{GS} = -4.5 V	P	-20			
Drain-Source On-Resistance[A]	$r_{DS(on)}$	VGS = 10 V, I_D = 7 A	N			28	mΩ
		VGS = 4.5 V, I_D = 6 A				40	
		VGS = -4.5 V, I_D = -5 A	P			52	
		VGS = -2.5 V, I_D = -4 A				80	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 15 V, I_D = 7 A	N		25		S
		V_{DS} = -15 V, I_D = -5 A	P		10		
Dynamic							
Total Gate Charge	Q_g	N-Channel V_{DS}=15V, V_{GS}=10V, I_D=7A P-Channel V_{DS}=-15V, V_{GS}=-4.5V, I_D=-5A	N		4		nC
			P		25		
Gate-Source Charge	Q_{gs}		N		1.1		
			P		2.4		
Gate-Drain Charge	Q_{gd}		N		1.4		
			P		3.9		
Switching							
Turn-On Delay Time	$t_{d(on)}$	N-Chaneel V_{DD}=15V, V_{GS}=10V, I_D=1A , R_{GEN}=6Ω, P-Channel V_{DD}=-15V, V_{GS}=-4.5V, I_D=-1A R_{GEN}=6Ω	N		8		nS
			P		7		
Rise Time	t_r		N		5		
			P		13		
Turn-Off Delay Time	$t_{d(off)}$		N		23		
			P		14		
Fall-Time	t_f		N		3		
			P		9		

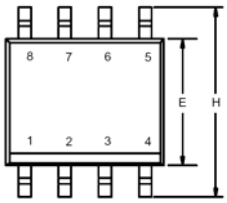
Notes

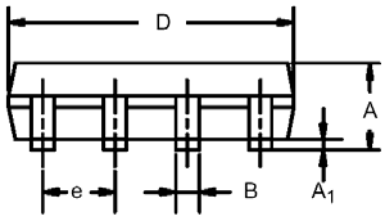
a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information

SO-8: 8LEAD





Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°