晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AM480272-00-0
APPROVED BY	
DATE	

☑ Approved For Specifications
☐ Approved For Specifications & Sample

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2008/12/31	--	New Release (16bit 80 interface)	Kokai

1 Features

3.4 inch AMOLED (Active Matrix Organic Light-Emitting Diode) module. This module is composed of a 3.4” AMOLED panel, LCD controller and power driver circuit.

1.1 AMOLED Feature :

(1) Construction: 3.4” AMOLED, HX5116 and FPC.
(2) Resolution (pixel): 480(R.G.B) X 272
(3) Interface: 40 pin pitch 0.5
(4) Power Supply Voltage: 3.3V single power input. Built-in power supply circuit.
(5) Fast Response Time : < 50 uS
(6) Wide Viewing Angle : 170°
(7) Hi contrast ratio : 10000:1
(8) Brightness : 200cd/m2

1.2 LCD Controller Feature:

(1) MCU interface 8/9/16/18 bit 80&68 series MCU interface.
(2) Display RAM size : 640x320x3x6 bits. Ex : 320x240 two frame buffer with 262K colors.
(3) Arbitrary display memory start position selection.
(4) 8 bit / 16 bit interface support 65K (R5G6B5) /262K(R6G6B6) colors data format.
(5) 9 bit / 18 bit interface support 262K(R6G6B6) colors data format only.

2 Physical specifications

Item	Specifications	Unit
Display resolution(dot)	480(R.G.B.) (W) x 272(H)	mm
Active area	74.88 (W) x 42.43 (H)	mm
Screen size	3.4 (Diagonal)	mm
Pixel size	0.156 (W) x 0.156 (H)	um
Color configuration	R.G.B stripe	
Overall dimension	82.8(W) x 54.3(H) x 5.8(D)	mm
Weight	T.B.D	mg

3 Default Setting & Option

- Interface :

The user can select the MCU interface by change the Jumper & Resister Array.

Setting / Interface Type	JP1	RA1	RA2	RA3	RA4	Remark
80-18Bit interface	1,2 short 2,3 open	2K ohm	OPEN	OPEN	OPEN	
80-16Bit interface	**1,2 short 2,3 open**	**OPEN**	**2K ohm**	**OPEN**	**OPEN**	Default
80-9Bit interface	1,2 short 2,3 open	OPEN	OPEN	2K ohm	OPEN	
80-8Bit interface	1,2 short 2,3 open	OPEN	OPEN	OPEN	2K ohm	
68-18Bit interface	1,2 open 2,3 short	2K ohm	OPEN	OPEN	OPEN	
68-16Bit interface	1,2 open 2,3 short	OPEN	2K ohm	OPEN	OPEN	
68-9Bit interface	1,2 open 2,3 short	OPEN	OPEN	2K ohm	OPEN	
68-8Bit interface	1,2 open 2,3 short	OPEN	OPEN	OPEN	2K ohm	

- Touch panel and Touch panel controller:

The user can select the with TP controller or without TP controller.

Pin Define / Option	SK/X1	DO/X2	DI/Y1	TPCS/Y2	IRQ	Remark
Without TP	**NC**	**NC**	**NC**	**NC**	**NC**	**Default**
With TP / Without TP controller	X1	X2	Y1	Y2	NC	
With TP / With TP controller	SK	DO	DI	TPCS	IRQ	

If user wants to change the default setting for mass production, please contact with Ampire. We'll apply a new P/N for you.

4 Electrical specification

4.1 Absolute max. ratings

4.1.1 Electrical Absolute max. ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VDD	VSS=0	-0.3	T.B.D	V	
Input voltege	V_{in}		-0.3	VDD+0.3	V	Note 1

Note1: /CS,/WR,/RD,RS,DB0~DB17

4.1.2 Environmental Absolute max. ratings

Item	OPERATING		STORAGE		Remark
	MIN	MAX	MIN	MAX	
Temperature	-20	70	-40	85	Note2,3,4,5
Humidity	Note1		Note1		
Corrosive Gas	Not Acceptable		Not Acceptable		

Note1 : Ta <= 40℃ : 85% RH max

Ta > 40℃ : Absolute humidity must be lower than the humidity of 85%RH at 40℃

Note2 : For storage condition Ta at -40℃ < 48h , at 85℃ < 100h

For operating condition Ta at -20℃ < 100h

Note3 : The response time will be slower at low temperature.

Note4 : Only operation is guarantied at operating temperature. Contrast , response time, another display quality are evaluated at +25℃

Note5 : This is panel surface temperature, not ambient temperature.

4.2 Electrical characteristics

4.2.1 DC Electrical characteristic of the AMOLED

Typical operating conditions (VSS=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	5.0	V	
Input Voltage for logic	H Level	V_{IH}	2.0	-	5.5	V	Note 1
	L Level	V_{IL}	VSS	-	0.8	V	
Output Voltage for Logic	H Level	V_{OH}	2.4	-	VDD	V	Note 2
	L Level	V_{OL}	VSS		0.4	V	
Power Supply current		IDD	-	T.B.D	-	mA	Note 3

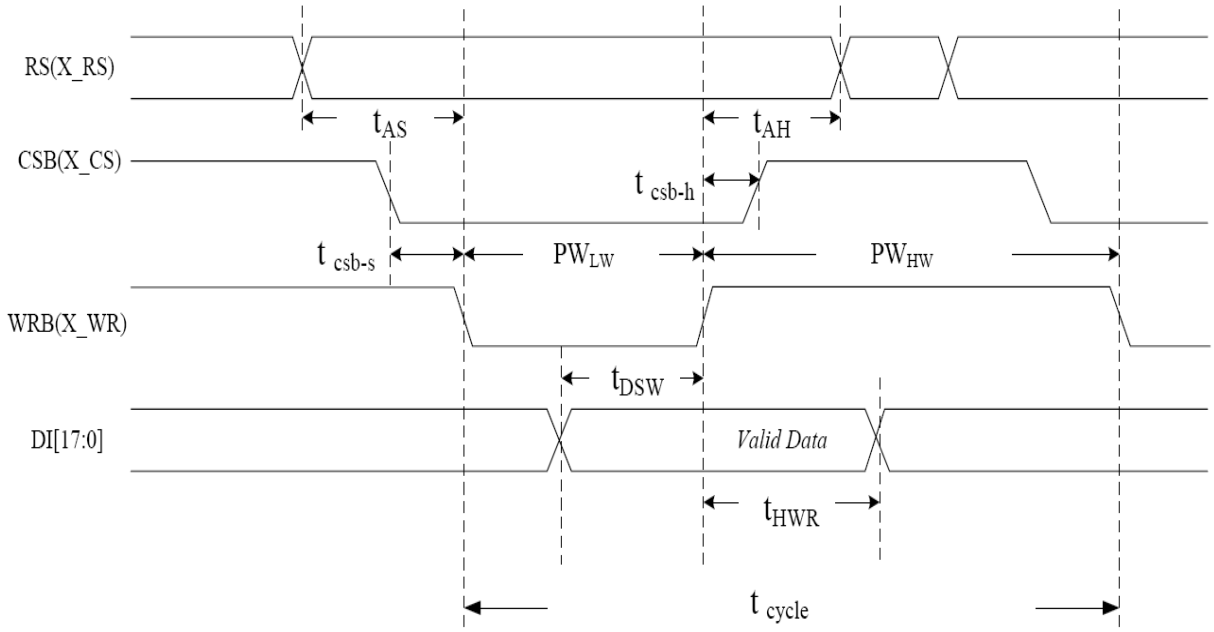
Note1: With 5V Tolerance Input, /CS, /WR,/RD,RS,DB0~DB17

Note2: /CS, /WR,/RD,RS,DB0~DB17

Note3: fv =60Hz , Ta=25℃ , Display pattern : 30% Pixel ON

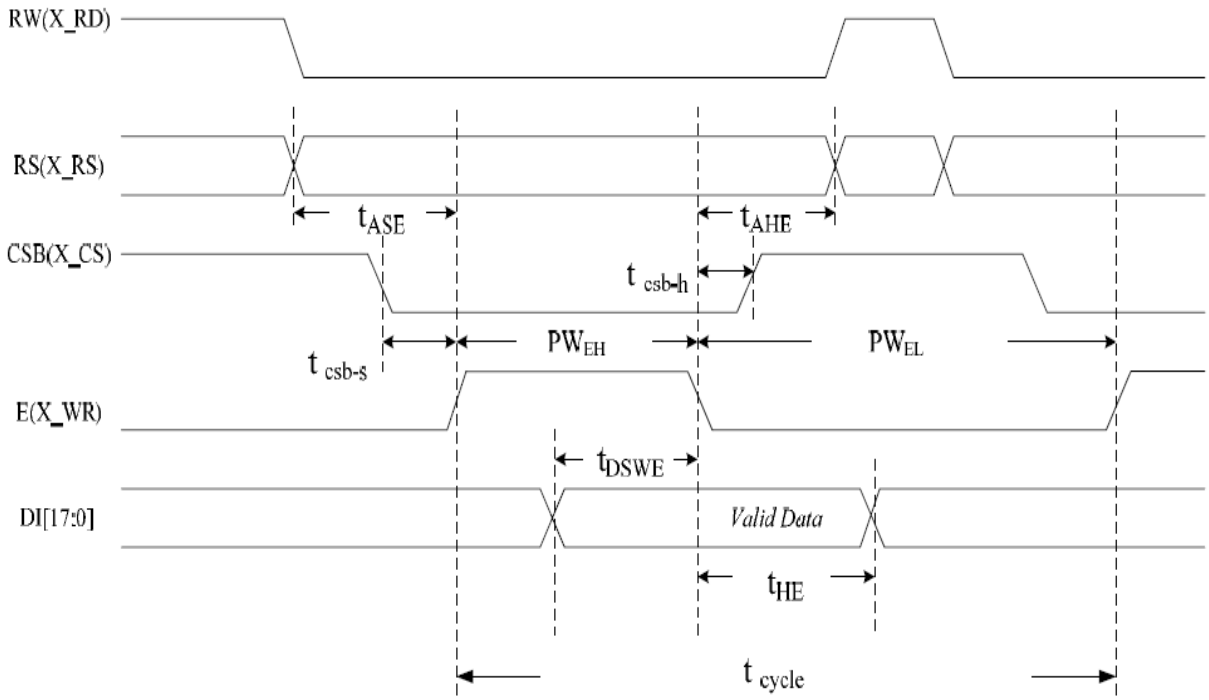
4.3 AC Timing characteristic of the Graphic TFT LCD controller

4.3.1 80 series Timing



Symbol	Parameter	Min	Typ	Max	Unit	Remark
t_{cycle}	Enable cycle time	100	200		ns	
PW_{HW}	Enable high-level pulse width	66	70		ns	
PW_{LW}	Enable low-level pulse width	33	130		ns	
t_{AS}	RS setup time	16	25		ns	
t_{AH}	RS hold time	16	45		ns	
t_{DSW}	Write data setup time	50	50		ns	
t_{HWR}	Write data hold time	50	40		ns	
t_{csb-s}	CSB setup time	16	20		ns	
t_{csb-h}	CSB hold time	16	30		ns	

4.3.2 68 series Timing



Symbol	Parameter	Min	Typ	Max	Unit	Remark
t_{cycle}	Enable cycle time	100	200		ns	
PW_{EH}	Enable high-level pulse width	66	70		ns	
PW_{EL}	Enable low level pulse width	33	130		ns	
t_{ASE}	RS setup time	16	25		ns	
t_{AHE}	RS hold time	16	45		ns	
t_{DSWE}	Write data setup time	50	50		ns	
t_{HE}	Write data hold time	50	40		ns	
t_{csb-s}	CSB setup time	16	20		ns	
t_{csbh}	CSB hold time	16	30		ns	

5 Optical specification

5.1 Optical characteristic :

Item		Symbol	Conditon	Min.	Typ.	Max.	Unit	Remark
Response Time		Tr / Tf	Θ=0°	--	--	50	μs	Note 1,2,3
Contrast ratio		CR	At optimized viewing angle	5000	10000	--		Note 1,2,4
Viewing Angle	Top		CR≧10	80	85	--	deg.	Note1,2, 5
	Bottom			80	85	--		
	Left			80	85	--		
	Right			80	85	--		
Brightness Without TP		Y_L	All Pixel ON 25℃	170	200	230	cd/m²	Note 1
Brightness With TP		Y_L	All Pixel ON 25℃	136	160	184	cd/m²	Note 1
Red chromaticity		X_R	Θ=0°	(0.62)	(0.66)	(0.70)		Note 1 , 2 For reference only. These data should be update according the prototype.
		Y_R		(0.30)	(0.34)	(0.38)		
Green chromaticity		X_G		(0.25)	(0.29)	(0.33)		
		Y_G		(0.62)	(0.66)	(0.70)		
Blue chromaticity		X_B		(0.11)	(0.15)	(0.19)		
		Y_B		(0.12)	(0.16)	(0.20)		
White chromaticity		X_W		(0.26)	(0.31)	(0.36)		
		Y_W		(0.28)	(0.31)	(0.36)		
Operation Life Time		LTop		20000			Hrs	Note1,6

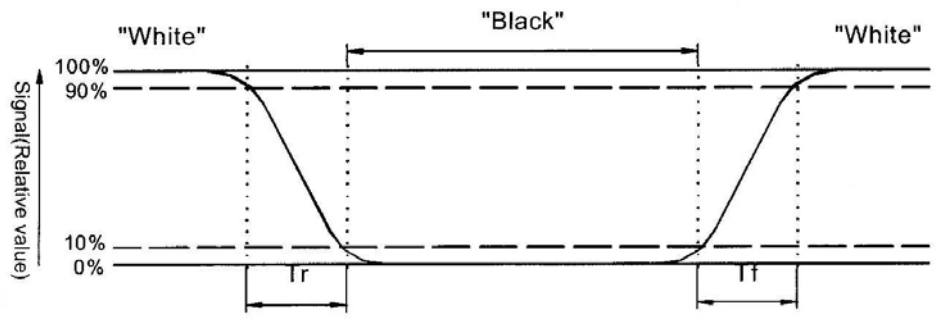
( )For reference only. These data should be update according the prototype.

Note 1: Ambient temperature=25℃,and AMOLED AR_VDD=5.0V , AR_VSS=-5.0V. To be measured in the dark room.

Note 2:To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-7,after 10 minutes operation. The measure position is the center of the Active area.

Note 3.Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black“ to “white”(falling time) and from ”white” to “black” (rising time),respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

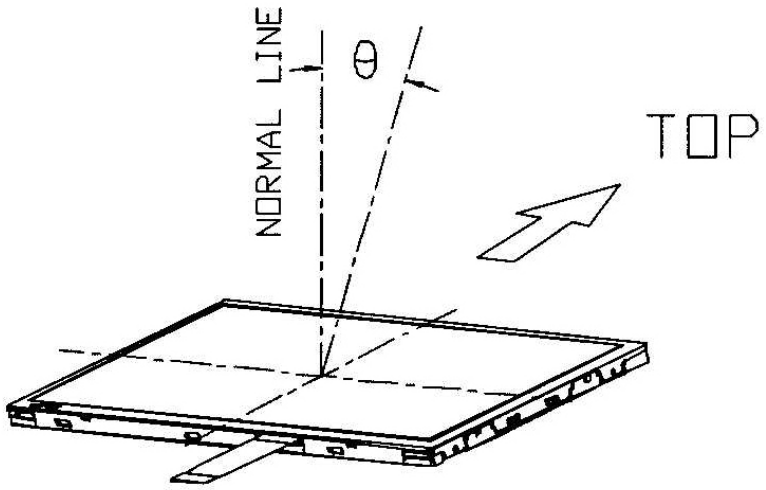


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio(CR)} = \frac{\text{Photo detector output when AMOLED is at "White"}}{\text{Photo detector Output when AMOLED is at "Black"}}$$

Note 5.Definition of viewing angle, Refer to figure as below.



Note 6. Brightness of 30 % power consumption. Operating Life Time is defined when the luminance has decayed to less than 50% of the initial measured luminance before life test.

6 Interface specifications

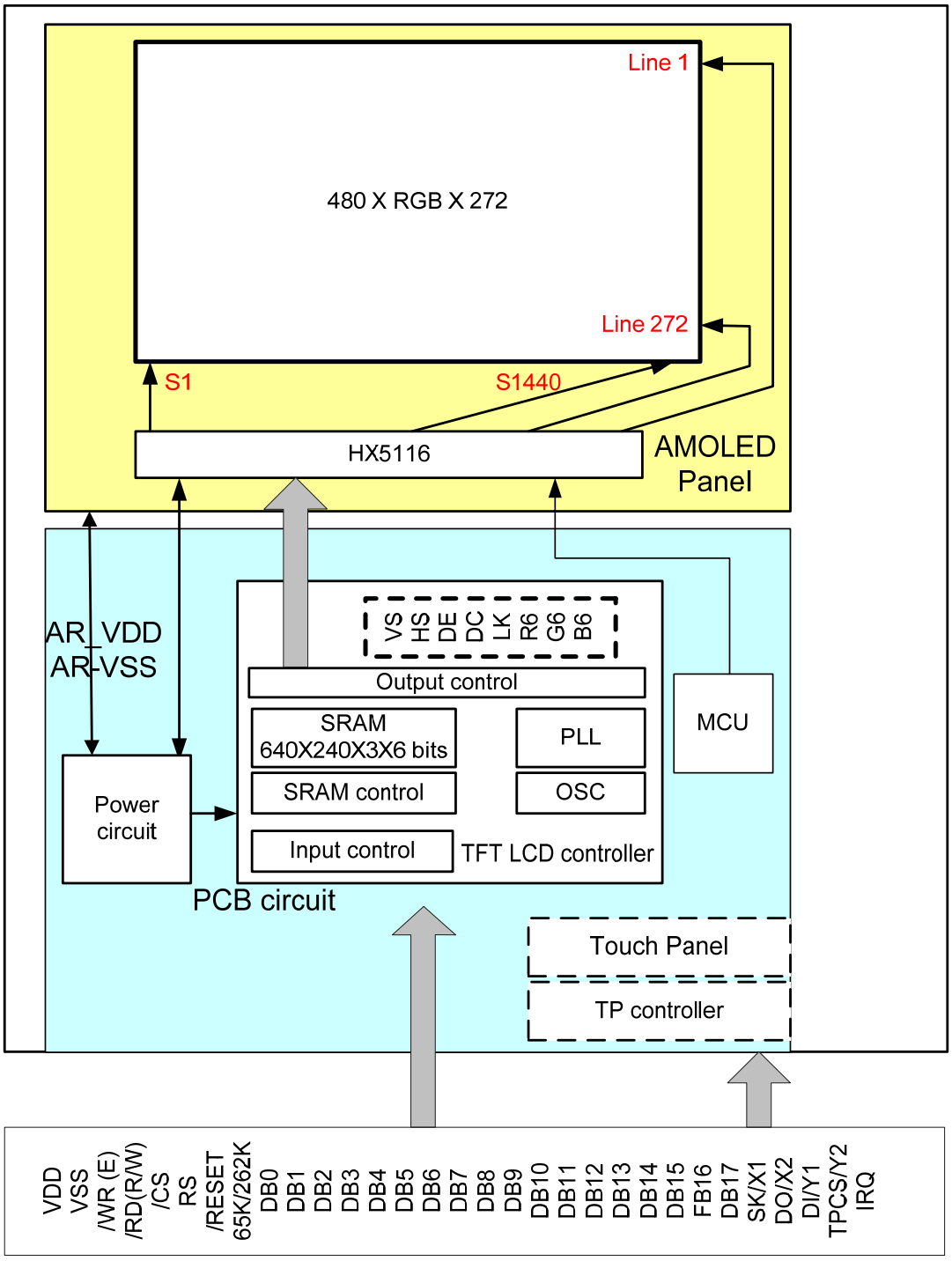
6.1 Driving signals for the AMOLED

Pin no	Symbol	I/O	Description	Remark
1 ~ 2	VSS		GND	
3~4	NC		No connection	
5	/RESET	I	Reset signal for AMOLE controller	
6	RS	I	Register and Data select for AMOLED controller	
7	/CS	I	Chip select low active signal for AMOLED controller	
8	/WR(E)	I	80mode : /WR low active signal for AMOLED 68mode : E signal latch on rising edge	
9	/RD(R/W)	I	80mode : /RD low active signal for AMOLED 68mode : R/W signal Hi: read Lo:Write	
10 ~ 27	DB0 ~ DB17	I/O	Data Bus	
28	65K/262K	I	Select colors data format H : 262K L : 65K	
29	VSS		GND	
30	Sk/X1	-	Serial clock for Touch panel controller Touch Panel Left Signal in X Axis	
31	DO/X2	-	Data Output for Touch panel controller Touch Panel Right Signal in X Axis	
32	DI/Y1	-	Data In for Touch panel controller Touch Panel Upper Signal in Y Axis	
33	TPCS/Y2	-	Chip Select for Touch panel controller Touch Panel Lower Signal in X Axis	
34	INT		Interrupt for Touch panel controller	
35 ~ 37	VDD		Power supply for the logic	
38 ~ 40	VSS		GND	

30~34 : SK, DO, DI, CS, INT for Touch Panel controller TSC2046

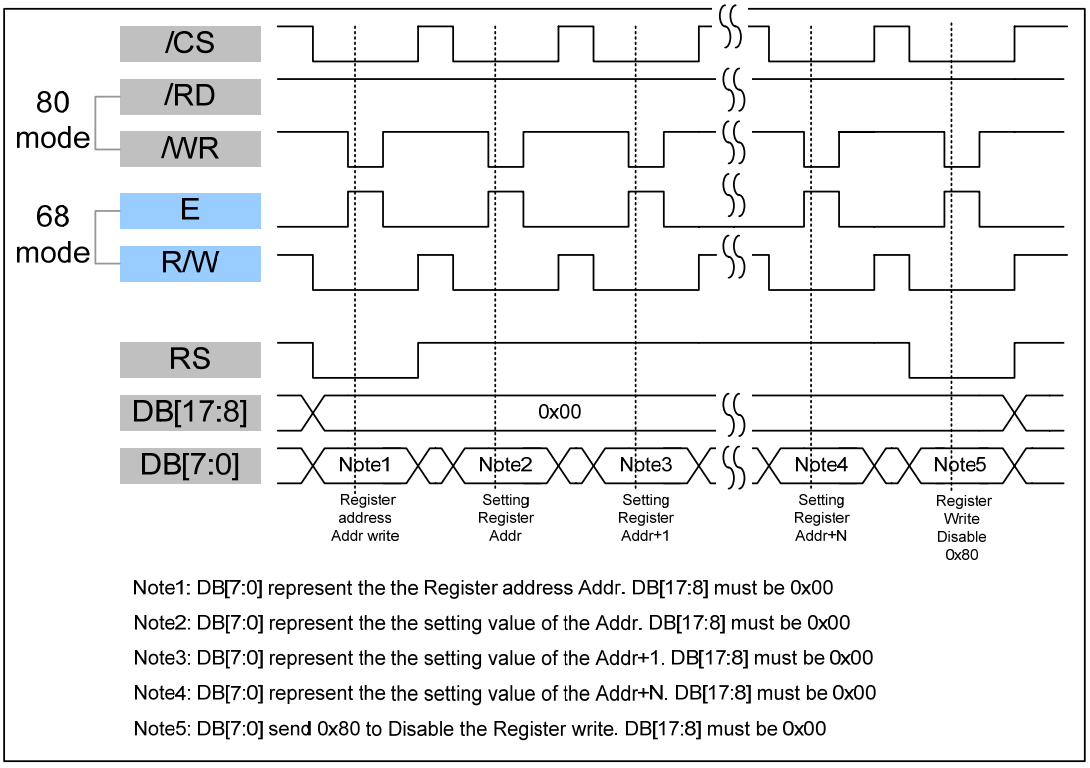
X1, X2, Y1, Y2 for Touch Panel (without TSC2046).

7 BLOCK DIAGRAM



8 Interface Protocol

8.1 18Bit-80/68-Write to Command Register



Note1: DB[7:0] represent the the Register address Addr. DB[17:8] must be 0x00

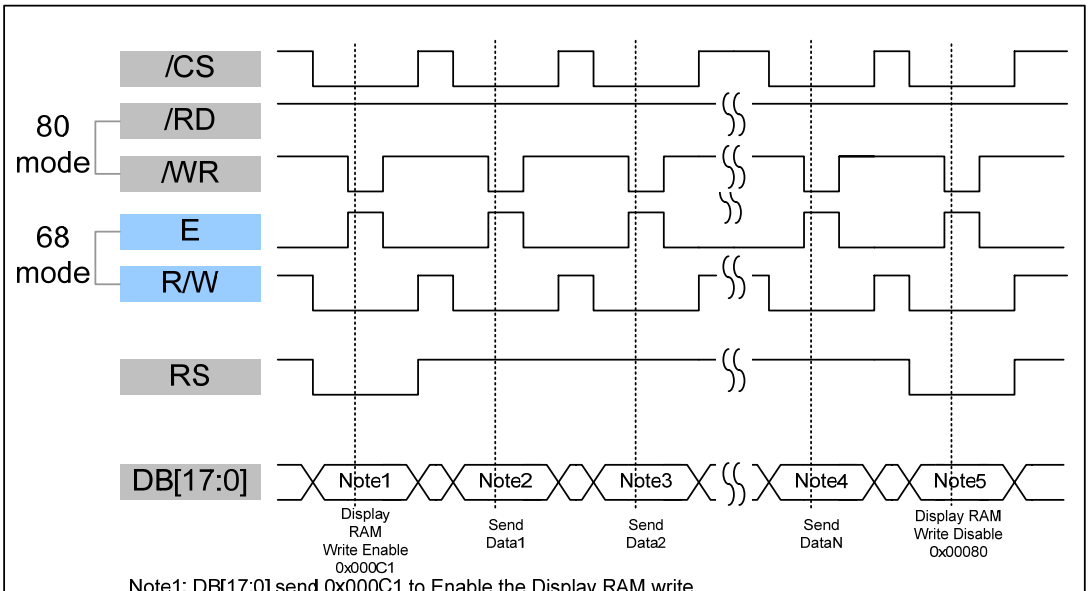
Note2: DB[7:0] represent the the setting value of the Addr. DB[17:8] must be 0x00

Note3: DB[7:0] represent the the setting value of the Addr+1. DB[17:8] must be 0x00

Note4: DB[7:0] represent the the setting value of the Addr+N. DB[17:8] must be 0x00

Note5: DB[7:0] send 0x80 to Disable the Register write. DB[17:8] must be 0x00

8.2 18Bit-80/68-Write to Display RAM



Note1: DB[17:0] send 0x000C1 to Enable the Display RAM write.

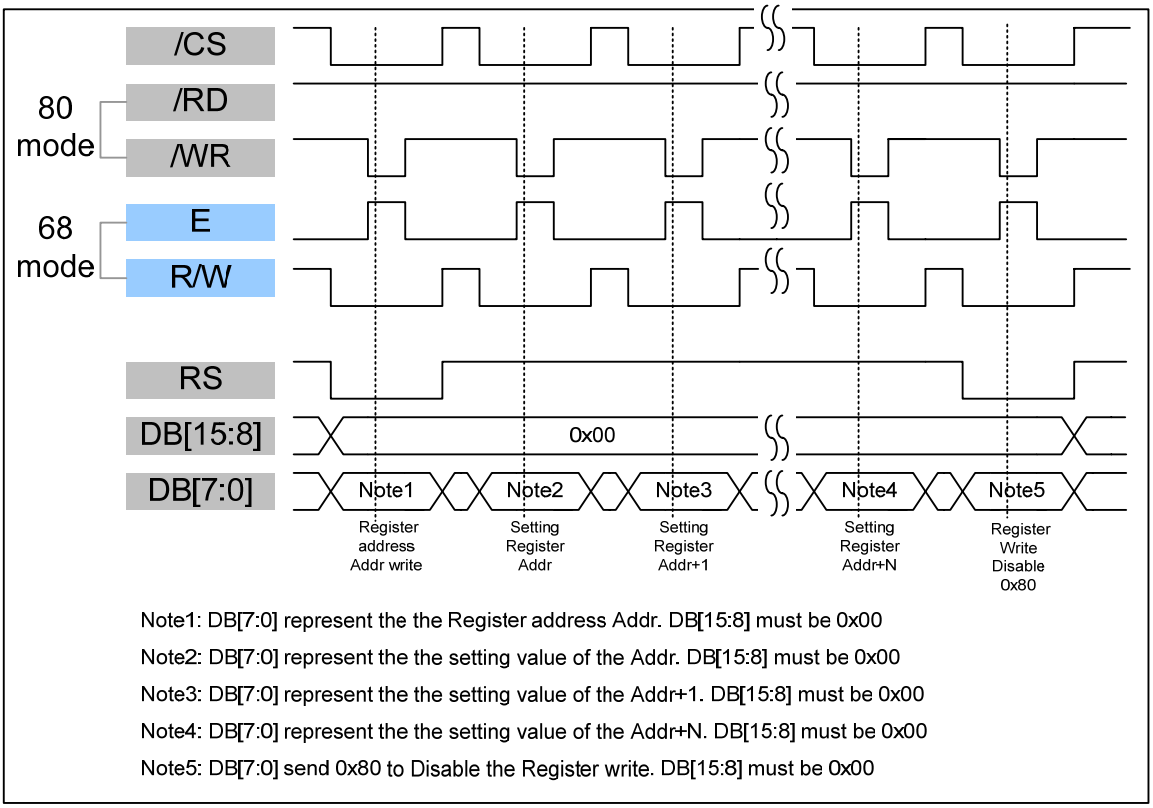
Note2: DB[17:0] represent the writing Data1 to Display RAM

Note3: DB[17:0] represent the writing Data2 to Display RAM

Note4: DB[17:0] represent the writing DataN to Display RAM

Note5: DB[17:0] send 0x00080 to Disable the Display RAM write.

8.3 16Bit-80/68- Write to Command Register



Note1: DB[7:0] represent the the Register address Addr. DB[15:8] must be 0x00

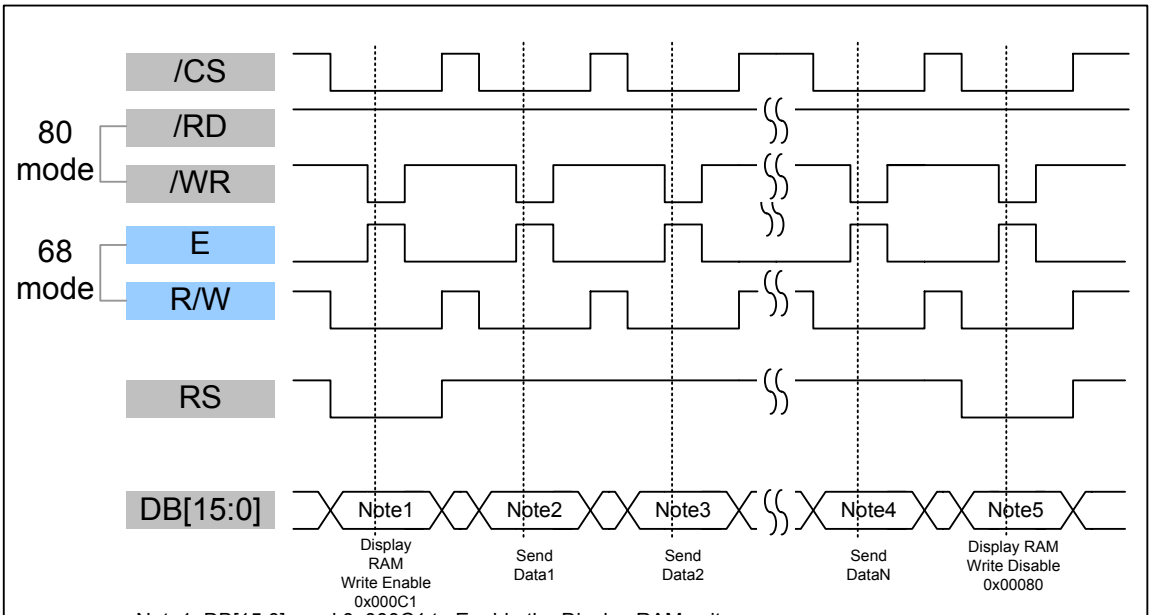
Note2: DB[7:0] represent the the setting value of the Addr. DB[15:8] must be 0x00

Note3: DB[7:0] represent the the setting value of the Addr+1. DB[15:8] must be 0x00

Note4: DB[7:0] represent the the setting value of the Addr+N. DB[15:8] must be 0x00

Note5: DB[7:0] send 0x80 to Disable the Register write. DB[15:8] must be 0x00

8.4 16Bit-80/68-Write to Display RAM



Note1: DB[15:0] send 0x000C1 to Enable the Display RAM write.

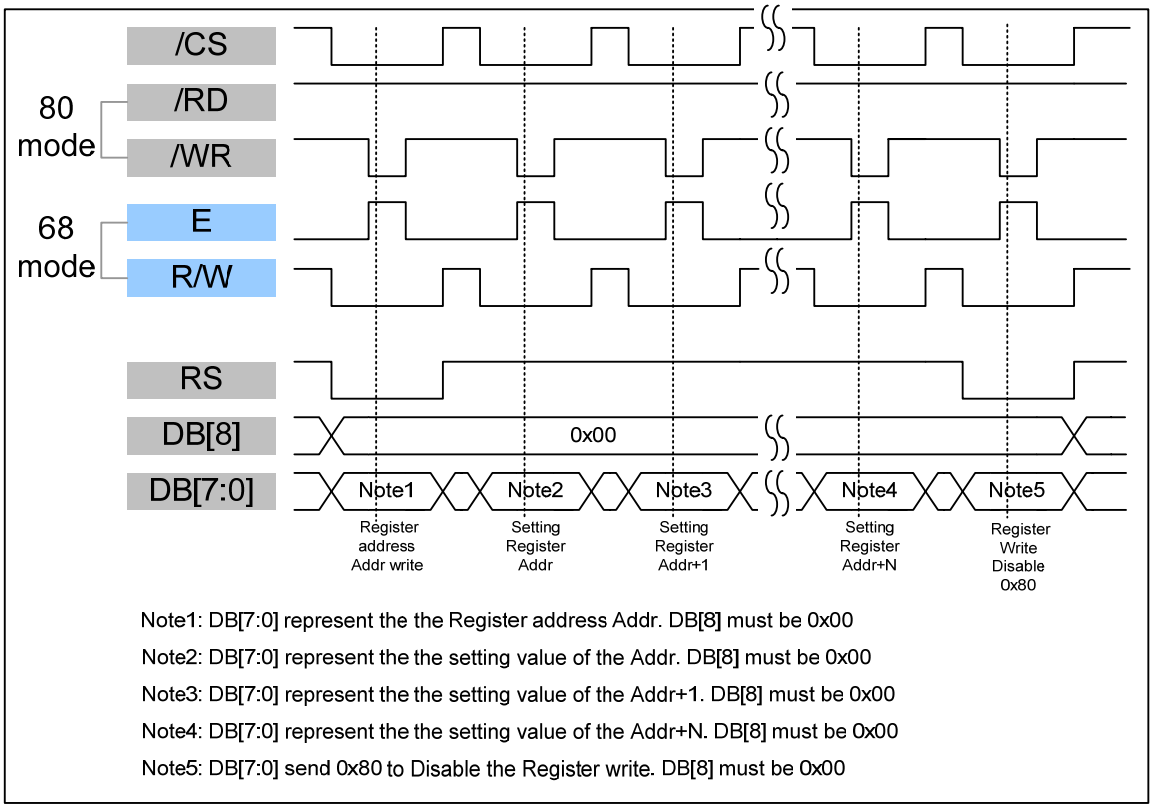
Note2: DB[15:0] represent the writing Data1 to Display RAM

Note3: DB[15:0] represent the writing Data2 to Display RAM

Note4: DB[15:0] represent the writing DataN to Display RAM

Note5: DB[15:0] send 0x00080 to Disable the Display RAM write.

8.5 9Bit-80/68- Write to Command Register



Note1: DB[7:0] represent the the Register address Addr. DB[8] must be 0x00

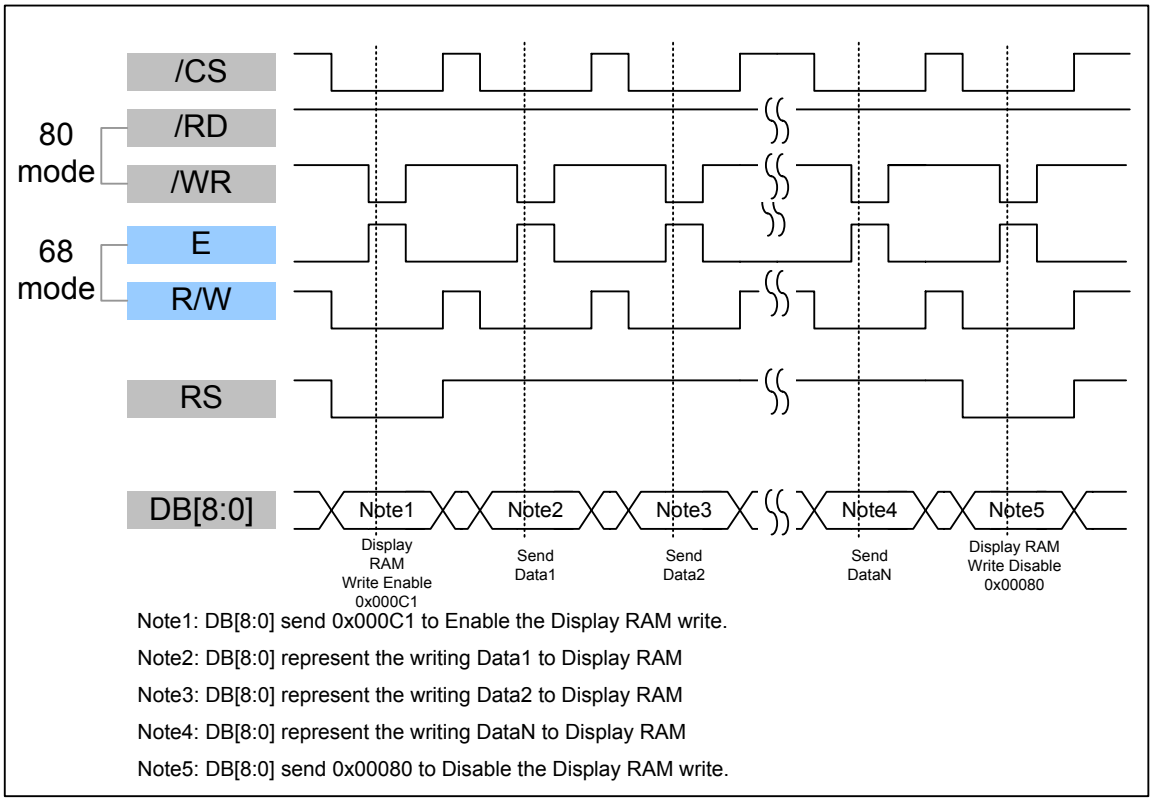
Note2: DB[7:0] represent the the setting value of the Addr. DB[8] must be 0x00

Note3: DB[7:0] represent the the setting value of the Addr+1. DB[8] must be 0x00

Note4: DB[7:0] represent the the setting value of the Addr+N. DB[8] must be 0x00

Note5: DB[7:0] send 0x80 to Disable the Register write. DB[8] must be 0x00

8.6 9Bit-80/68-Write to Display RAM



Note1: DB[8:0] send 0x000C1 to Enable the Display RAM write.

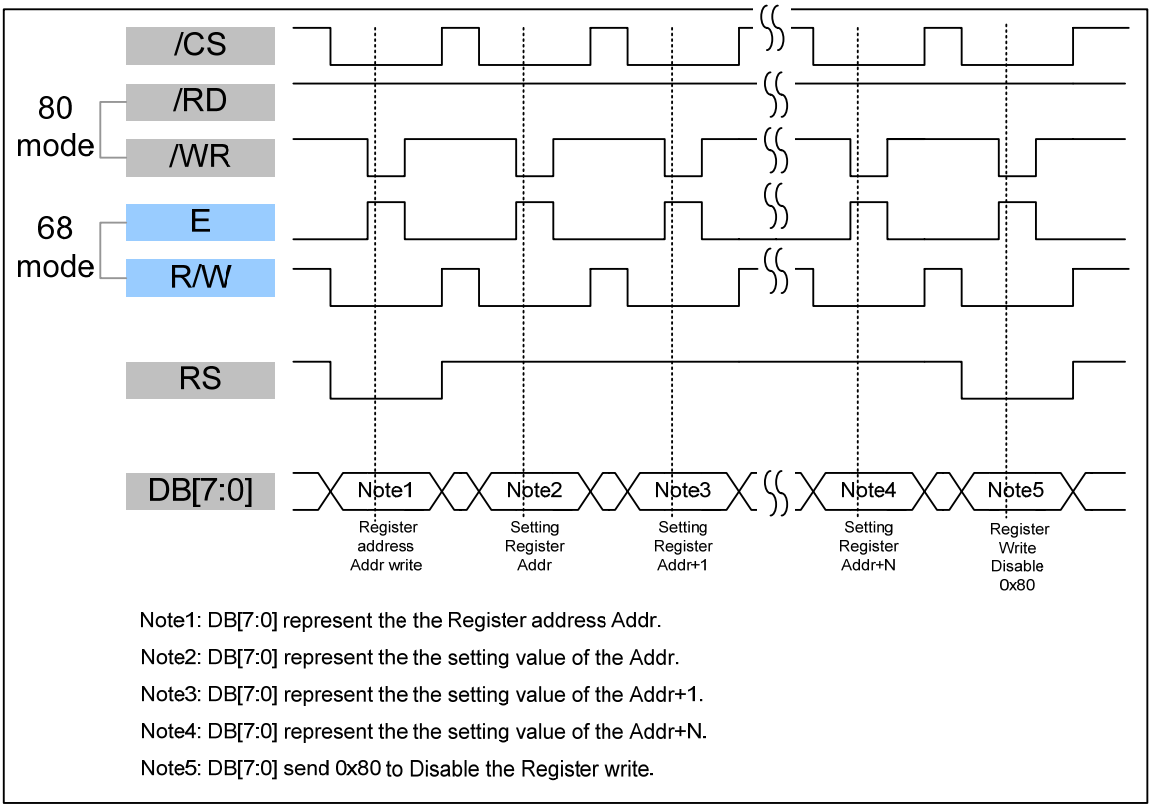
Note2: DB[8:0] represent the writing Data1 to Display RAM

Note3: DB[8:0] represent the writing Data2 to Display RAM

Note4: DB[8:0] represent the writing DataN to Display RAM

Note5: DB[8:0] send 0x00080 to Disable the Display RAM write.

8.7 8Bit-80/68- Write to Command Register



Note1: DB[7:0] represent the the Register address Addr.

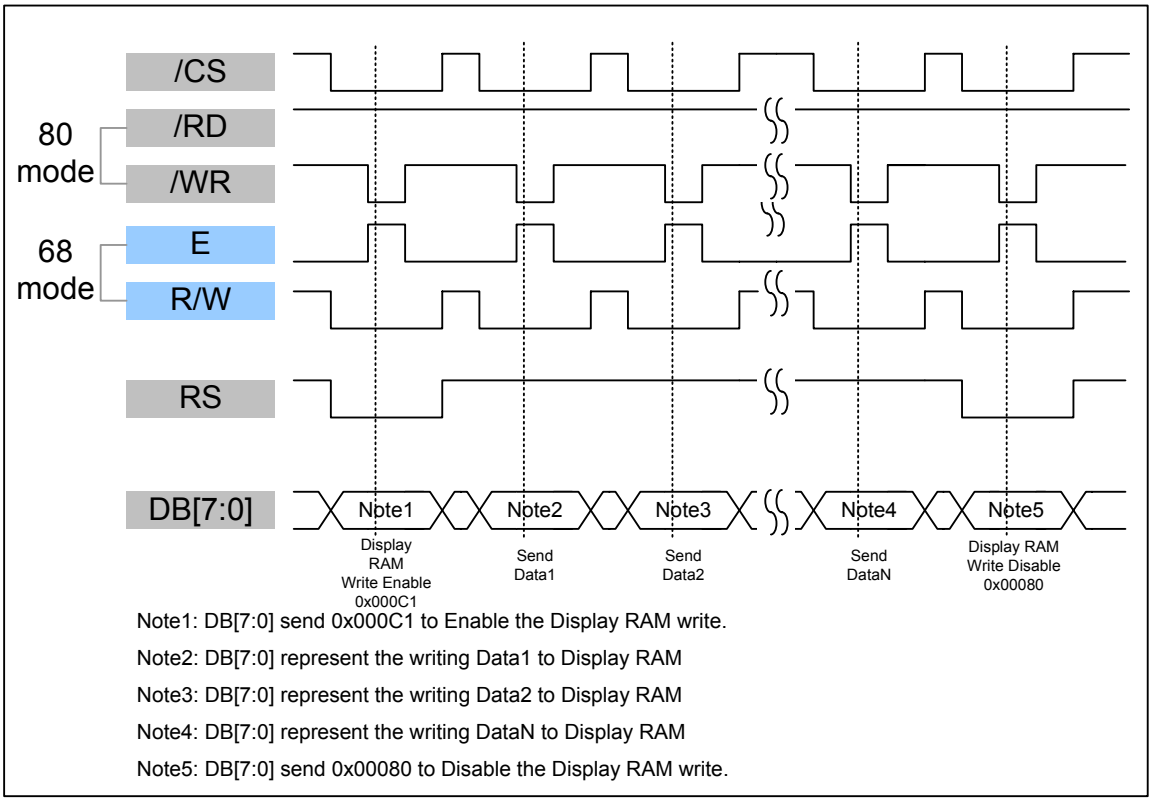
Note2: DB[7:0] represent the the setting value of the Addr.

Note3: DB[7:0] represent the the setting value of the Addr+1.

Note4: DB[7:0] represent the the setting value of the Addr+N.

Note5: DB[7:0] send 0x80 to Disable the Register write.

8.8 8Bit-80/68-Write to Display RAM



Note1: DB[7:0] send 0x000C1 to Enable the Display RAM write.

Note2: DB[7:0] represent the writing Data1 to Display RAM

Note3: DB[7:0] represent the writing Data2 to Display RAM

Note4: DB[7:0] represent the writing DataN to Display RAM

Note5: DB[7:0] send 0x00080 to Disable the Display RAM write.

8.9 Data transfer order Setting

8.9.1 18 bit interface 262K color only (Pin28 65K/262K =High)

DB	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

8.9.2 16 bit interface 65K color (Pin28 65K/262K =Low)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

8.9.3 16 bit interface 262K color (Pin28 65K/262K =High)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	X	X	X	X	X	X	X	X	X	X	X	X	X	X	R5	R4
2nd data	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

8.9.4 9 bit interface 262K color only (Pin28 65K/262K =High)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	X	X	X	X	X	X	X	R5	R4	R3	R2	R1	R0	G5	G4	G3
2nd data	X	X	X	X	X	X	X	G2	G1	G0	B5	B4	B3	B2	B1	B0

8.9.5 8 bit interface 65K color (Pin28 65K/262K =Low)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	X	X	X	X	X	X	X	X	R4	R3	R2	R1	R0	G5	G4	G3
2nd data	X	X	X	X	X	X	X	X	G2	G1	G0	B4	B3	B2	B1	B0

8.9.6 8 bit interface 262K color (Pin28 65K/262K =High)

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	X	X	X	X	X	X	X	X							R5	R4
2nd data	X	X	X	X	X	X	X	X	R3	R2	R1	R0	G5	G4	G3	G2
3rd data	X	X	X	X	X	X	X	X	G1	G0	B5	B4	B3	B2	B1	B0

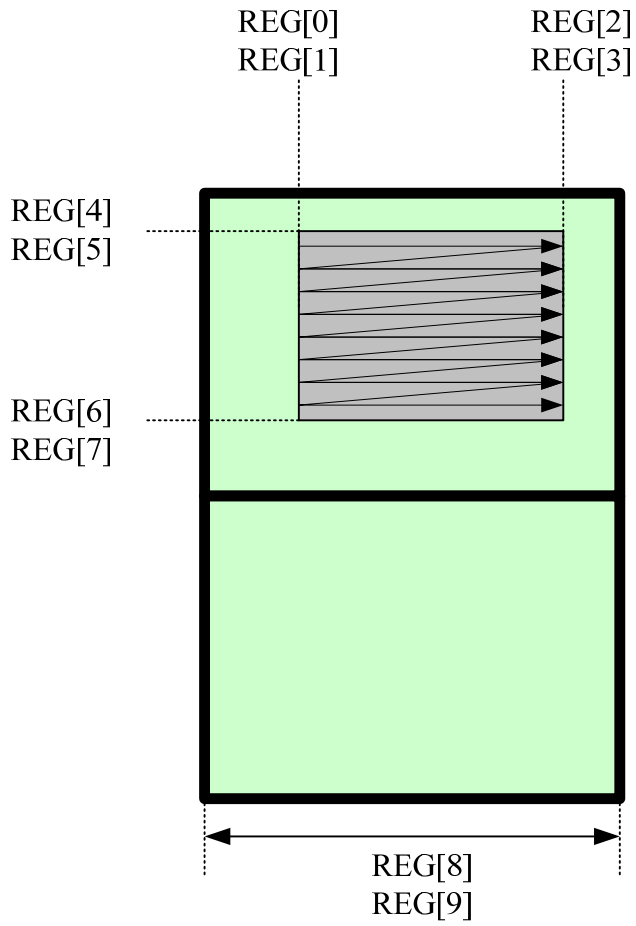
9 Register Depiction

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
00	00	MSB of X-axis start position								
Description	set the horizontals start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
01	00	LSB of X-axis start position								
Description	set the horizontals start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
02	01	MSB of X-axis end position								
Description	set the horizontals end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
03	3F	LSB of X-axis end position								
Description	set the horizontals end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
04	00	MSB of Y-axis start position								
Description	set the vertical start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
05	00	LSB of Y-axis start position								
Description	Set the vertical start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
06	00	MSB of Y-axis end position								
Description	set the vertical end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
07	EF	LSB of Y-axis end position								
Description	Set the vertical end position of display active region									

To simplify the address control of display RAM access, the window area address function allows for writing data only within a window area of display RAM specified by registers REG[00]~REG[07] .

After writing data to the display RAM, the Address counter will be increased within setting window address-range which is specified by

MIN X address (REG[0] & REG[1])
MAX X address (REG[2] & REG[3])
MIN Y address (REG[4] & REG[5])
MAX Y address (REG[6] & REG[7])
Therefore, data can be written consecutively without thinking the data address.



Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
08	01	X	X	X	X	X	X	_PanelXSize H_Byte[1:0]		
Description	Set the panel X size									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
09	40	_PanelXSize L_Byte[7:0]								
Description	Set the panel X size									

The register REG[08] and REG[09] is use to calculate the RAM address. If you want to use the TFT as Landscape mode (320x240), the REG[08] & RGE[09 must set to 320. If you want to use the TFT as Portrait mode (240x320), the REG[08] & RGE[09] must set to 240.

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0A	00	X	X	X	X	X	[17:16] bits of memory write start address			
Description	Memory write start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0B	00	[15:8] bits of memory write start address								
Description	Memory write start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0C	00	[7:0] bits of memory write start address								
Description	Memory write start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x10	0x0D	Bit_SWAP	OUT_TEST	BUS_SEL		Blanking	P/S_SEL	CLK_SEL		
Description	"0x10_Clk_sel[1:0]" : The TFT controller built-in 40Mhz PLL clock. These bits are for select the TFT panel dot clock frequency. 00 : 20Mhz 01: 10Mhz 02: 5 Mhz									
	"0x10_ps_sel[2]" : The TFT controller support parallel and serial RGB interface. These bits are for select the output timing. 0 : serial Panel 1: Parallel panel									
	"0x10_blanking_tmp[3]" 0 : OFF (blanking) 1: ON (normal operation)									
	"0x10_bus_sel[5:4]" : It only for serial Panel 00=R , 01=G , 10=B									
	"0x10_out_test[6]" : Self test 0 : normal operation 1: for test (don't use for normal operation) When set the bit to "1" , the Rout=(Reg 2a[6:0]) Gout=(Reg 2b[6:0]) Bout=(Reg 2c[6:0])									
	"0x10_bit_swap[7]" : 0-normal									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x11	00	X	X	EVEN			_ODD			
Description	" Even line of serial panel data out sequence or data bus order of parallel panel 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR Others: reserved Odd line of serial panel data out sequence 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG **101: BGR** Others: reserved **Must Set to 0x05**									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x12	00					Hsync_stH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync start position H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x13	00	Hsync_stL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync start position L-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x14	00					Hsync_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync pulse width H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x15	10	Hsync_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync pulse width L-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x16	00					Hact_stH_Byte[3:0]				
Description	For TFT output timing adjust: DE pulse start position H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x17	38	Hact_stL_Byte[7:0]								
Description	For TFT output timing adjust: DE pulse start position L-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x18	01					Hact_pwH_Byte[3:0]				
Description	For TFT output timing adjust: DE pulse width H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x19	40	Hact_pwL_Byte[7:0]								
Description	For TFT output timing adjust: DE pulse width L-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1A	01					HtotalH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync total clocks H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1B	B8	HtotalL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync total clocks H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1C	00					Vsync_stH_Byte[3:0]				
Description	For TFT output timing adjust: Vsync start position H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1D	00	Vsync_stL_Byte[7:0]								
Description	For TFT output timing adjust: Vsync start position L-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1E	00					Vsync_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Vsync pulse width H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1F	08	Vsync_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Vsync pulse width L-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x20	00					Vact_stH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical DE pulse start position H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x21	12	Vact_stL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical DE pulse start position L-Byte									

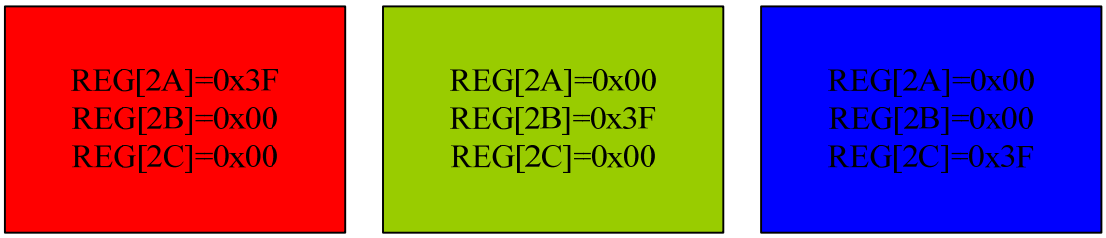
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x22	00					Vact_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical Active width H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x23	F0	Vact_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical Active width H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x24	01					VtotalH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical total width H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x25	09	VtotalL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical total width L-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
26	00	X	X	X	X	X	[17:16] bits of memory read start address			
Description	Memory read start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
27	00	[15:8] bits of memory write start address								
Description	Memory read start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
28	00	[7:0] bits of memory write start address								
Description	Memory read start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
29	00	[7:1] Reversed								
Description	[0] Load output timing related setting (H sync., V sync. and DE) to take effect									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2A	00	X	TestPatternRout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Rout data equal to TestPatternRout[6:0]									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2B	00	X	TestPatternGout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Gout data equal to TestPatternGout[6:0]									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2C	00	X	TestPatternBout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Bout data equal to TestPatternBout[6:0]									

If you set the " REG[0x10]_out_test[6]" : Self test =1 , the TFT controller will skip the connect of the display RAM. The Output port will send the REG[2A] ,REG[2B],REG[2C] data.



Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2D	00	X	X	X	X	[3]	Rising/falling edge[2]	_rotate [1:0]		
Description	[3] Output pin X_DCON level control ; TFT Power ON/OFF control 0: TFT POWER circuit OFF 1: TFT POWER circuit ON									
	Rising/falling edge[2] : 0: The RGB out put data are on the Rising edge of the DCLK. 1: The RGB out put data are on the Falling edge of the DCLK.									
	_rotate [1:0]: 00 : rotate 0 degree 01 : rotate90 degree 10 : rotate 270 degree 11 : rotate 180 degree									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
30	00	X	X	X	X	X	_H byte H-Offset[3:0]			
Description	Set the Horizontal offset									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
31	00	_L byte H-Offset[7:0]								
Description	Set the Horizontal offset									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
32	00	X	X	X	X	X	_H byte V-Offset[3:0]			
Description	Set the Vertical offset									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
33	00	_L byte V-Offset[7:0]								
Description	Set the Vertical offset									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
34	00	[7:4] Reserved					_H byte H-def[3:0]			
Description	[3:0] MSB of image horizontal physical resolution in memory									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
35	40	_L byte H-def[7:0]								
Description	[7:0] LSB of image horizontal physical resolution in memory									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
36	01	[7:4] Reserved					_H byte V-def[3:0]			
Description	[3:0] MSB of image vertical physical resolution in memory									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
37	E0	_L byte V-def[7:0]								
Description	[7:0] LSB of image vertical physical resolution in memory									

The total RAM size is 640x240x18bit. The user can arrange the Horizontal ram size by REG[34],REG[35] and the Vertical ram size by REG[36],REG[37].
EX: 320x480x18bit REG[34]=0x01 , REG[35]=0x40 , REG[36]=0x01 , REG[37]=0xE0
EX: 640x240x18bit. REG[34]=0x02 , REG[35]=0x80 , REG[36]=0x00 , REG[37]=0xF0

DISPLAYED COLOR AND INPUT DATA

	Color & Gray Scale	DATA SIGNAL																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(61)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(31)	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(1)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(61)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(31)	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(1)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(0)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(31)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

10 QUALITY AND RELIABILITY

10.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : 25 ± 5°C

Humidity : 60 ± 25% RH.

10.2 SAMPLING PLAN

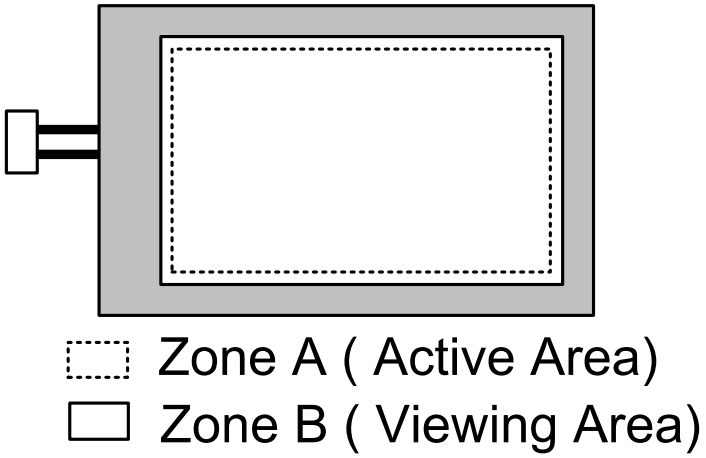
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

10.3 ACCEPTABLE QUALITY LEVEL

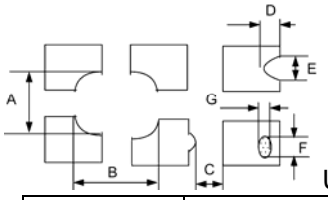
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

10.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the AMOLED module under flourescent light. The inspection area of AMOLED panel shall be within the range of following limits.

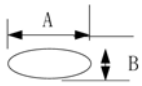


10.5 INSPECTION QUALITY CRITERIA

<table>
<tr><th>No.</th><th>Item</th><th>Criterion for defects</th><th>Class of Defect</th><th>Acceptable level</th></tr>
<tr><td>1</td><td>Non display</td><td>No non display is allowed</td><td>Major</td><td>0.4</td></tr>
<tr><td>2</td><td>Irregular operation</td><td>No irregular operation is allowed</td><td>Major</td><td>0.4</td></tr>
<tr><td>3</td><td>Short</td><td>No short are allowed</td><td>Major</td><td>0.4</td></tr>
<tr><td>4</td><td>Open</td><td>Any segments or common patterns that don't activate are rejectable.</td><td>Major</td><td>0.4</td></tr>
<tr><td>5</td><td>Black/White spot (I)</td><td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.1</td><td>Ignore</td></tr>
<tr><td>0.1 < D ≤ 0.15</td><td>2 ※1</td></tr>
<tr><td>0.15 < D</td><td>0</td></tr>
</table>
※1: The distance of two defects must be more than 20mm.
</td><td>Minor</td><td>1.5</td></tr>
<tr><td>6</td><td>Dot Defect</td><td>
<table>
<tr><td>Bright dot</td><td>1</td></tr>
<tr><td>Dark dot</td><td>N≦3</td></tr>
<tr><td>Total dot defect
(Bright dot + Dark dot)</td><td>N≦4</td></tr>
<tr><td>Minimum distance between dark dot and dark dot</td><td>0.1＜D≦0.3mm,N≦2</td></tr>
</table>
</td><td>Minor</td><td>1.5</td></tr>
<tr><td>7</td><td>Back Light</td><td>1. No Lighting is rejectable
2. Flickering and abnormal lighting are rejectable</td><td>Major</td><td>0.4</td></tr>
<tr><td>8</td><td>Display pattern</td><td>


Unit:mm
<table>
<tr><td>$\frac{A+B}{2} \le 0.30$</td><td>0 < C</td><td>$\frac{D+E}{2} \le 0.25$</td><td>$\frac{F+G}{2} \le 0.25$</td></tr>
</table>
Note: 1. Acceptable up to 3 damages
2. NG if there're to two or more pinholes per dot
</td><td>Minor</td><td>1.5</td></tr>
<tr><td>9</td><td>Blemish & Foreign matters

Size:
$D = \frac{A+B}{2}$</td><td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.15</td><td>Ignore</td></tr>
<tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr>
<tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr>
<tr><td>0.30 < D</td><td>0</td></tr>
</table>
</td><td>Minor</td><td>1.5</td></tr>
</table>

<table>
<tr><td>10</td><td>Scratch on Polarizer
  </td><td><table><tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr><tr><td>W≤0.03</td><td>L ≤ 2.0</td><td>2</td></tr></table>Note: The distance of two defects must be more than 20mm.</td><td>Minor</td><td>1.5</td></tr>
<tr><td>11</td><td>Bubble in polarizer</td><td>Zone A Active area : No bubble are allowed.
Zone B Viewing area: ≤ 0.05mm^2, N≤ 1</td><td>Minor</td><td>1.5</td></tr>
<tr><td>12</td><td>Stains on LCD panel surface</td><td>Stains that cannot be removed even when wiped lightly with a soft cloth or similar cleaning too are rejectable.</td><td>Minor</td><td>1.5</td></tr>
<tr><td>13</td><td>Rust in Bezel</td><td>Rust which is visible in the bezel is rejectable.</td><td>Minor</td><td>1.5</td></tr>
<tr><td>14</td><td>Defect of land surface contact (poor soldering)</td><td>Evident crevices which is visible are rejectable.</td><td>Minor</td><td>1.5</td></tr>
<tr><td>15</td><td>Parts mounting</td><td>1. Failure to mount parts
2. Parts not in the specifications are mounted
3. Polarity, for example, is reversed</td><td>Major
Major
Major</td><td>0.4</td></tr>
<tr><td>16</td><td>Parts alignment</td><td>1. LSI, IC lead width is more than 50% beyond pad outline.
2. Chip component is off center and more than 50% of the leads is off the pad outline.</td><td>Minor
Minor</td><td>1.5</td></tr>
<tr><td>17</td><td>Conductive foreign matter (Solder ball, Solder chips)</td><td>1. 0.45<φ ,N≧1
2. 0.30<φ≤0.45 ,N≧1
φ:Average diameter of solder ball (unit: mm)
3. 0.50<L ,N≧1
L: Average length of solder chip (unit: mm)</td><td>Major
Minor

Minor</td><td>0.4
1.5

1.5</td></tr>
<tr><td>18</td><td>Faulty PCB correction</td><td>1. Due to PCB copper foil pattern burnout, the pattern is connected, using a jumper wire for repair; 2 or more places are corrected per PCB.
2. Short circuited part is cut, and no resist coating has been performed.</td><td>Minor
Minor</td><td>1.5</td></tr>
</table>

11 RELIABILITY TEST CONDITIONS

ITEM	CONDITIONS	NOTE
HIGH TEMPERATURE OPERATION	60℃ , 240Hrs	
HIGH TEMPERATURE AND HIGH HUMIDITY OPERATION	60℃ , 90%RH , 240Hrs	
HIGH TEMPERATURE STORAGE	85℃ , 240Hrs	
LOW TEMPERATURE OPERATION	-20℃ , 240Hrs	
LOW TEMPERATURE STORAGE	-30℃ , 240Hrs	
THERMAL SHOCK	-30℃(1Hr) ~80℃(1Hr) 100Cycle	

12 USE PRECAUTIONS

12.1 Handling precautions

1) The AMOLED plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the AMOLED plate surface with bare hands so as not to make it dirty. If the surface or other related part of the AMOLED plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.

12.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack AMOLED and cause circuit failure.
3) To protect AMOLED, especially AMOLED plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make AMOLED surface (AMOLED plate) and product case stick together. Failure to do so may cause the AMOLED plate to peel off.

12.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

12.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the AMOLED module controller before removing or inserting the AMOLED module input connector. If the input connector is removed or inserted while the power is turned on, the AMOLED module internal circuit may break.
2) The AMOLED contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the AMOLED dive voltage.
3) When carrying out the test, do not take the module out of the low-temperature space

suddenly. Failure to do so will cause the module condensing, leading to malfunctions.

4) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
5) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
6) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the AMOLED may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

12.5 Other

1) Do not disassemble or take the AMOLED module into pieces. The AMOLED modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

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