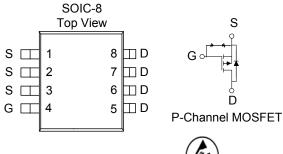
P-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

•	Low r _{DS(on)} provides higher efficiency and
	extends battery life

- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY				
V _{DS} (V)	$I_{D}(A)$			
-30	$13 @ V_{GS} = -10V$	-11.5		
-30	$19 @ V_{GS} = -4.5V$	-9.3		



ESD Protected 3000 V

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)						
Paramete r	Symbol	Maximum	Units			
Drain-Source Voltage			-30	V		
Gate-Source Voltage	V_{GS}	±25	V			
Continuous Drain Current ^a	$T_A=25^{\circ}C$	I.	-11.5			
Continuous Drain Current	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	1D	-9.3	A		
Pulsed Drain Current ^b	I_{DM}	±50				
Continuous Source Current (Diode Conduction) ^a	I_S	-2.1	A			
D	$T_A=25^{\circ}C$	D_	3.1	W		
Power Dissipation ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	Гр	2.3	**		
Operating Junction and Storage Temperature Range	T_{J}, T_{stg}	-55 to 150	°C			

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Maximum	Units			
Maximum Junction-to-Case ^a	t <= 5 sec	$R_{ heta JC}$	25	°C/W		
Maximum Junction-to-Ambient ^a	t <= 5 sec	$R_{\theta JA}$	50	°C/W		

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Dovamator	Sambol	Toot Conditions	Limits			4	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = -250 \text{ uA}$	-30			\ \	
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \text{ uA}$	-1]	
Gate-Body Leakage	I _{GSS}	V _{DS} =0 V, V _{GS} =±25 V			±1	uA	
Zero Gate Voltage Drain Current	L	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uΑ	
Zao Cale Vollage Dan Curra II.	l _{DSS}	$V_{DS} = -24 \text{ V}, V_{CS} = 0 \text{ V}, T_J = 55^{\circ}\text{C}$			-5	uA	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-50			Α	
Danier Courses On Designation of	_	$V_{GS} = -10 \text{ V}, I_D = -11.5 \text{ A}$			13	mΩ	
Drain-Source On-Resistance ^A	r _{DS(on)}	$V_{GS} = -4.5 \text{ V}, I_D = -9.3 \text{ A}$			19.0	1162	
Forward Tranconductance ^A	9 _{fs}	$V_{DS} = -15 \text{ V}, I_D = -11.5 \text{ A}$		29		S	
Diode Forward Voltage	V_{SD}	I _S = 2.5 A, V _{GS} = 0 V		-0.8		V	
Dynamic ^b							
Total Gate Charge	Q_g	$V_{DS} = -15 \text{ V}, V_{GS} = -5 \text{ V},$		25			
Gate-Source Charge	Qgs	$V_{DS} = -15 \text{ V}, V_{GS} = -5 \text{ V},$ $I_{D} = -11.5 \text{ A}$		11		nC	
Gate-Drain Charge	Q_{gd}	I _D = -11.5 A		17		1	
Input Capacitance	Gss			2300			
Output Capacitance	Coss	V_{DS} =-15V, V_{GS} =0V, f=1MHz		600		pF	
Reverse Transfer Capacitance	C _{rss}			300		Ī	
Turn-On Delay Time	t _{d(on)}			15			
Rise Time	t _r	$V_{DD} = -15 V, R_L = 6 \Omega$,		13		nS	
Tum-Off Delay Time	t _{d(off)}	ID=-1 A, VGEN=-10 V		100			
Fall-Time	t _f			54		Ī	

Notes

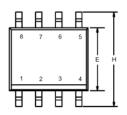
- a. Pulse test: $PW \le 300us duty cycle \le 2\%$.
- b. Guaranteed by design, not subject to production testing.

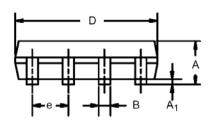
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Package Information

SO-8: 8LEAD





	MILLIM	IETERS	INC	HES
Dim	Min	Max	Min	Max
Α	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
В	0.35	0.51	0.014	0.020
С	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
е	1.27	BSC	0.050	BSC
Н	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°

