PRELIMINARY

Am486® DX2 3.3-Volt Processor

High-Performance, Clock-Doubled, 32-Bit Microprocessor

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Operating voltage range 3.3 V ± 0.3 V**
  - — 66-MHz and 80-MHz operating frequencies
  - — Wide range of chipsets and support available through the AMD® FusionPC℠ Program
- **High Integration On-Chip**
  - — 8-Kbyte code and data cache
  - — Floating-point unit
  - — Paged, virtual memory management
- **High-Performance Design**
  - — Frequent instructions execute in one clock
  - — 105.6-million bytes/second burst bus at 33 MHz
  - — 128-million bytes/second burst bus at 40 MHz
  - — Advanced submicron CMOS technology
  - — Dynamic bus sizing for 8-, 16-, and 32-bit buses
- **Complete 32-Bit Architecture**
  - — Address and data buses
  - — All registers
  - — 8-, 16-, and 32-bit data types
- **Multiprocessor Support**
  - — Multiprocessor instructions
  - — Cache consistency protocols
  - — Support for second-level cache
- **Standard 168-pin PGA Package**
- **Environmental Protection Agency's "Energy Star" program compliant**
  - — Energy management capability provides an excellent base for energy-efficient design
  - — Works with a variety of energy-efficient, power-managed devices

GENERAL DESCRIPTION

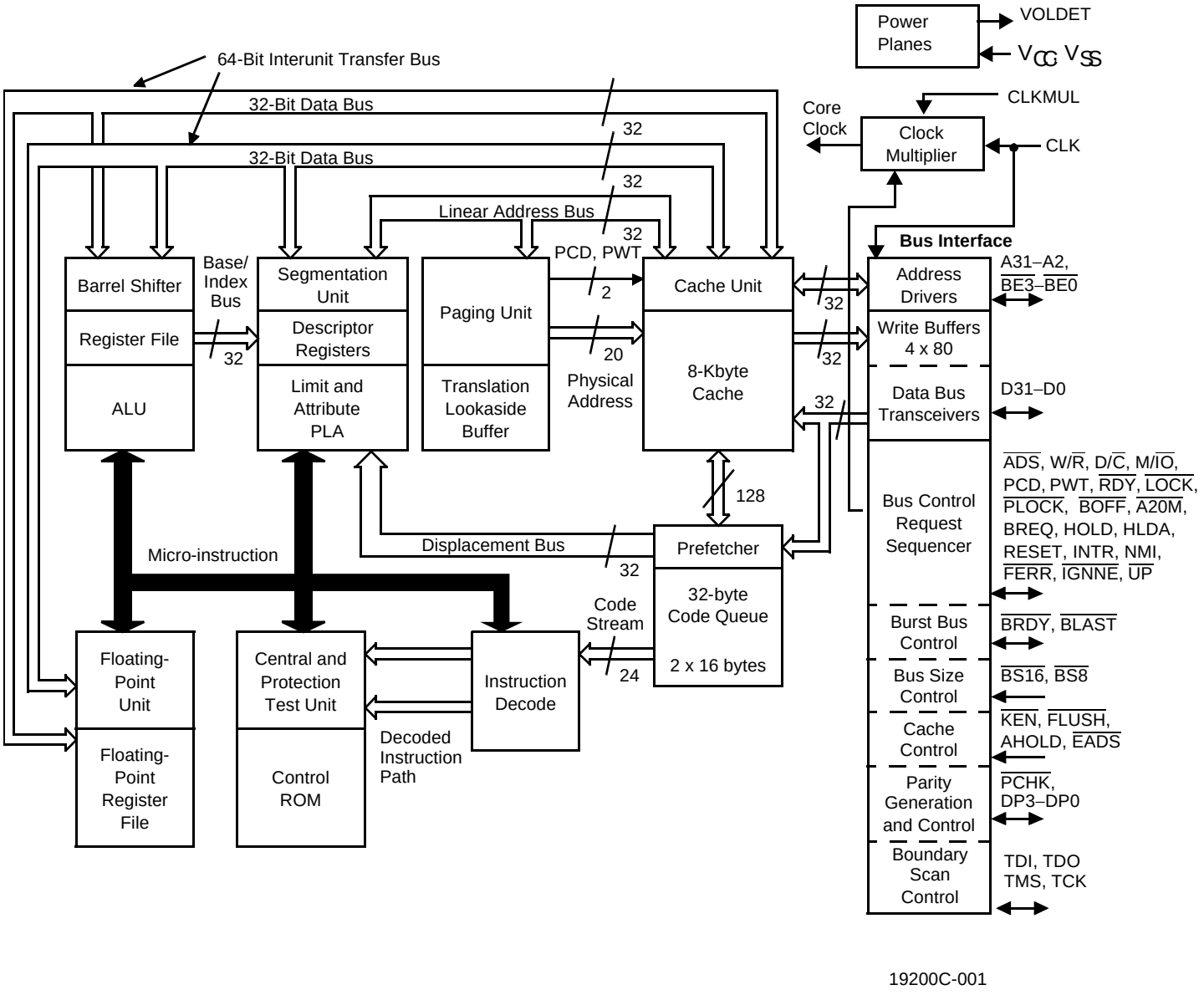
The clock-doubled Am486DX2 processor is a high-performance 486 desktop solution that provides optimal price/performance for high-end 486 power-managed systems. The Am486DX2 CPU offers superior local bus graphics performance for Microsoft® Windows®.

The Am486DX2 processor operates with a 1x clock input. This 1x clock simplifies system design by reducing the clock frequency required by external devices. The 1x clock also reduces RF emission and simplifies clock generation. The input signal is doubled internally to achieve the maximum 2x operating frequency. The phases of the core clock are controlled by an internal Phase Lock Loop (PLL) circuit.

Publication# **19200** Rev: **D** Amendment/**0**
Issue Date: **August 1995**

BLOCK DIAGRAM

Am486 CPU Pipelined 32-Bit Microarchitecture

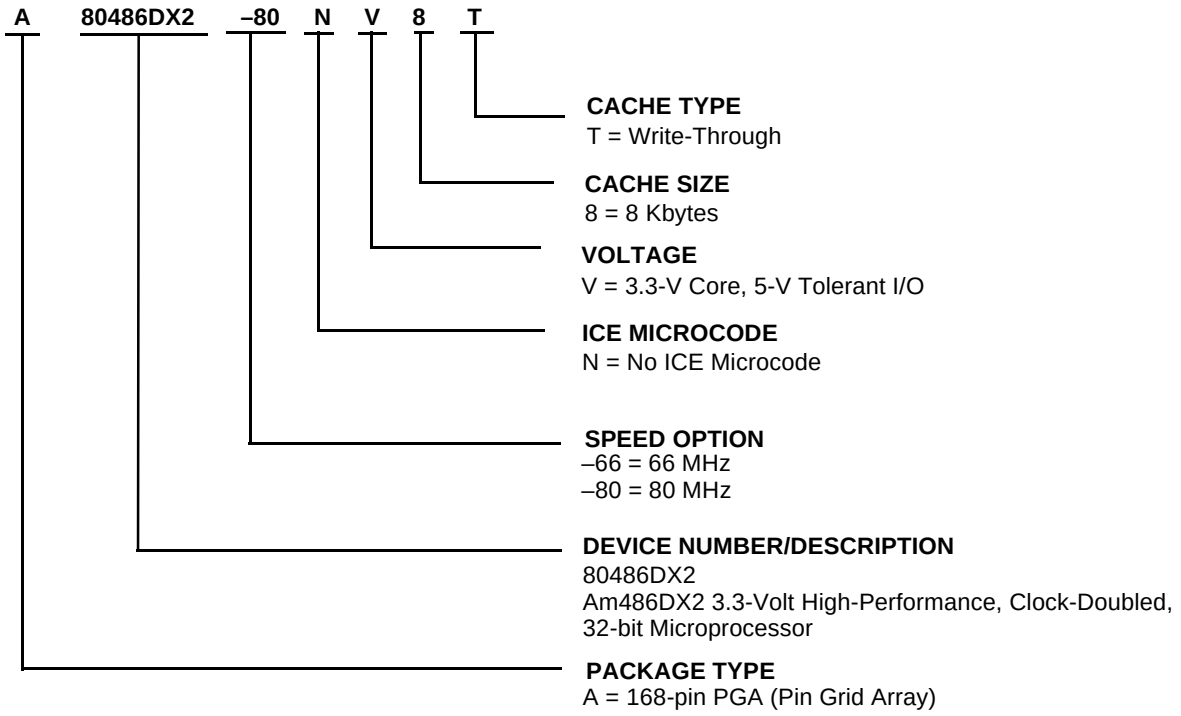


19200C-001

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations			
A	80486DX2	-66 -80	NV8T

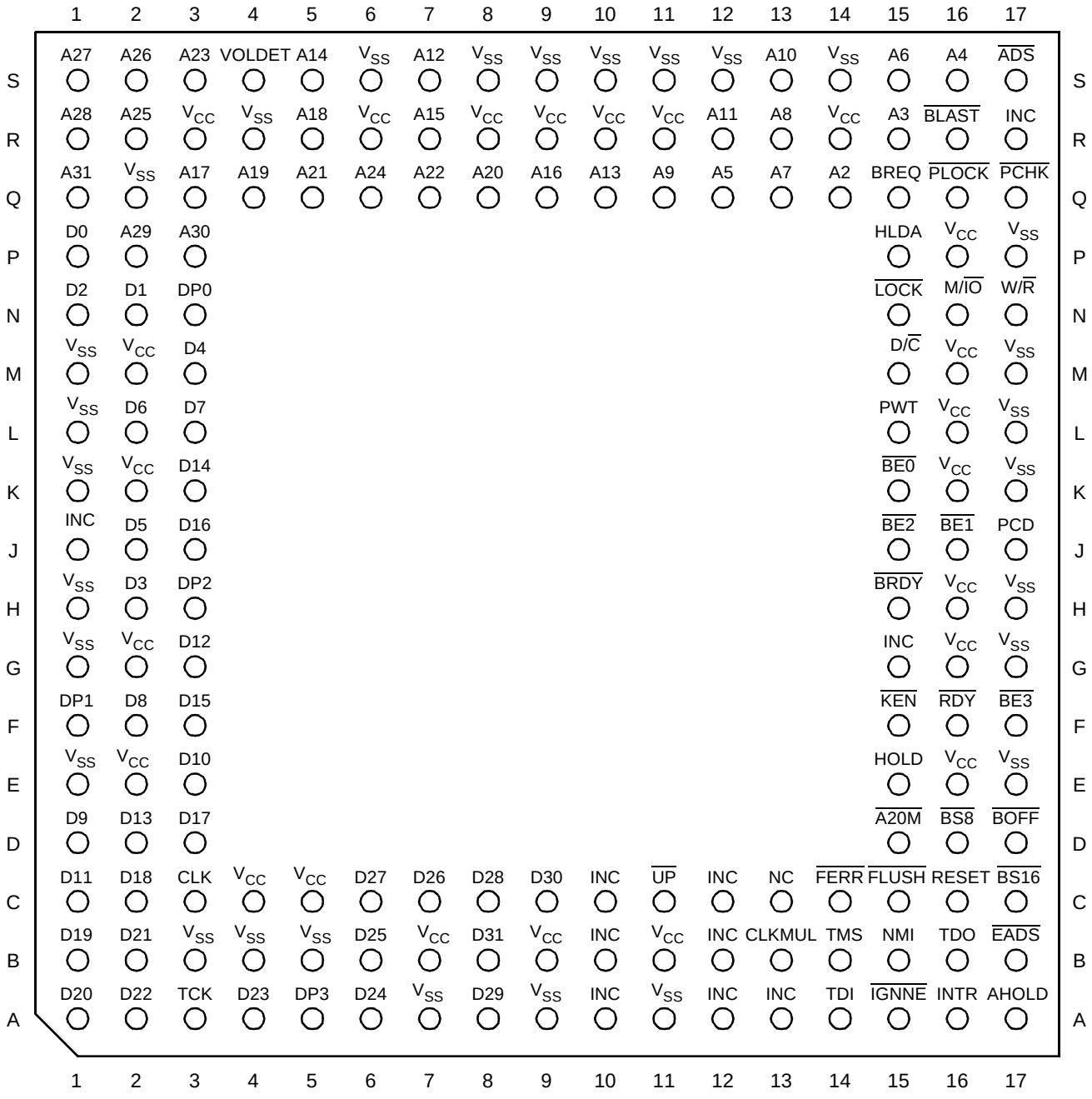
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

CONNECTION DIAGRAMS

Am486DX2 CPU
Pin Side View

168-Pin PGA (Pin Grid Array) Package



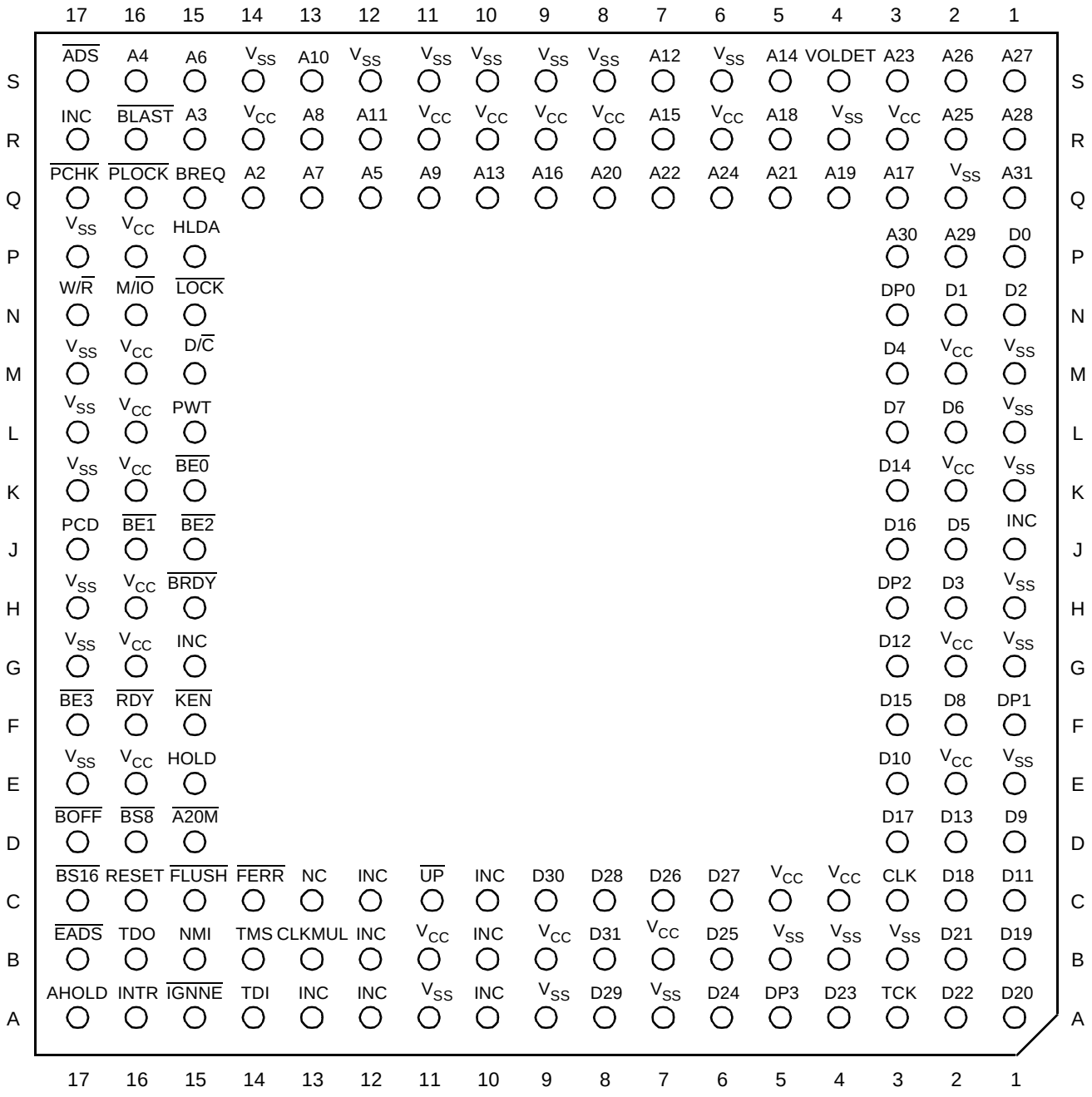
Note:
NC = No Connect. To guarantee functionality with future revisions, these pins must not be connected.
INC = Internal No Connect. No special requirements.

19200C-002

CONNECTION DIAGRAMS

Am486DX2 CPU
Top Side View

168-Pin PGA (Pin Grid Array) Package



Note:
NC = No Connect. To guarantee functionality with future revisions, these pins must not be connected.
INC = Internal No Connect. No special requirements.

19200C-003

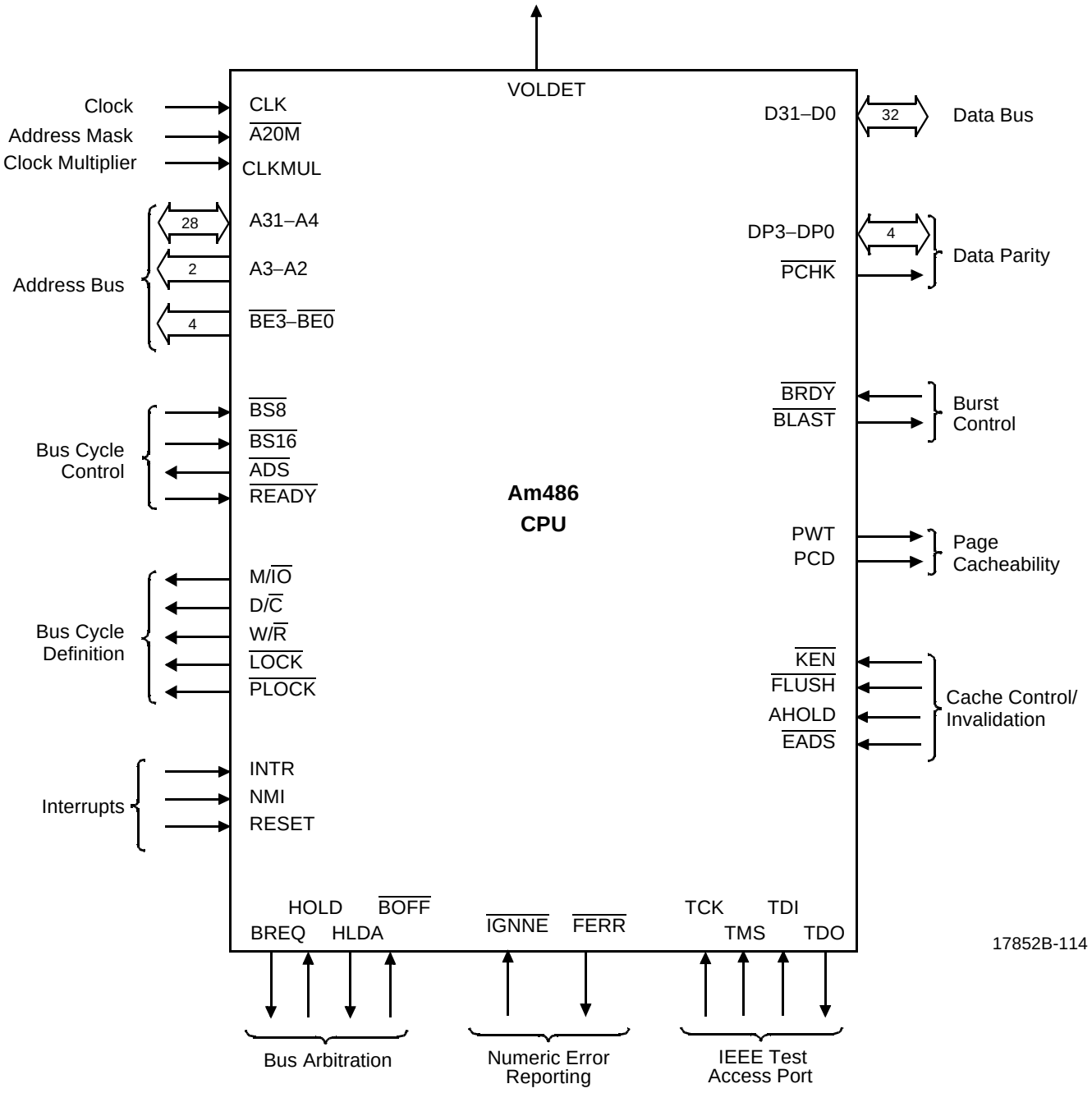
PIN DESIGNATIONS (Functional Grouping)

Address		Data		Control		Test		INC/NC	V_{CC}	V_{SS}
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin No.	Pin No.	Pin No.
A2	Q-14	**D0**	P-1	**$\overline{A20M}$**	D-15	**TCK**	A-3	A-10	B-7	A-7
A3	R-15	**D1**	N-2	**$\overline{ADS}$**	S-17	**TDI**	A-14	A-12	B-9	A-9
A4	S-16	**D2**	N-1	**AHOLD**	A-17	**TDO**	B-16	A-13	B-11	A-11
A5	Q-12	**D3**	H-2	**$\overline{BE0}$**	K-15	**TMS**	B-14	B-10	C-4	B-3
A6	S-15	**D4**	M-3	**$\overline{BE1}$**	J-16			B-12	C-5	B-4
A7	Q-13	**D5**	J-2	**$\overline{BE2}$**	J-15			C-10	E-2	B-5
A8	R-13	**D6**	L-2	**$\overline{BE3}$**	F-17			C-12	E-16	E-1
A9	Q-11	**D7**	L-3	**$\overline{BLAST}$**	R-16			C-13	G-2	E-17
A10	S-13	**D8**	F-2	**$\overline{BOFF}$**	D-17			G-15	G-16	G-1
A11	R-12	**D9**	D-1	**$\overline{BRDY}$**	H-15			J-1	H-16	G-17
A12	S-7	**D10**	E-3	**BREQ**	Q-15			R-17	K-2	H-1
A13	Q-10	**D11**	C-1	**$\overline{BS8}$**	D-16				K-16	H-17
A14	S-5	**D12**	G-3	**$\overline{BS16}$**	C-17				L-16	K-1
A15	R-7	**D13**	D-2	**CLK**	C-3				M-2	K-17
A16	Q-9	**D14**	K-3	**CLKMUL**	B-13				M-16	L-1
A17	Q-3	**D15**	F-3	**D/$\overline{C}$**	M-15				P-16	L-17
A18	R-5	**D16**	J-3	**DP0**	N-3				R-3	M-1
A19	Q-4	**D17**	D-3	**DP1**	F-1				R-6	M-17
A20	Q-8	**D18**	C-2	**DP2**	H-3				R-8	P-17
A21	Q-5	**D19**	B-1	**DP3**	A-5				R-9	Q-2
A22	Q-7	**D20**	A-1	**$\overline{EADS}$**	B-17				R-10	R-4
A23	S-3	**D21**	B-2	**$\overline{FERR}$**	C-14				R-11	S-6
A24	Q-6	**D22**	A-2	**$\overline{FLUSH}$**	C-15				R-14	S-8
A25	R-2	**D23**	A-4	**HLDA**	P-15					S-9
A26	S-2	**D24**	A-6	**HOLD**	E-15					S-10
A27	S-1	**D25**	B-6	**$\overline{IGNNE}$**	A-15					S-11
A28	R-1	**D26**	C-7	**INTR**	A-16					S-12
A29	P-2	**D27**	C-6	**$\overline{KEN}$**	F-15					S-14
A30	P-3	**D28**	C-8	**$\overline{LOCK}$**	N-15					
A31	Q-1	**D29**	A-8	**M/$\overline{IO}$**	N-16					
		D30	C-9	**NMI**	B-15					
		D31	B-8	**PCD**	J-17					
				$\overline{PCHK}$	Q-17					
				PWT	L-15					
				$\overline{PLOCK}$	Q-16					
				$\overline{RDY}$	F-16					
				RESET	C-16					
				$\overline{UP}$	C-11					
				VOLDET	S-4					
				W/$\overline{R}$	N-17					

Notes:

INC = Internal No Connect (A-10, A-12, A-13, B-10, B-12, C-10, C-12, G-15, J-1, R-17).
NC = No Connect (C-13).
VOLDET is connected internally to V_{SS}.
*CLKMUL **must** be connected externally to V_{SS}*

LOGIC SYMBOL



PIN DESCRIPTIONS

The following paragraphs define the Am486DX2 CPU pins (signals).

A31–A4/A3–A2

Address Lines (Inputs/Outputs)/(Outputs)

A31–A2, together with the byte enables $\overline{BE3}$–$\overline{BE0}$, define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the microprocessor to perform cache line invalidations. Input signals must meet setup and hold times t_{22} and t_{23}. A31–A2 are not driven during bus or address hold.

$\overline{A20M}$

Address Bit 20 Mask (Active Low; Input)

When asserted, the Am486DX2 microprocessor masks physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. $\overline{A20M}$ emulates the address wraparound at 1 Mbyte, which occurs on the 8086. $\overline{A20M}$ is active Low and should be asserted only when the processor is in Real mode. This pin is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, $\overline{A20M}$ should be sampled High at the falling edge of RESET.

$\overline{ADS}$

Address Status (Active Low; Output)

$\overline{ADS}$ indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. $\overline{ADS}$ is driven active in the same clock as the addresses are driven. $\overline{ADS}$ is active Low and is not driven during bus hold.

AHOLD

Address Hold (Active High; Input)

This request allows another bus master access to the Am486DX2 microprocessor's address bus for a cache invalidation cycle. The Am486DX2 microprocessor stops driving its address bus in the clock following AHOLD going active. Only the address bus is floated during address hold; the remainder of the bus remains active. AHOLD is active High and is provided with a small internal pull-down resistor. For proper operation, AHOLD must meet setup and hold times t_{18} and t_{19}.

$\overline{BE3}$–$\overline{BE0}$

Byte Enables (Active Low; Outputs)

These pins indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. $\overline{BE3}$ applies to D31–D24, $\overline{BE2}$ applies to D23–D16, $\overline{BE1}$ applies to D15–D8, and $\overline{BE0}$ applies to D7–D0. $\overline{BE3}$–$\overline{BE0}$ are active Low and are not driven during bus hold.

The Am486DX2 microprocessor provides four special bus cycles to indicate that certain instructions have been executed, or certain conditions have occurred internally. The special bus cycles (in Table 1) are defined when the bus cycle definition pins are in the following state: M/$\overline{IO}$=0, D/$\overline{C}$=0, and W/$\overline{R}$=1. During these cycles, the address bus is driven Low while the data bus is undefined.

The external hardware must acknowledge these special bus cycles by returning $\overline{RDY}$ and $\overline{BRDY}$.

Table 1. Special Bus Cycle Encoding

$\overline{BE3}$	$\overline{BE2}$	$\overline{BE1}$	$\overline{BE0}$	Special Bus Cycles
1	1	1	0	Shutdown
1	1	0	1	Flush
1	0	1	1	Halt
0	1	1	1	Write Back

$\overline{BS8}$/$\overline{BS16}$

Bus Size 8 (Active Low; Input)/
Bus Size 16 (Active Low; Input)

These pins cause the Am486DX2 microprocessor to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The state of these pins in the clock before $\overline{RDY}$ is used by the Am486DX2 microprocessor to determine the bus size. These signals are active Low and are provided with internal pull-up resistors. These inputs must satisfy setup and hold times t_{14} and t_{15} for proper operation.

$\overline{BLAST}$

Burst Last (Active Low; Output)

$\overline{BLAST}$ indicates that the next time $\overline{BRDY}$ is returned, the burst bus cycle is complete. $\overline{BLAST}$ is active for both burst and non-burst bus cycles. $\overline{BLAST}$ is active Low and is not driven during bus hold.

$\overline{BOFF}$

Backoff (Active Low; Input)

This input pin forces the Am486DX2 microprocessor to float its bus in the next clock. The microprocessor floats all pins normally floated during bus hold, but HLDA is not asserted in response to $\overline{BOFF}$. $\overline{BOFF}$ has higher priority than $\overline{RDY}$ or $\overline{BRDY}$; if both are returned in the same clock, $\overline{BOFF}$ takes effect. The microprocessor remains in bus hold until $\overline{BOFF}$ is negated. If a bus cycle is in progress when $\overline{BOFF}$ is asserted, the cycle is restarted. $\overline{BOFF}$ is active Low and must meet setup and hold times t_{18} and t_{19} for proper operation.

BRDY
Burst Ready Input (Active Low; Input)

This input pin performs the same cycle during a burst cycle that RDY performs during a non-burst cycle. BRDY indicates that the external system has presented valid data in response to a read or that the external system has accepted data in response to write. BRDY is ignored when the bus is idle and at the end of the first clock in a bus cycle. BRDY is sampled in the second and subsequent clocks of a burst cycle. The data presented on the data bus is strobed into the microprocessor when BRDY is sampled active. If RDY is returned simultaneously with BRDY, BRDY is ignored and the burst cycle is prematurely aborted. BRDY is active Low and is provided with a small pull-up resistor. BRDY must satisfy the setup and hold times t_{16} and t_{17}.

BREQ
Internal Cycle Pending (Active High; Output)

BREQ indicates that the Am486DX2 microprocessor has internally generated a bus request. BREQ is generated whether or not the Am486DX2 microprocessor is driving the bus. BREQ is active High and is never floated, except for three-state test mode (see FLUSH).

CLK
Clock (Input)

CLK is a 1x clock providing the fundamental timing for the bus interface unit and is multiplied in accordance with the CLKMUL pin to provide the internal frequency for the Am486DX2 microprocessor. All external timing parameters are specified with respect to the rising edge of CLK.

CLKMUL
Clock Multiplier (Input)

This pin must be connected to V_{SS} for proper operation.

D31–D0
Data Lines (Inputs/Outputs)

Lines D7–D0 define the least significant data byte and lines D31–D24 define the most significant byte. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. The pins are driven during the second and subsequent write cycle clocks.

D/C, M/IO, W/R
Data/Control, Memory/Input/Output, Write/Read (Active High/Active Low; Output)

These are the primary bus definition signals. These signal are driven valid as the ADS signal is asserted. The bus definition signals are not driven during bus hold and follow the timing of the address bus (see Table 2).

The D/C bus cycle definition pin distinguishes memory and I/O data cycles (D) from the control cycles (C): interrupt acknowledge, halt, and instruction fetching.

The M/IO bus cycle definition pin distinguishes memory cycles (M) from input/output cycles (IO).

The W/R bus definition pin distinguishes write cycles from read cycles.

Table 2. Bus Cycle Definition

M/IO	D/C	W/R	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Halt/Special Cycle
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Code Read
1	0	1	Reserved
1	1	0	Memory Read
1	1	1	Memory Write

DP3–DP0
Data Parity (Active High; Inputs/Outputs)

Data parity is generated on all write data cycles using the same timing as the data lines. Even parity information must be driven back into the microprocessor on the data parity pins with the same timing as read information. This process ensures that the correct parity check status is indicated. The signals read on these pins do not affect program execution. Input signals must meet setup and hold times t_{22} and t_{23}. DP3–DP0 should be connected to V_{CC} through a pull-up resistor in systems not using parity. DP3–DP0 are active High and are driven during the second and subsequent clocks of write cycles.

EADS
Valid External Address (Active Low; Input)

This pin indicates a valid external address has been driven onto the Am486DX2 microprocessor address pins. This address is used to perform an internal cache invalidation cycle. EADS is active Low and is provided with an internal pull-up resistor. EADS must satisfy setup and hold times t_{12} and t_{13}, for proper operation.

FERR
Floating-Point Error (Active Low; Output)

Driven active when a floating-point error occurs. FERR is similar to the ERROR pin on a 387 math coprocessor. FERR is included for compatibility with systems using DOS-type floating-point error reporting. FERR is active Low, and is not floated during bus hold, except during three-state test mode (see FLUSH).

FLUSH
Cache Flush (Active Low; Input)

FLUSH forces the Am486DX2 microprocessor to flush its entire internal cache. FLUSH is active Low and need only be asserted for one clock. FLUSH is asynchronous but setup and hold times t_{20} and t_{21} must be met for

recognition in any specific clock. $\overline{\text{FLUSH}}$ being sampled Low in the clock before the falling edge of RESET causes the Am486DX2 microprocessor to enter the three-state test mode.

HLDA
Hold Acknowledge (Active High; Output)

HLDA goes active in response to a hold request presented on the HOLD pin. HLDA indicates that the Am486DX2 microprocessor has given the bus to another local bus master. HLDA is driven active in the same clock that the Am486DX2 microprocessor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active High and remains driven during bus hold. HLDA is never floated except during three-state test mode (see $\overline{\text{FLUSH}}$).

HOLD
Bus Hold Request (Active High; Input)

This input pin allows another bus master complete control of the Am486DX2 microprocessor bus. In response to HOLD going active, the Am486DX2 microprocessor floats most of its output and input/output pins. HLDA is asserted after completing the current bus cycle, burst cycle, or sequence of locked cycles. The Am486DX2 microprocessor remains in this state until HOLD is deasserted. HOLD is active High and is not provided with an internal pull-down resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper operation.

$\overline{\text{IGNNE}}$
Ignore Numeric Error (Active Low; Input)

When this pin is asserted, the Am486DX2 microprocessor will ignore a numeric error and continue executing non-control floating-point instructions. When $\overline{\text{IGNNE}}$ is deasserted, the Am486DX2 microprocessor will freeze on a non-control floating-point instruction if a previous floating-point instruction caused an error. $\overline{\text{IGNNE}}$ has no effect when the NE bit in Control Register 0 is set. $\overline{\text{IGNNE}}$ is active Low and is provided with a small internal pull-up resistor. $\overline{\text{IGNNE}}$ is asynchronous but must meet setup and hold times t_{20} and t_{21} to ensure recognition in any specific clock.

INTR
Maskable Interrupt (Active High; Input)

INTR indicates an external interrupt has been generated. If the internal interrupt flag is set in EFLAGS, active interrupt processing is initiated. The Am486DX2 microprocessor generates two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed. This ensures that the interrupt is recognized. INTR is active High and is not provided with an internal pull-down resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

$\overline{\text{KEN}}$
Cache Enable (Active Low; Input)

$\overline{\text{KEN}}$ is used to determine whether the current cycle is cacheable. When the Am486DX2 microprocessor generates a cacheable cycle and $\overline{\text{KEN}}$ is active, the cycle becomes a cache line fill cycle. Returning $\overline{\text{KEN}}$ active one clock before $\overline{\text{RDY}}$ during the last read in the cache line fill causes the line to be placed in the on-chip cache. $\overline{\text{KEN}}$ is active Low and is provided with a small internal pull-up resistor. $\overline{\text{KEN}}$ must satisfy setup and hold times t_{14} and t_{15} for proper operation.

$\overline{\text{LOCK}}$
Bus Lock (Active Low; Output)

$\overline{\text{LOCK}}$ indicates the current bus cycle is locked. The Am486DX2 microprocessor does not allow a bus hold when $\overline{\text{LOCK}}$ is asserted (but address holds are allowed). $\overline{\text{LOCK}}$ goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when $\overline{\text{RDY}}$ is returned. $\overline{\text{LOCK}}$ is active Low and is not driven during bus hold. Locked read cycles are not transformed into cache fill cycles if $\overline{\text{KEN}}$ is active.

NMI
Non-Maskable Interrupt (Active High; Input)

A high NMI signal indicates that external non-maskable interrupt occurred. NMI is rising edge sensitive, but must be held Low for at least four-CLK periods before the rising edge. NMI does not have an internal pull-down resistor. NMI is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

PCD/PWT
Page Cache Disable/Page Write-Through (Active High; Outputs)

The outputs reflect the state of the page attribute bits PWT and PCD in the page table or page directory entry. If paging is disabled or unpaged cycles occur, PWT and PCD reflect the state of the PWT and PCD bits in Control Register 3. PWT and PCD have the same timing as the cycle definition pins (M/$\overline{\text{IO}}$, D/$\overline{\text{C}}$, and W/$\overline{\text{R}}$). PWT and PCD are active High and are not driven during bus hold. PCD is masked by the Cache Disable Bit (CD) in Control Register 0.

$\overline{\text{PCHK}}$
Parity Status (Active Low; Output)

For read operations, the parity status is driven on the $\overline{\text{PCHK}}$ pin one clock after $\overline{\text{RDY}}$ for data sampled at the end of the previous clock. A parity error is indicated by $\overline{\text{PCHK}}$ being Low. Parity status is only checked for enabled bytes as indicated by the byte enable and bus size signals. $\overline{\text{PCHK}}$ is valid only in the clock immediately after read data is returned to the microprocessor. At all other times, $\overline{\text{PCHK}}$ is inactive High. $\overline{\text{PCHK}}$ is never floated except during three-state test mode (see $\overline{\text{FLUSH}}$).

PLOCK
Pseudo-Lock (Active Low; Output)

PLOCK indicates that the current bus transaction requires more than one bus cycle to complete. Examples of such operations are floating-point long reads and writes (64 bits), segment table descriptor reads (64 bits), and cache line fills (128 bits). The Am486DX2 microprocessor drives PLOCK active until the addresses for the last bus cycle of the transaction have been driven, regardless of whether RDY or BRDY has been returned. Normally, PLOCK and BLAST are inverse of each other. However, during the first bus cycle of a 64-bit floating-point write, both PLOCK and BLAST will be asserted. PLOCK is a function of the BS8, BS16, and KEN inputs. PLOCK should be sampled only if the clock RDY is returned. PLOCK is active Low and is not driven during bus hold.

RESET
Reset (Active High; Input)

This pin forces the Am486DX2 microprocessor to begin execution at a known state. The microprocessor cannot begin execution of instructions until at least 1 ms after V_{CC} and CLK have reached proper DC and AC specifications. The RESET pin should remain active during this time to ensure proper microprocessor operation. RESET is active High. RESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

RDY
Non-Burst Ready (Active Low; Input)

This input pin indicates that the current bus cycle is complete. RDY indicates that the external system has presented valid data on the data pins in response to a read, or that the external system has accepted data from the Am486DX2 microprocessor in response to a write. RDY is ignored when the bus is idle and at the end of the bus cycle's first clock.

RDY is active during address hold. Data can be returned to the processor while AHOLD is active.

RDY is active Low and is not provided with an internal pull-up resistor. RDY must satisfy setup and hold times t_{16} and t_{17} for proper chip operation.

TCK
Test Clock (Input)

Test Clock is an input to the Am486DX2 CPU and provides the clocking function required by the JTAG boundary scan feature. TCK is used to clock state information and data into and out of the component. State select information and data are clocked into the component on the rising edge of TCK on TMS and TDI, respectively. Data is clocked out of the component on the falling edge of TCK on TDO.

TDI
Test Data Input (Input)

TDI is the serial input used to shift JTAG instructions and data into the component. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and the SHIFT-DR TAP controller states. During all other tap controller states, TDI is a "don't care."

TDO
Test Data Output (Output)

TDO is the serial output used to shift JTAG instructions and data out of the component. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. At all other times, TDO is driven to the high impedance state.

TMS
Test Mode Select (Input)

TMS is decoded by the JTAG TAP (Test Access Port) to select the operation of the test logic. TMS is sampled on the rising edge of TCK. To guarantee deterministic behavior of the TAP controller, TMS is provided with an internal pull-up resistor.

UP
Upgrade Present (Active Low; Input)

The Upgrade Present pin forces the Am486DX2 CPU to three-state all its outputs and enter the power-down mode. When the Upgrade Present pin is sampled asserted by the CPU in the clock before the falling edge of RESET, the power-down mode is enabled. UP has no effect on the power-down status expect during this edge. The CPU is also forced to three-state all of its outputs immediately in response to this signal. The UP signal must remain asserted in order to keep the pins three-state. UP is active Low and is provided with an internal pull-up resistor.

VOLDET
Voltage Detect (Output)

The voltage detect signal allows external system logic to distinguish between a 5-V Am486 processor and the 3.3-V Am486DX2 processor. The signal is active Low for a 3.3-V Am486DX2 processor.

Table 3. Output Pins

Name	Active Level	Floated At
BREQ	High	Three-State Test Mode
HLDA	High	Three-State Test Mode
BE3–BE0	Low	Bus Hold
PCD/PWT	High	Bus Hold
W/R, D/C, M/IO	High	Bus Hold
LOCK	Low	Bus Hold
PLOCK	Low	Bus Hold
ADS	Low	Bus Hold
BLAST	Low	Bus Hold
PCHK	Low	Three-State Test Mode
A3–A2	High	Bus, Address Hold
FERR	Low	Three-State Test Mode
VOLDET	–	-

Table 4. Input Pins

Name	Active Level	Synchronous/ Asynchronous
CLK	–	–
RESET	High	Asynchronous
HOLD	High	Synchronous
AHOLD	High	Synchronous
EADS	Low	Synchronous
BOFF	Low	Synchronous
FLUSH	Low	Asynchronous
A20M	Low	Asynchronous
BS16, BS8	Low	Synchronous
KEN	Low	Synchronous
RDY	Low	Synchronous
BRDY	Low	Synchronous
INTR	High	Asynchronous
NMI	High	Asynchronous
UP	Low	Asynchronous
IGNNE	Low	Asynchronous
CLKMUL	–	–

Table 5. Input/Output Pins

Name	Active Level	Floated At
D31—D0	High	Bus Hold
DP3–DP0	High	Bus Hold
A31–A4	High	Bus, Address Hold

Table 6. Test Pins

Name	Input or Output	Sampled/Driven On
TCK	Input	N/A
TDI	Input	Rising Edge of TCK
TDO	Output	Falling Edge of TCK
TMS	Input	Rising Edge of TCK

CPU IDENTIFICATION CODES

The DX register always contains a component identification at the conclusion of RESET. The upper byte of DX (DH) will contain 04 and the lower byte of DX (DL) will contain a CPU type/stepping identifier.

Table 7. CPU ID

Component ID (DH)	Component ID (DL)
04	32

Table 8. JTAG ID Code

Version Code	Part Number Code	Manufacturer Identity
00h	0432	01

ARCHITECTURAL OVERVIEW

The Am486DX2 processor is a 32-bit architecture with on-chip memory management and cache memory units. It is a fully compatible member of the Am486 microprocessor family.

On-chip cache memory allows frequently used data and code to be stored on-chip, thereby reducing accesses to the external bus. RISC design techniques are used to reduce instruction cycle times. A burst bus feature enables fast cache fills.

The Am486 CPU Memory Management Unit (MMU) consists of a segmentation unit and a paging unit. Segmentation allows management of the logical address space by providing easy data and code relocatibility and efficient sharing of global resources. The paging mechanism operates beneath segmentation and is transparent to the segmentation process. Paging is optional and can be disabled by system software. Each segment can be divided into one or more 4-Kbyte segments. To implement a virtual memory system, the Am486DX2 microprocessor supports full restartability for all page and segment faults.

Memory is organized into one or more variable length segments, each up to 4 Gbytes (2^{32} bytes) in size. A segment can have attributes associated with it. These attributes include its location, size, type (i.e., stack, code, or data), and protection characteristics. Each task on an Am486DX2 microprocessor can have a maximum of 16,381 segments, each up to 4 Gbytes in size. Thus, each task has a maximum of 64 Tbytes (terabytes) of virtual memory.

The segmentation unit provides four levels of protection for isolating and protecting applications and the operating system from each other. The hardware enforced protection allows high integrity system designs.

The Am486DX2 microprocessor has three modes of operation: Real Address mode (Real mode), Virtual Address mode (Protected mode), and within Protected mode, tasks may be performed in Virtual 8086 mode. In Real mode, the Am486DX2 microprocessor operates as a very fast 8086. Real mode is required primarily to set up the processor for Protected mode operation. Protected mode provides access to the sophisticated memory management paging and privilege capabilities of the processor.

Within Protected mode, software can perform a task switch to enter into tasks designated as Virtual 8086 mode tasks. Each Virtual 8086 task behaves with 8086 semantics, allowing 8086 software (an application program or an entire operating system) to execute.

The on-chip cache is 8 Kbytes. It is four-way set associative and follows a write-through policy. The on-chip cache includes features that provide flexibility in external memory system design. Individual pages can be designated as cacheable or non-cacheable by software or hardware. The cache can also be enabled and disabled by software or hardware.

Finally, the Am486DX2 microprocessor has features that facilitate high-performance hardware designs. The 2x clock multiplier improves execution performance without increasing the board design complexity. This 2x clock multiplier enhances all operations operating out of the cache and/or not blocked by external bus assesses. The burst bus feature enables fast cache fills.

ELECTRICAL DATA

The following sections describe recommended electrical connections for the Am486DX2 microprocessor and its electrical specifications.

Power and Grounding

Power Connections

The Am486DX2 microprocessor is implemented in advanced submicron CMOS-process technology and has modest power requirements. However, its high clock frequency output buffers can cause power surges as multiple output buffers drive new signal levels simultaneously. For clean, on-chip power distribution at high frequency, 23 V_{CC} and 28 V_{SS} pins feed the Am486DX2 microprocessor.

Power and ground connections must be made to all external V_{CC} and GND pins of the Am486DX2 microprocessor. On the circuit board, all V_{CC} pins must be connected on a V_{CC} plane. All V_{SS} pins must likewise be connected on a GND plane.

Power Decoupling Recommendations

Liberal decoupling capacitance should be placed near the Am486DX2 CPU. The Am486DX2 microprocessor, driving its 32-bit parallel address and data buses at high frequencies, can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high-frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the Am486DX2 microprocessor, and using decoupling capacitors as much as possible. Capacitors specifically for PGA packages are also commercially available.

System Clock Recommendations

The CLK input to the Am486DX2 processor should not be driven until V_{CC} has reached its normal operating level (3.3 V). Once V_{CC} has reached its normal operating level, the Am486DX2 CPU can handle the clock frequency for which it is specified and the oscillator/clock driver should have locked onto its desired frequency.

Other Connection Recommendations

NC pins should always remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Active Low inputs should be connected to V_{CC} through a pull-up resistor. Pull-ups in the range of 20 KΩ are recommended. Active High inputs should be connected to GND.

Any pin designated as INC is electrically isolated and has no special requirements.

ABSOLUTE MAXIMUM RATINGS

Case Temperature under Bias ..... –65°C to +110°C

Storage Temperature ..... –65°C to +150°C

Voltage on any pin
with respect to ground ..... –0.5 V to V_{CC} +2.6 V

Supply voltage with
respect to V_{SS} ..... –0.5 V to +4.6 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

T_{CASE} ..... 0°C to +85°C

V_{CC} ..... 3.3 V ± 0.3 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

Functional Operating Range: V_{CC} = 3.3 V ± 0.3 V. T_{CASE}=0°C to +85°C.

			Preliminary		
Symbol	**Parameter Description**	**Notes**	**Min**	**Max**	**Unit**
V_{IL}	Input Low Voltage		–0.3	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+2.4	V
V_{OL}	Output Low Voltage	I_{OL}=(Note 1)		0.45	V
V_{OH}	Output High Voltage	I_{OH}=(Note 2)	2.4		V
I_{CC}	Power Supply Current	(Note 3) 66 MHz (Note 3) 80 MHz		660 800	mA
I_{LI}	Input Leakage Current	(Note 4) (Note 8)		±15 ± 50	µA µA
I_{IH}	Input Leakage Current	(Note 5)		200	µA
I_{IL}	Input Leakage Current	(Note 6)		–400	µA
I_{LO}	Output Leakage Current	(Note 9) (Note 10)		±15 ± 50	µA µA
C_{IN}	Input Capacitance	F_C=1 MHz (Note 7)		10	pF
C_O	I/O or Output Capacitance	F_C=1 MHz (Note 7)		14	pF
C_{CLK}	CLK Capacitance	F_C=1 MHz (Note 7)		12	pF

Notes:

1. This parameter is measured at: *Address, Data, $\overline{BE3}$–$\overline{BE0}$* *4.0 mA*
Definition, Control *5.0 mA*

2. This parameter is measured at: *Address, Data, $\overline{BE3}$–$\overline{BE0}$* *–1.0 mA*
Definition, Control *–0.9 mA*

3. Typical supply current: 530 mA @ 66 MHz and 640 mA @ 80 MHz.

4. This parameter is for inputs without pull-ups or pull-downs and $0 \le V_{IN} \le V_{CC}$.

5. This parameter is for inputs with pull-downs and V_{IH}=2.4 V.

6. This parameter is for inputs with pull-ups and V_{IL}=0.45 V.

7. Not 100% tested.

8. This parameter is for inputs without pull-ups or pull-downs and $V_{CC} \le V_{IN} \le 5$ V.

9. This parameter is for three-state outputs where V_{EXT} is driven on the three-state output and $0 \le V_{EXT} \le V_{CC}$.

10. This parameter is for three-state outputs where V_{EXT} is driven on the three-state output and $V_{CC} \le V_{EXT} \le 5$ V.

SWITCHING CHARACTERISTICS

The switching characteristics consist of output delays, input setup requirements, and input hold requirements. All switching characteristics are relative to the rising edge of the CLK signal.

Switching characteristics measurement is defined by Figures 2–9. Inputs must be driven to the voltage levels indicated by Figure 2 when switching characteristics are measured.

Am486DX2 microprocessor delays are specified with minimum and maximum limits. The minimum Am486DX2 processor delay times are hold times provided to external circuitry. Am486DX2 CPU input setup and hold times are specified as minimums, defining the smallest acceptable sampling windows. Within the sampling windows, a synchronous input signal must be stable for correct Am486DX2 microprocessor operation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Switching Characteristics at 66 MHz; T_{CASE}=0°C to +85°C; C_L=50 pF unless otherwise specified.

Symbol	Parameter Description	Notes	Figure	Preliminary		Unit
				Min	Max	
	Operating Frequency			8	33	MHz
t_1	CLK Period		2	30	125	ns
t_{1a}	CLK Period Stability	Adjacent Clocks			0.1%	Δ
t_2	CLK High Time	@ 2.0 V	2	11		ns
t_3	CLK Low Time	@ 0.8 V	2	11		ns
t_4	CLK Fall Time		2		3	ns
t_5	CLK Rise Time		2		3	ns
t_6	A31–A2, PWT, PCD, M/$\overline{IO}$, $\overline{BE3}$–$\overline{BE0}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$, $\overline{FERR}$, BREQ, HLDA Valid Delay		7	3	14	ns
t_7	A31–A2, PWT, PCD, M/$\overline{IO}$, $\overline{BE3}$–$\overline{BE0}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$, $\overline{FERR}$, BREQ, HLDA Float Delay	(Note 1)	8		20	ns
t_8	$\overline{PCHK}$ Valid Delay		6	3	14	ns
t_{8a}	$\overline{BLAST}$, $\overline{PLOCK}$ Valid Delay		7	3	14	ns
t_9	$\overline{BLAST}$, $\overline{PLOCK}$ Float Delay	(Note 1)	8		20	ns
t_{10}	D31–D0, DP3–DP0 Write Data Valid Delay		7	3	14	ns
t_{11}	D31–D0, DP3–DP0 Write Data Float Delay	(Note 1)	8		20	ns
t_{12}	$\overline{EADS}$ Setup Time		4	5		ns
t_{13}	$\overline{EADS}$ Hold Time		4	3		ns
t_{14}	$\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Setup Time		4	5		ns
t_{15}	$\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Hold Time		4	3		ns
t_{16}	$\overline{RDY}$, $\overline{BRDY}$ Setup Time		5	5		ns
t_{17}	$\overline{RDY}$, $\overline{BRDY}$ Hold Time		5	3		ns
t_{18}	HOLD, AHOLD Setup Time		4	6		ns
t_{18a}	$\overline{BOFF}$ Setup Time		4	7		ns
t_{19}	HOLD, AHOLD, $\overline{BOFF}$ Hold Time		4	3		ns
t_{20}	RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR, $\overline{IGNNE}$ Setup Time		3, 4	5		ns
t_{21}	RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR, $\overline{IGNNE}$ Hold Time		3, 4	3		ns
t_{22}	D31–D0, DP3–DP0, A31–A4 Read Setup Time		4, 5	5		ns
t_{23}	D31–D0, DP3–DP0, A31–A4 Read Hold Time		4, 5	3		ns

***Note**:*

1. Not 100% tested. Guaranteed by design characterization.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

Switching Characteristics at 80 MHz; T_{CASE}=0°C to +85°C; C_L=50 pF unless otherwise specified.

Symbol	Parameter Description	Notes	Figure	Preliminary		Unit
				Min	Max	
	Operating Frequency			8	40	MHz
t_1	CLK Period		2	25	125	ns
t_{1a}	CLK Period Stability	Adjacent Clocks			0.1%	Δ
t_2	CLK High Time	@ 2.0 V	2	9		ns
t_3	CLK Low Time	@ 0.8 V	2	9		ns
t_4	CLK Fall Time		2		3	ns
t_5	CLK Rise Time		2		3	ns
t_6	A31–A2, PWT, PCD, M/$\overline{IO}$, $\overline{BE3}$–$\overline{BE0}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$, $\overline{FERR}$, BREQ, HLDA Valid Delay		7	3	14	ns
t_7	A31–A2, PWT, PCD, M/$\overline{IO}$, $\overline{BE3}$–$\overline{BE0}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$, $\overline{FERR}$, BREQ, HLDA Float Delay	(Note 1)	8	3	18	ns
t_8	$\overline{PCHK}$ Valid Delay		6	3	16	ns
t_{8a}	$\overline{BLAST}$, $\overline{PLOCK}$ Valid Delay		7	3	18	ns
t_9	$\overline{BLAST}$, $\overline{PLOCK}$ Float Delay	(Note 1)	8	3	16	ns
t_{10}	D31–D0, DP3–DP0 Write Data Valid Delay		7	3	14	ns
t_{11}	D31–D0, DP3–DP0 Write Data Float Delay	(Note 1)	8	3	18	ns
t_{12}	$\overline{EADS}$ Setup Time		4	5		ns
t_{13}	$\overline{EADS}$ Hold Time		4	3		ns
t_{14}	$\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Setup Time		4	5		ns
t_{15}	$\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Hold Time		4	3		ns
t_{16}	$\overline{RDY}$, $\overline{BRDY}$ Setup Time		5	5		ns
t_{17}	$\overline{RDY}$, $\overline{BRDY}$ Hold Time		5	3		ns
t_{18}	HOLD, AHOLD Setup Time		4	6		ns
t_{18a}	$\overline{BOFF}$ Setup Time		4	8		ns
t_{19}	HOLD, AHOLD, $\overline{BOFF}$ Hold Time		4	3		ns
t_{20}	RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR, $\overline{IGNNE}$ Setup Time		3, 4	5		ns
t_{21}	RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR, $\overline{IGNNE}$ Hold Time		3, 4	3		ns
t_{22}	D31–D0, DP3–DP0, A31–A4 Read Setup Time		4, 5	5		ns
t_{23}	D31–D0, DP3–DP0, A31–A4 Read Hold Time		4, 5	3		ns

***Note**:*

1. Not 100% tested. Guaranteed by design characterization.

Am486DX2 CPU AC Characteristics for Boundary Scan Test Signals at 25 MHz

V_{CC} = 3.3 V ± 0.3 V; T_{CASE}=0°C to +85°C; C_L = 50 pF. All inputs and outputs are TTL Level.

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{24}	TCK Frequency		25	MHz		1x Clock
t_{25}	TCK Period	40		ns		Note 2
t_{26}	TCK High Time	10		ns		at 2.0 V
t_{27}	TCK Low Time	10		ns		at 0.8 V
t_{28}	TCK Rise Time		4	ns		Note 1
t_{29}	TCK Fall Time		4	ns		Note 1
t_{30}	TDI, TMS Setup Time	8		ns	9	Note 3
t_{31}	TDI, TMS Hold Time	7		ns	9	Note 3
t_{32}	TDO Valid Delay	3	25	ns	9	Note 3
t_{33}	TDO Float Delay		36	ns	9	Note 3
t_{34}	All Outputs (Non-Test) Valid Delay	3	25	ns	9	Note 3
t_{35}	All Outputs (Non-Test) Float Delay		36	ns	9	Note 3
t_{36}	All Inputs (Non-Test) Setup Time	8		ns	9	Note 3
t_{37}	All Inputs (Non-Test) Hold Time	7		ns	9	Note 3

Notes:

1. Rise/Fall times are measured between 0.8 V and 2.0 V. Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.

2. TCK period $\geq$ CLK period.

3. Parameter measured from TCK.

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

Figure 1. Change State Diagram

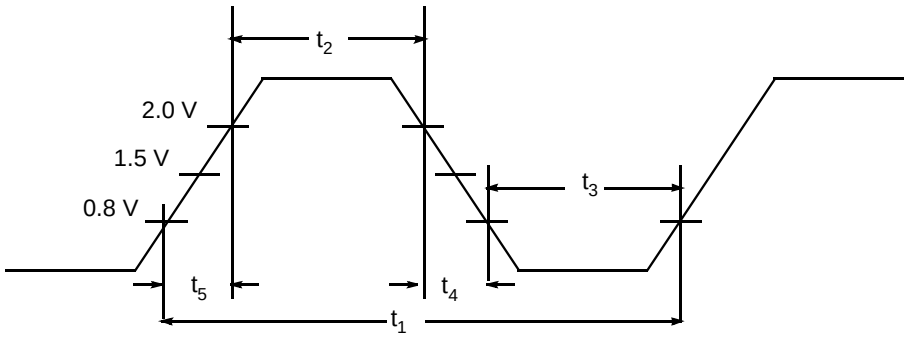


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Figure 2. CLK Waveforms

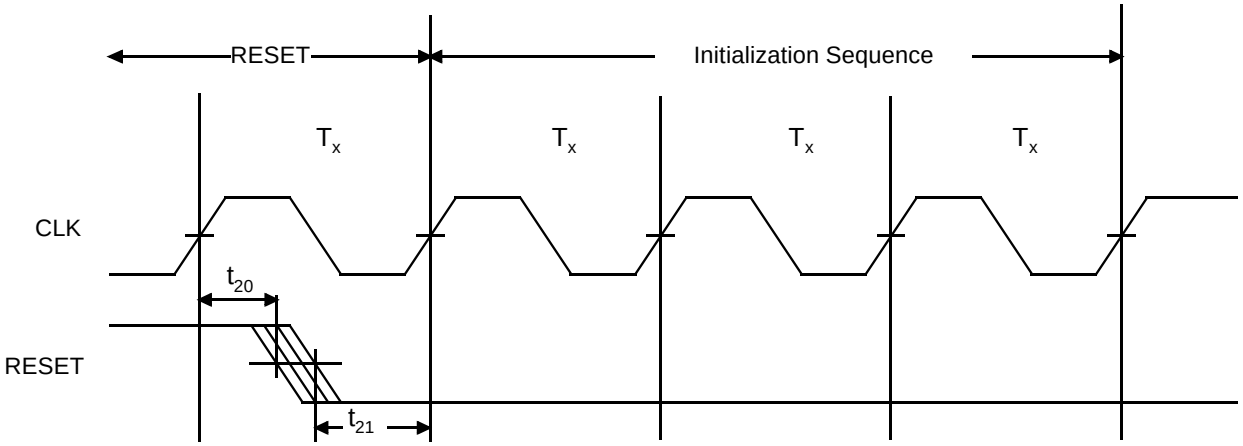

Figure 3. Reset Setup and Hold Timing

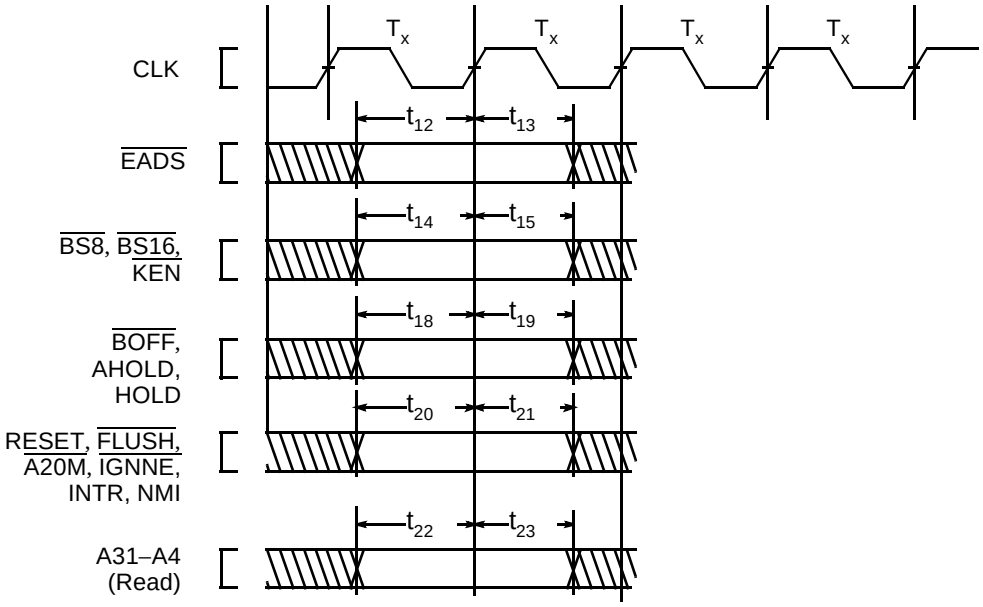

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Figure 3. Input Setup and Hold Timing

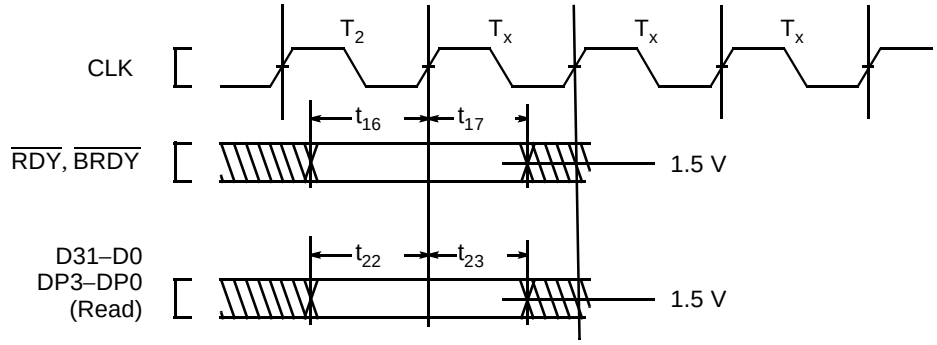

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Figure 4. $\overline{\text{RDY}}$ and $\overline{\text{BRDY}}$ Input Setup and Hold Timing

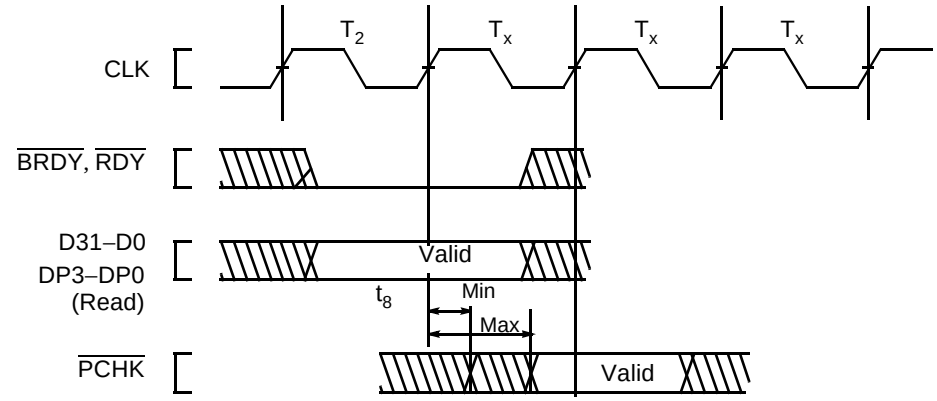

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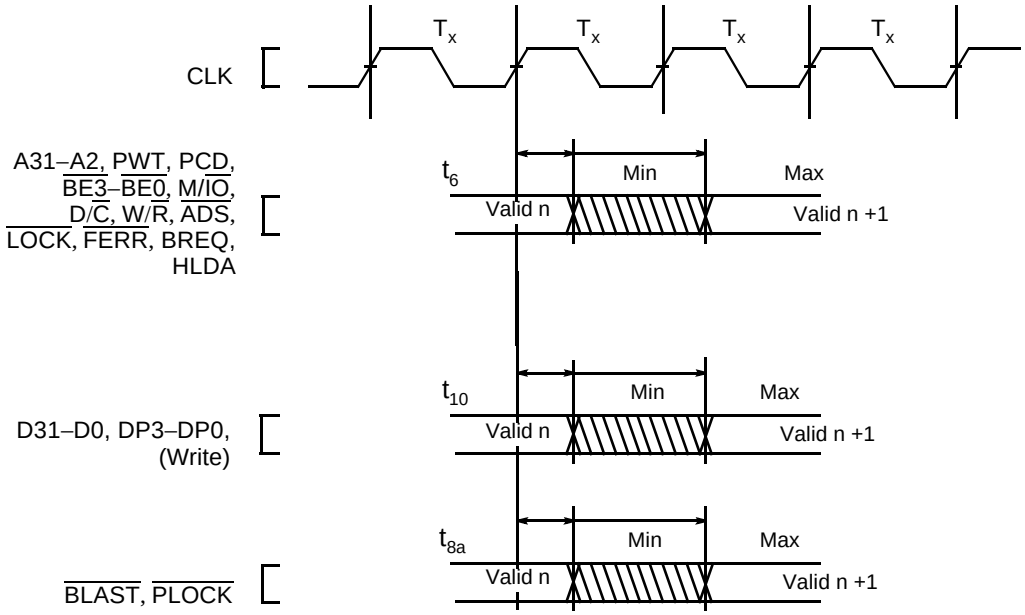
Figure 5. $\overline{\text{PCHK}}$ Valid Delay Timing



17852A-102

Figure 6. Output Valid Delay Timing

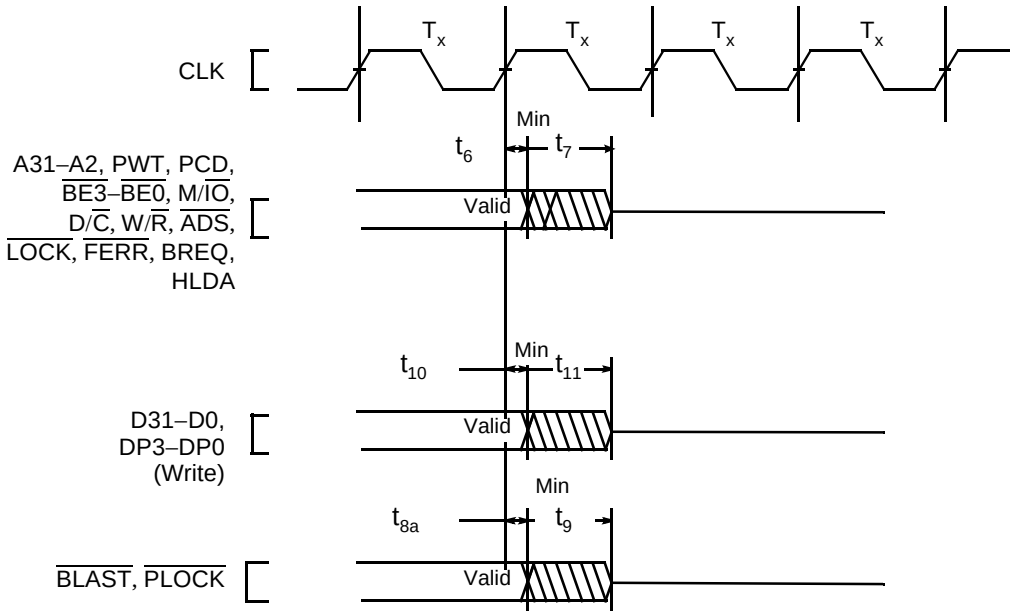


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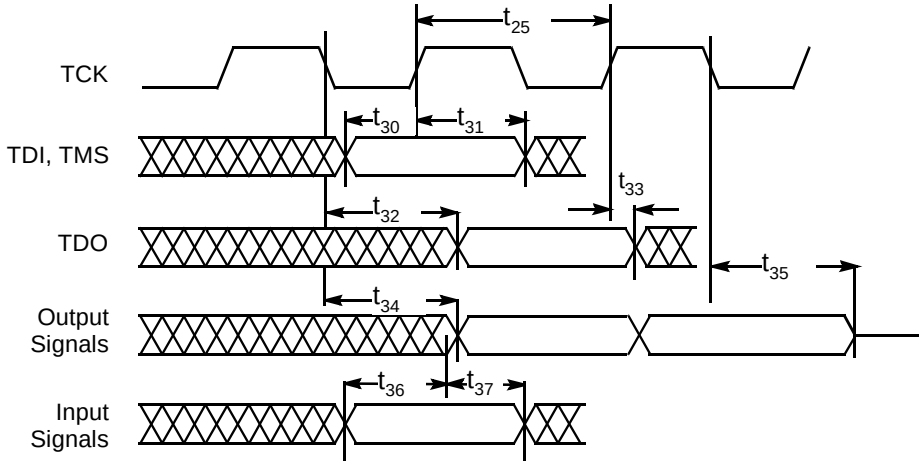
Figure 7. Maximum Float Delay Timing



17852B-104

Figure 8. Test Signal Timing Diagram

Package Thermal Specifications

The Am486DX2 microprocessor is specified for operation when T_{CASE} (the case temperature) is within the range of 0°C to +85°C. T_{CASE} can be measured in any environment to determine whether the Am486DX2 microprocessor is within specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

The ambient temperature (T_A) is guaranteed as long as T_{CASE} is not violated. The ambient temperature can be calculated from θ_{JC} and θ_{JA} and from the following equations:

$T_J = T_{CASE} + P \bullet \theta_{JC}$

$T_A = T_J - P \bullet \theta_{JA}$

$T_{CASE} = T_A + P \bullet [\theta_{JA} - \theta_{JC}]$

where:

T_J, T_A, T_{CASE}= Junction, Ambient, and Case Temperature.

θ_{JC}, θ_{JA} = Junction-to-Case and Junction-to-Ambient Thermal Resistance, respectively.

P = Maximum Power Consumption

The values for θ_{JA} and θ_{JC} are given in Table 9 for the 1.75 sq. in., 168-pin, ceramic PGA.

Table 10 shows the T_A allowable (without exceeding T_{CASE}) at various airflows and operating frequencies (Clock). Note that T_A is greatly improved by attaching fins or a heat sink to the package. Heat sink dimensions are shown in Figure 10. P (the maximum power consumption) is calculated by using the maximum I_{CC} as tabulated in the *DC Characteristics*.

Table 9. Thermal Resistance (°C/W) θ_{JC} and θ_{JA} for the 66-MHz and 80-MHz Am486DX2 CPU

		θ_{JA} vs. Airflow-ft/min. (m/sec)					
	θ_{JC}	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
No Heat Sink	1.5	16.5	14.0	12.0	10.5	9.5	9.0
Heat Sink*	2.0	12.0	7.0	5.0	4.0	3.5	3.25
Heat Sink* and fan	2.0	5.0	4.6	4.2	3.8	3.5	3.25

**0.350″ high unidirectional heat sink (Al alloy 6063-T5, 40 mil fin width, 155 mil center-to-center fin spacing).*

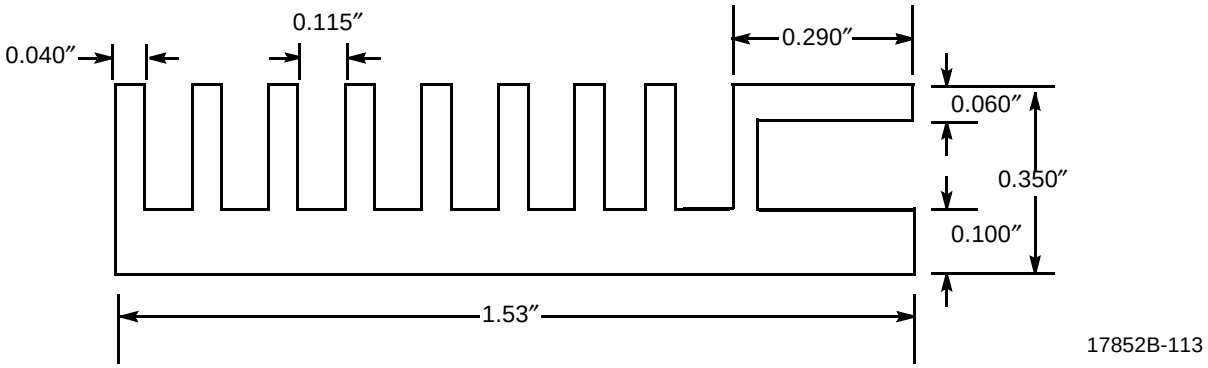


Figure 10. Heat Sink Dimensions

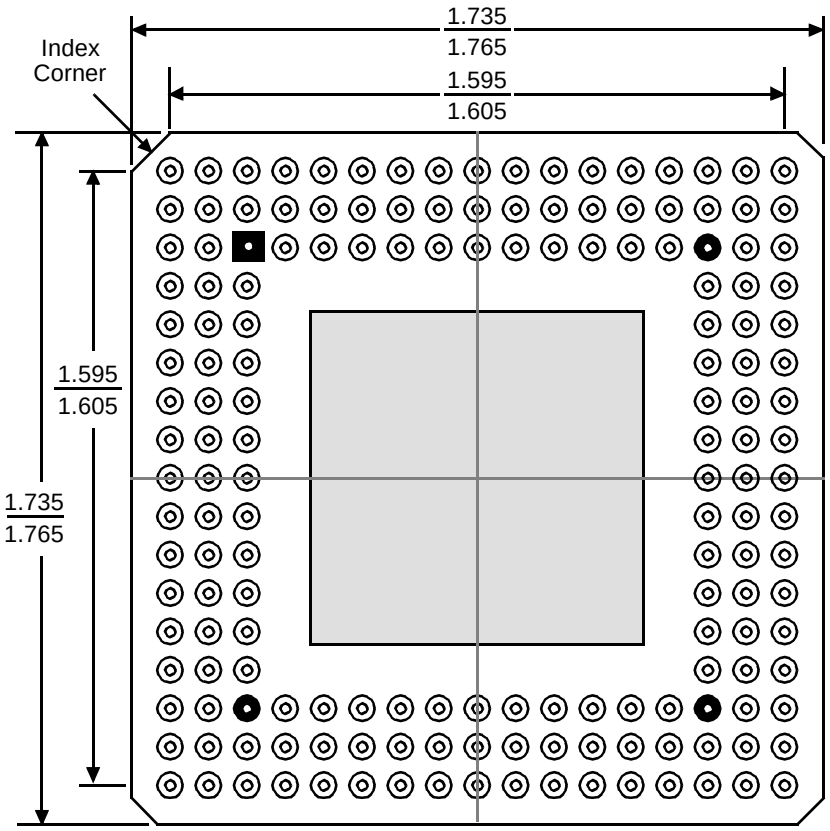
Table 10. Maximum T_A at Various Airflows in °C

		Airflow-ft/min. (m/sec)					
	Clock	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
T_A without Heat Sink*	66 MHz	49.4	55.3	60.1	63.6	66.0	67.2
T_A with Heat Sink	66 MHz	61.2	73.1	77.9	80.3	81.4	82.0
	80 MHz	56.2	70.6	76.4	79.2	80.7	81.4
T_A with Heat Sink and fan	66 MHz	77.9	78.8	79.8	80.7	81.4	82.0
	80 MHz	76.4	77.5	78.7	79.8	80.7	81.4

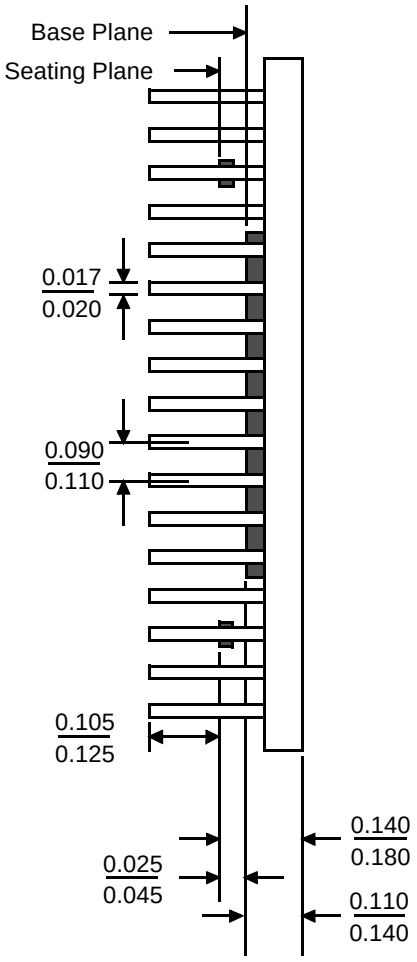
PHYSICAL DIMENSIONS

For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Space Centering.

CGM 168



Bottom View (Pins Facing Up)



Side View

16734C

5/11/93 MH