Dual N-Channel 60-V (D-S) MOSFET

Key Features:

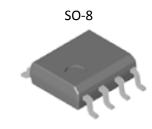
- Low r_{DS(on)} trench technology
- · Low thermal impedance
- Fast switching speed

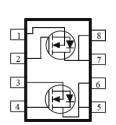
Typical Applications:

- · White LED boost converters
- Automotive Systems
- Industrial DC/DC Conversion Circuits

PRODUCT SUMMARY				
V _{DS} (V)	$r_{DS(on)}(m\Omega)$	I⊳(A)		
60	$35 @ V_{GS} = 10V$	6.4		
	45 @ V _{GS} = 4.5V	5.6		







ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}$ C UNLESS OTHERWISE NOTED)					
Parameter			Limit	Units	
Drain-Source Voltage	V_{DS}	60	V		
Gate-Source Voltage	V_{GS}	±20	V		
Continuous Drain Current ^a	T _A =25°C		6.4		
Continuous Drain Current	T _A =70°C	I _D	5	Α	
Pulsed Drain Current ^b	I _{DM}	25			
Continuous Source Current (Diode Conduction) a	I_S	3.1	Α		
Power Dissipation ^a	T _A =25°C	P _D	2.1	W	
Fower Dissipation	T _A =70°C	l 'D	1.3	V V	
Operating Junction and Storage Temperature Range			-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
Maximum Junction-to-Ambient ^a	t <= 10 sec	$R_{\theta JA}$	62.5	°C/W	
Maximum Junction-to-Ambient	Steady State	IΛθJA	110	C/VV	

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Electrical Characteristics

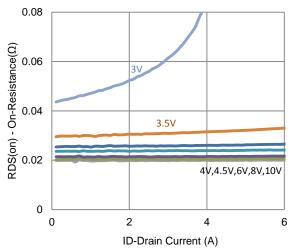
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Source Threshold Voltage	$V_{GS(th)}$ $V_{DS} = V_{GS}$, $I_D = 250 \text{ uA}$		1			V	
Gate-Body Leakage	I_{GSS} $V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$				±100	nA	
Zero Gate Voltage Drain Current	lana	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA	
Zero Gate Voltage Brain Gurrent	I _{DSS}	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			25] uA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	10			Α	
Drain-Source On-Resistance ^a	r	$V_{GS} = 10 \text{ V}, I_D = 5.4 \text{ A}$			35	mΩ	
Drain-Source On-Resistance	r _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 4.4 \text{ A}$			45	11152	
Forward Transconductance ^a	g _{fs}	$V_{DS} = 15 \text{ V}, I_{D} = 5.4 \text{ A}$		13		S	
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.6 \text{ A}, V_{GS} = 0 \text{ V}$		0.74		V	
		Dynamic ^b					
Total Gate Charge	Q_g	$V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V},$		16			
Gate-Source Charge	Q_gs	$I_{DS} = 30 \text{ V}, \text{ V}_{GS} = 4.3 \text{ V},$ $I_{D} = 5.4 \text{ A}$		3.9		nC	
Gate-Drain Charge	Q_gd	ID = 0.4 //		8.2			
Turn-On Delay Time	t _{d(on)}	$V_{DS} = 30 \text{ V}, R_1 = 5.6 \Omega,$		8			
Rise Time	t _r	$I_{DS} = 30 \text{ V}, \text{ NL} = 3.0 \Omega_{2},$ $I_{D} = 5.4 \text{ A},$		9		ne	
Turn-Off Delay Time	$t_{d(off)}$	$V_{GEN} = 10 \text{ V}, R_{GEN} = 6 \Omega$		49		ns	
Fall Time	t _f	VGEN - 10 V, NGEN 0 12		14			
Input Capacitance	C_{iss}			1460			
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		125		pF	
Reverse Transfer Capacitance	C_{rss}	1		110			

Notes

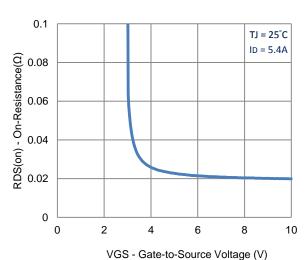
- Pulse test: PW <= 300us duty cycle <= 2%.
- Guaranteed by design, not subject to production testing. b.

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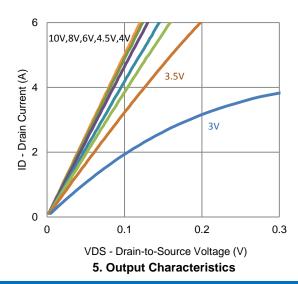
Typical Electrical Characteristics

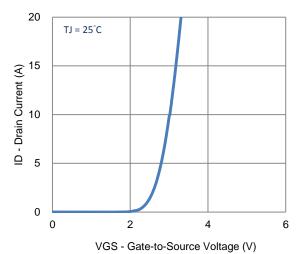


1. On-Resistance vs. Drain Current

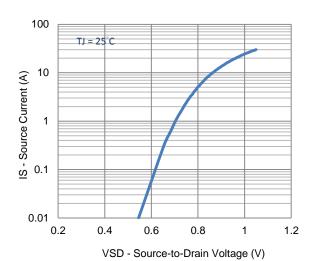


3. On-Resistance vs. Gate-to-Source Voltage

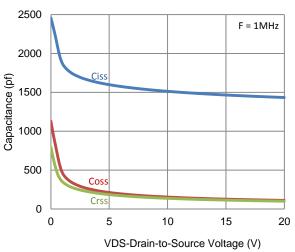




2. Transfer Characteristics

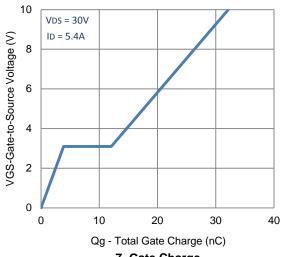


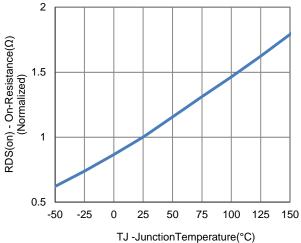
4. Drain-to-Source Forward Voltage



6. Capacitance

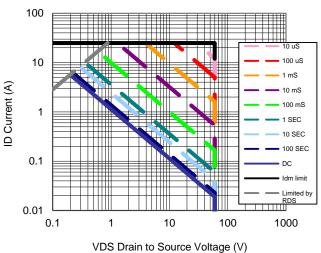
Typical Electrical Characteristics

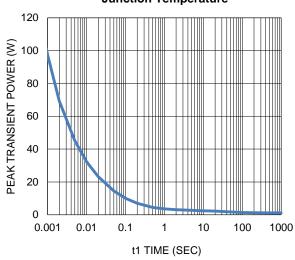




7. Gate Charge

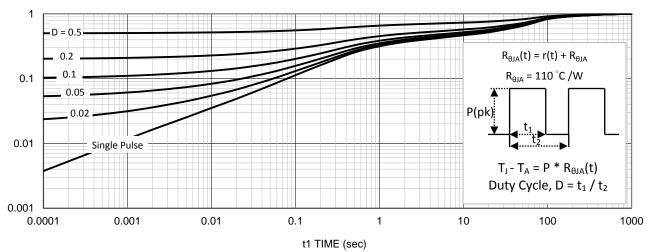
8. Normalized On-Resistance Vs
Junction Temperature





9. Safe Operating Area

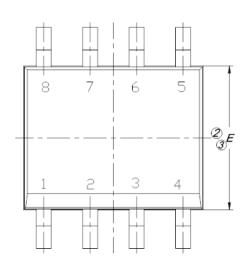
10. Single Pulse Maximum Power Dissipation

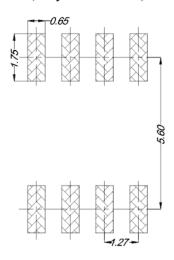


11. Normalized Thermal Transient Junction to Ambient

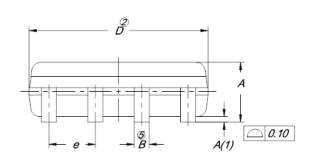
Package Information

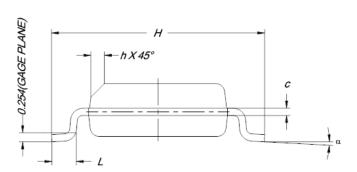
Land Pattern (Only for Reference)





5114	MILLIMETERS					
DIM.	MIN.	NOM.	MAX.			
Α	1.35	1.55	1.75			
A(1)	0.10	0.18	0.25			
В	0.38	0.45	0.51			
С	0.19	0.22	0.25			
D	4.80	4.90	5.00			
E	3.80	3.90	4.00			
е	1.27 BSC					
Н	5.80	6.00	6.20			
L	0.50	0.72	0.93			
α	0°	4°	8°			
h	0.25	0.38	0.50			





Note:

- 1. All Dimension Are In mm.
- Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- 3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
- 4. The Package Top May Be Smaller Than The Package Bottom.
- Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.