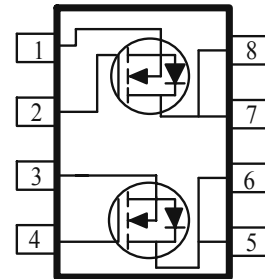
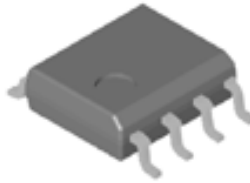


**Dual N-Channel 30-V (D-S) MOSFET**

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ m( $\Omega$ )	$I_D$ (A)
30	58 @ $V_{GS} = 4.5V$	5.0
	82 @ $V_{GS} = 2.5V$	4.2

- Low  $r_{DS(on)}$  provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	
Continuous Drain Current <sup>a</sup>	$I_D$	$T_A=25^\circ C$	5.0
		$T_A=70^\circ C$	4.1
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	$\pm 30$	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	1.7	A
Power Dissipation <sup>a</sup>	$P_D$	$T_A=25^\circ C$	2.1
		$T_A=70^\circ C$	1.3
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	$t \leq 10$ sec	62.5
		Steady State	80

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

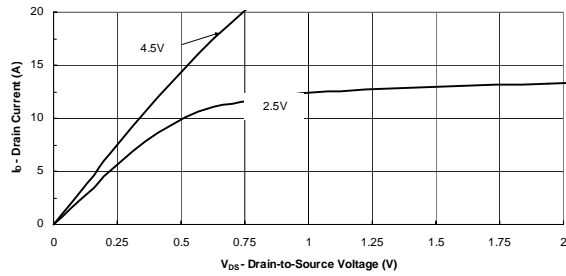
SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
<b>Static</b>						
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 uA	0.7			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	uA
		V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55°C			25	
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 4.5 V	20			A
Drain-Source On-Resistance <sup>A</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A			58	mΩ
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 4.2 A			82	
Forward Transconductance <sup>A</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 A		22		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 1.7 A, V <sub>GS</sub> = 0 V		0.7		V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A		6.3		nC
Gate-Source Charge	Q <sub>gs</sub>			0.9		
Gate-Drain Charge	Q <sub>gd</sub>			1.9		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1MHz		257		pF
Output Capacitance	C <sub>oss</sub>			62		
Reverse Transfer Capacitance	C <sub>rss</sub>			30		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 15 Ω, I <sub>D</sub> = 1 A, V <sub>GEN</sub> = 4.5 V		22		nS
Rise Time	t <sub>r</sub>			40		
Turn-Off Delay Time	t <sub>d(off)</sub>			50		
Fall-Time	t <sub>f</sub>			20		

Notes

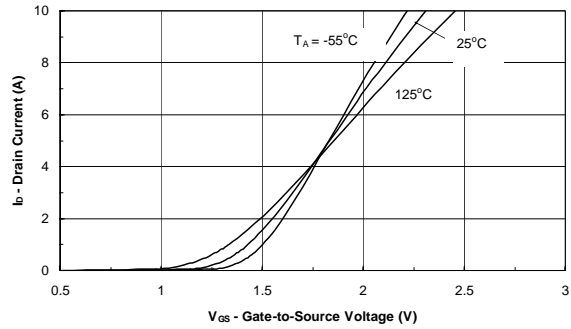
- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

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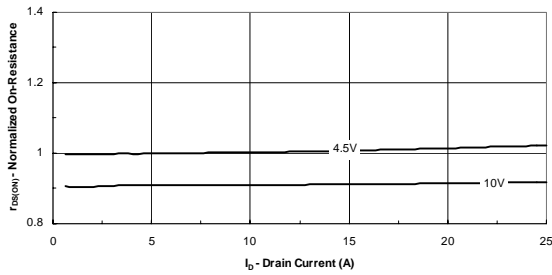
Typical Electrical Characteristics (N-Channel)



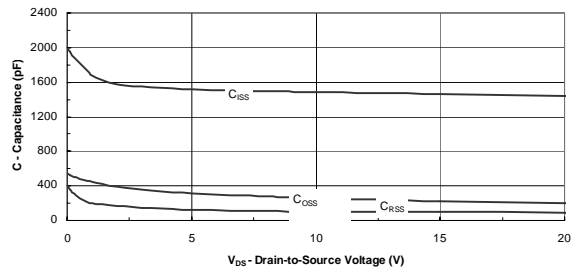
Output Characteristics



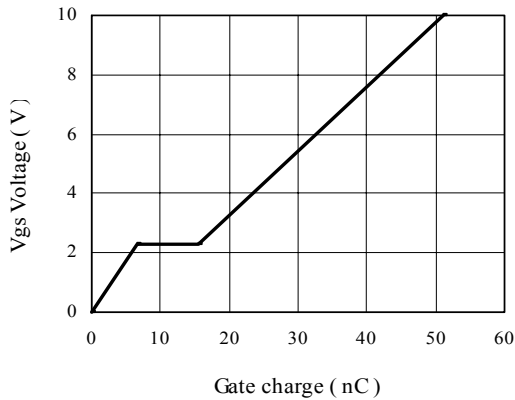
Transfer Characteristics



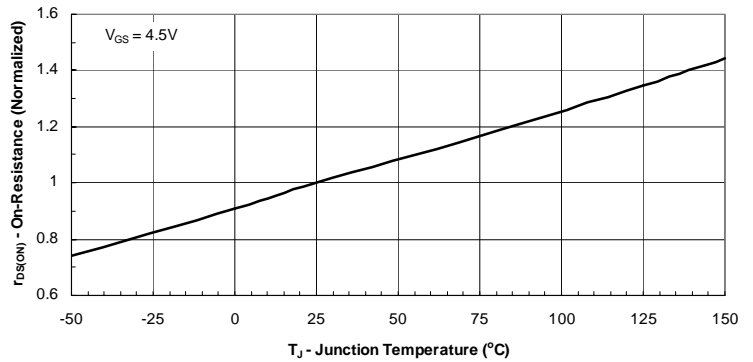
On-Resistance vs. Drain Current



Capacitance

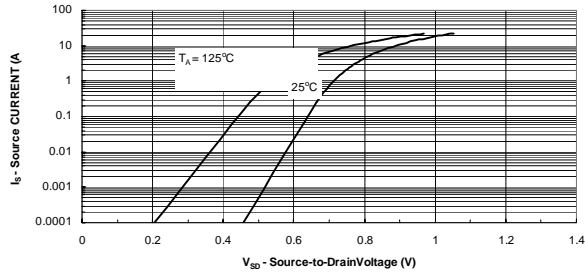


Gate Charge

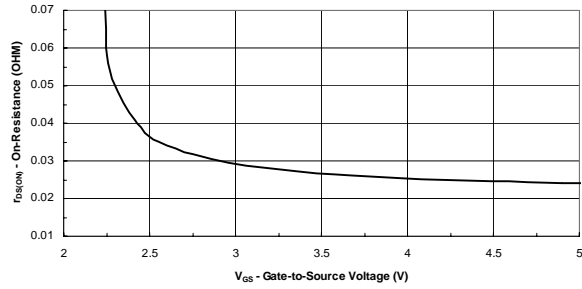


On-Resistance vs. Junction Temperature

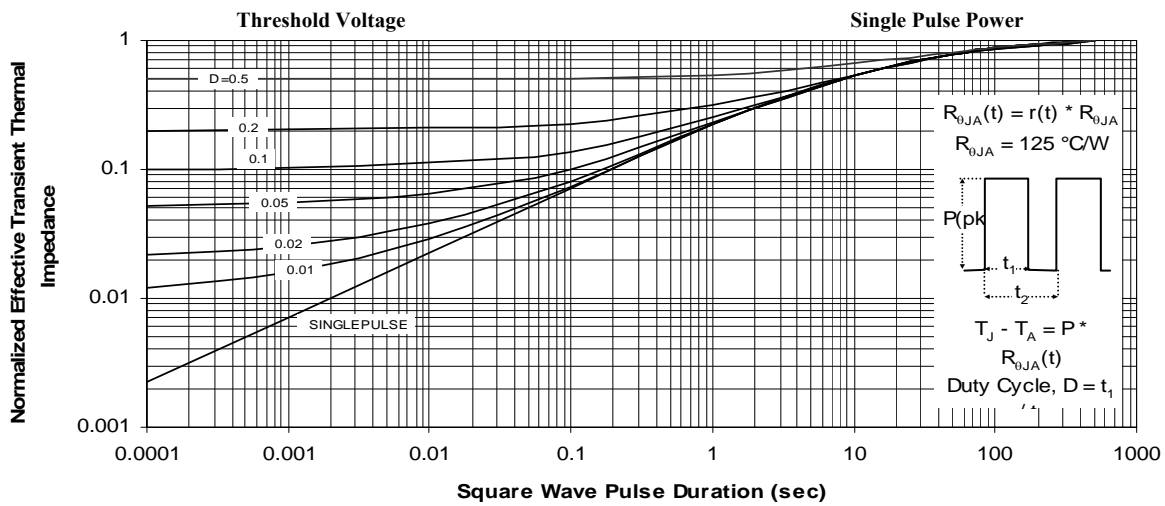
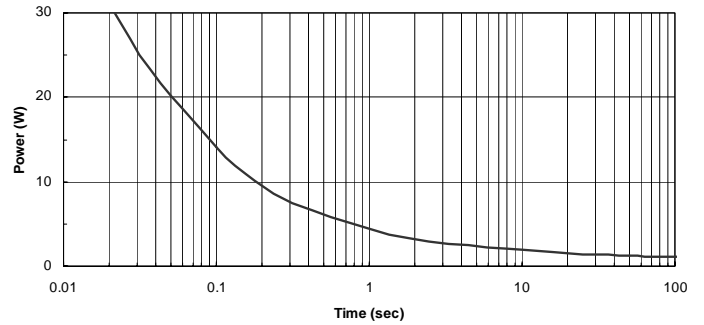
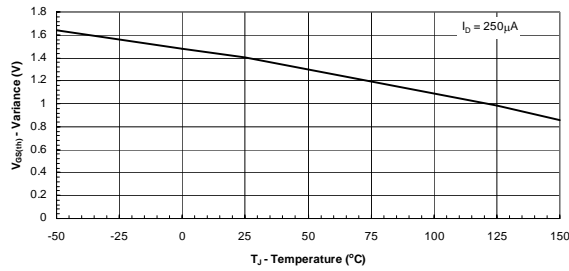
Typical Electrical Characteristics (N-Channel)



Source-Drain Diode Forward Voltage



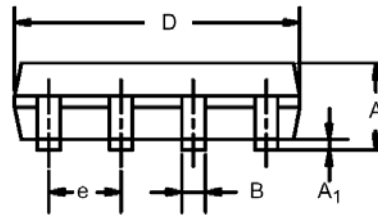
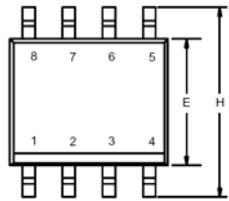
On-Resistance vs. Gate-to-Source Voltage



Normalized Thermal Transient Impedance, Junction-to-Ambient

Package Information

SO-8: 8LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°

