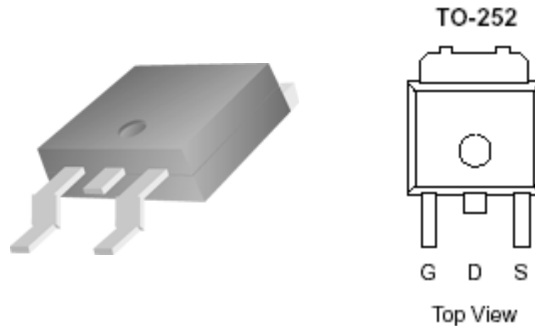


P-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature TO-252 Surface Mount Package Saves Board Space
- High power and current handling capability
- Extended VGS range (± 25) for battery pack applications



PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} m(Ω)	I _D (A)
-20	9 @ V _{GS} = -4.5V	18
	13 @ V _{GS} = -2.5V	15

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V _{DS}	-20	V
Gate-Source Voltage	V _{GS}	±12	
Continuous Drain Current ^a	T _A =25°C I _D	18	A
Pulsed Drain Current ^b	I _{DM}	±100	
Continuous Source Current (Diode Conduction) ^a	I _S	-30	A
Power Dissipation ^a	T _A =25°C P _D	70	W
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 175	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	R _{θJA}	30	°C/W
Maximum Junction-to-Case	R _{θJC}	1.8	°C/W

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

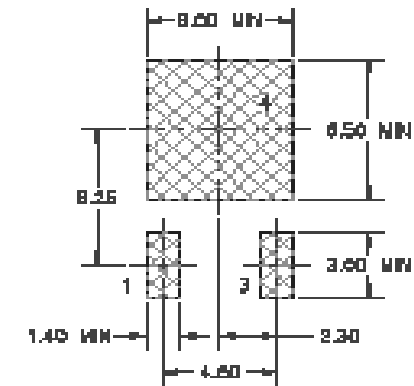
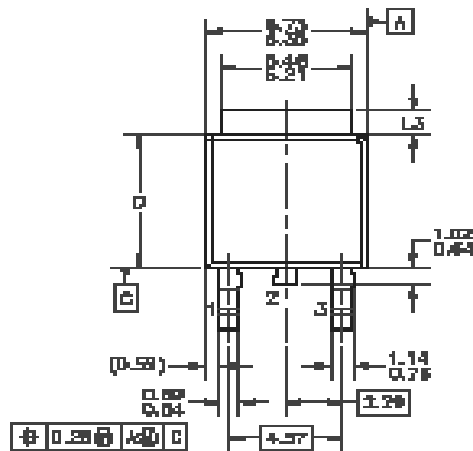
SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 uA	-0.7			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±25 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V			-1	uA
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 55°C			-5	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -4.5 V	-41			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -18 A			9	mΩ
		V _{GS} = -2.5 V, I _D = -15 A			13	
Forward Transconductance ^A	g _{fs}	V _{DS} = -15 V, I _D = -18 A		31		S
Diode Forward Voltage	V _{SD}	I _S = -41 A, V _{GS} = 0 V		-0.7		V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -18 A		66		nC
Gate-Source Charge	Q _{gs}			13.0		
Gate-Drain Charge	Q _{gd}			17		
Switching						
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 15 Ω, I _D = -41 A, V _{GEN} = -10 V, R _G = 6Ω		15		nS
Rise Time	t _r			12		
Turn-Off Delay Time	t _{d(off)}			62		
Fall-Time	t _f			46		

Notes

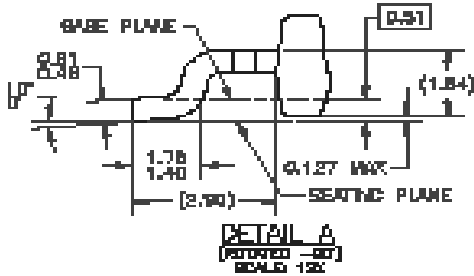
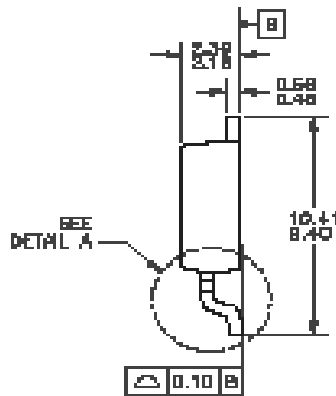
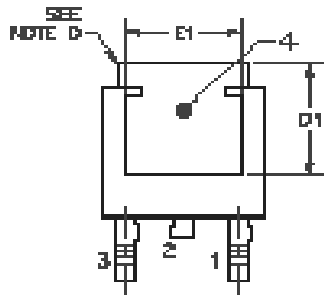
- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

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Package Information



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-262, ISSUE C, VARIATION AA, 30 DE, DATED NOV. 1999.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.004-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION A1	OPTION A2
L3	0.68-1.27	1.65-2.54
D	0.92-0.99	0.93-0.99
E1	4.92 MIN	3.81 MIN
D1	3.41 MIN	4.57 MIN