

# Am25LS192 • Am25LS193 Am54LS/74LS192 • Am54LS/74LS193

## Decimal and Hexadecimal Up/Down Counters

### DISTINCTIVE CHARACTERISTICS

- Separate up and down clocks
- Asynchronous parallel load
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower  $V_{OL}$  at  $I_{OL} = 8mA$
  - Twice the fan-out over military range
  - 440 $\mu A$  source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

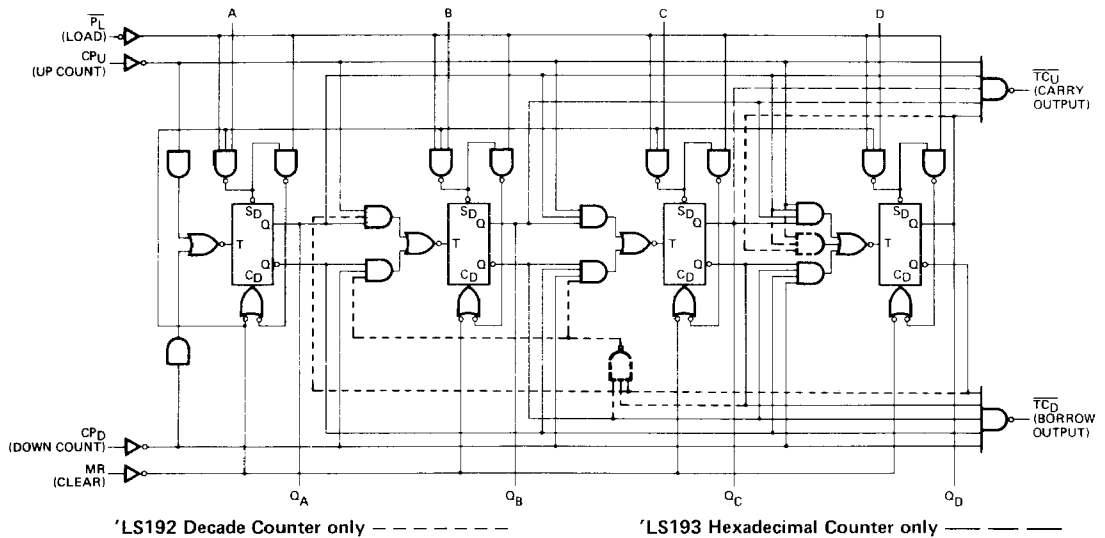
### FUNCTIONAL DESCRIPTION

The 'LS192 and 'LS193 are four-bit up/down counters using advanced Low-Power Schottky processing. The 'LS192 counts in the BCD mode and the 'LS193 counts in the binary mode. These counters have separate count-up and count-down clock inputs ( $CP_U$  and  $CP_D$ , respectively). The  $Q_i$  outputs change state synchronously on the LOW-to-HIGH transition on either the up clock input or the down clock input. Only one clock input can be LOW at a time or erroneous counting will result.

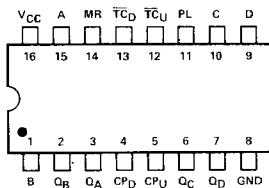
Each of the four flip-flops can be preset to a logic HIGH or a logic LOW by means of four parallel inputs (A, B, C, and D). When the parallel load input ( $\overline{PL}$ ) goes LOW, all four flip-flops set to the state of the direct inputs (A, B, C, and D) independent of the clock inputs. An active HIGH master reset ( $\overline{MR}$ ) is provided which overrides both the clock and parallel load inputs forcing all  $Q_i$  outputs LOW.

Two terminal count outputs are gated with the clock inputs to provide clock signal to other counters. The  $TC_D$  output goes LOW when the counter is in state 0000 and the count down clock goes LOW. The  $TC_U$  goes LOW when the count up goes LOW and the counter is in state 1001 ('LS192) or state 1111 ('LS193). The  $TC_U$  and  $TC_D$  outputs can drive the count up and count down clocks on the next counter in a series. The  $Q_i$  outputs of such a connection scheme are not synchronous on cascaded counters in this series.

### LOGIC DIAGRAM

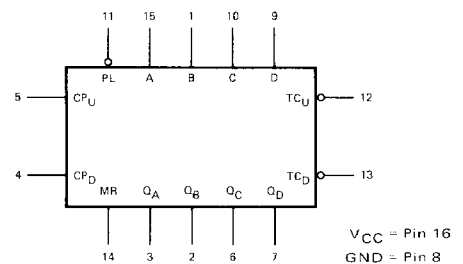


### CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL



$V_{CC} = \text{Pin } 16$   
 $GND = \text{Pin } 8$

## Am25LS192 • Am25LS193

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25LS192XC/Am25LS193XC	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = 5.0\text{V} \pm 5\%$ (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am25LS192XM/Am25LS193XM	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$	$V_{CC} = 5.0\text{V} \pm 10\%$ (MIL)	MIN. = 4.50V	MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)	Typ. (Note 2)			Units	
			Min.	Max.	Max.		
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{MIN.}, I_{OH} = -440\mu\text{A}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	MIL	2.5	3.4	Volts	
			COM'L	2.7	3.4		
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{MIN.},$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 4.0\text{mA}$		0.25	0.40	Volts
			$I_{OL} = 8.0\text{mA}$		0.35	0.45	
$V_{IH}$	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts	
$V_{IL}$	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL		0.7	Volts	
			COM'L		0.8		
$V_I$	Input Clamp Voltage	$V_{CC} = \text{MIN.}, I_{IN} = -18\text{mA}$			-1.5	Volts	
$I_{IL}$	Input LOW Current	$V_{CC} = \text{MAX.}, V_{IN} = 0.4\text{V}$			-0.4	mA	
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 2.7\text{V}$			20	$\mu\text{A}$	
$I_I$	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 7.0\text{V}$			0.1	mA	
$I_{SC}$	Output Short Circuit Current (Note 3)	$V_{CC} = \text{MAX.}$	-15		-85	mA	
$I_{CC}$	Power Supply Current	$V_{CC} = \text{MAX.}$ (Note 4)		19	34	mA	

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical characteristics for the applicable device type.  
 2. Typical limits are at  $V_{CC} = 5.0\text{V}$ ,  $25^\circ\text{C}$  ambient and maximum loading.  
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 4.  $I_{CC}$  is measured with all outputs open; clear and load inputs grounded; and all other inputs at 4.5V

## Am25LS • Am54LS/74LS

## MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	$-65^\circ\text{C to } +150^\circ\text{C}$
Temperature (Ambient) Under Bias	$-55^\circ\text{C to } +125^\circ\text{C}$
Supply Voltage to Ground Potential Continuous	$-0.5\text{V to } +7.0\text{V}$
DC Voltage Applied to Outputs for High Output State	$-0.5\text{V to } +V_{CC} \text{ max.}$
DC Input Voltage	$-0.5\text{V to } +7.0\text{V}$
DC Output Current, Into Outputs	30mA
DC Input Current	$-30\text{mA to } +5.0\text{mA}$

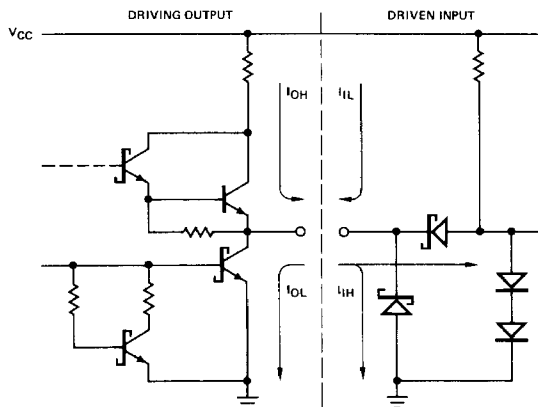
## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74LS192X/74LS193X	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = 5.0\text{V} \pm 5\% (\text{COM'L})$	MIN. = 4.75V	MAX. = 5.25V
Am54LS192X/54LS193X	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$	$V_{CC} = 5.0\text{V} \pm 10\% (\text{MIL})$	MIN. = 4.50V	MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)	Typ. (Note 2)			Units	
			Min.	Max.	Max.		
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{MIN.}, I_{OH} = -400\mu\text{A}$ $V_{IN} = V_{IH}$ or $V_{IL}$	MIL	2.5	3.4	Volts	
			COM'L	2.7	3.4		
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{MIN.},$ $V_{IN} = V_{IH}$ or $V_{IL}$	All, $I_{OL} = 4.0\text{mA}$		0.25	0.40	Volts
			74LS only, $I_{OL} = 8.0\text{mA}$		0.35	0.50	
$V_{IH}$	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts	
$V_{IL}$	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L				
$V_I$	Input Clamp Voltage	$V_{CC} = \text{MIN.}, I_{IN} = -18\text{mA}$				-1.5	Volts
$I_{IL}$	Input LOW Current	$V_{CC} = \text{MAX.}, V_{IN} = 0.4\text{V}$				-0.4	mA
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 2.7\text{V}$				20	$\mu\text{A}$
$I_I$	Input HIGH Current	$V_{CC} = \text{MAX.}, V_{IN} = 7.0\text{V}$				0.1	mA
$I_{SC}$	Output Short Circuit Current (Note 3)	$V_{CC} = \text{MAX.}$	-15			-100	mA
$I_{CC}$	Power Supply Current	$V_{CC} = \text{MAX.}$ (Note 4)		19	34	mA	

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.  
 2. Typical limits are at  $V_{CC} = 5.0\text{V}$ ,  $25^\circ\text{C}$  ambient and maximum loading.  
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 4.  $I_{CC}$  is measured with all outputs open; clear and load inputs grounded; and all other inputs at 4.5V

### Am25LS • 54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

## SWITCHING CHARACTERISTICS

(T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0V)

Parameters	Description	Am25LS			Am54LS/74LS			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t <sub>PLH</sub>	CP <sub>U</sub> or CP <sub>D</sub> to Q <sub>n</sub>		24	34		25	38	ns	C <sub>L</sub> = 15pF R <sub>L</sub> = 2.0kΩ
t <sub>PHL</sub>			28	39		31	47		
t <sub>PLH</sub>	CP <sub>U</sub> to TC <sub>U</sub>		10	15		17	26	ns	
t <sub>PHL</sub>			10	15		21	33		
t <sub>PLH</sub>	CP <sub>D</sub> to TC <sub>D</sub>		10	15		16	24	ns	
t <sub>PHL</sub>			11	17		21	33		
t <sub>PLH</sub>	A-D to Q <sub>n</sub> Output		13	18		—	—	ns	
t <sub>PHL</sub>			27	38		—	—		
t <sub>PLH</sub>	A-D to TC <sub>U</sub> Output		35	49		—	—	ns	
t <sub>PHL</sub>			19	27		—	—		
t <sub>PLH</sub>	A-D to TC <sub>D</sub> Output		26	36		—	—	ns	
t <sub>PHL</sub>			28	39		—	—		
t <sub>PHL</sub>	MR Input to Q <sub>n</sub> Output		20	29		22	35	ns	
t <sub>PLH</sub>	MR Input to TC <sub>U</sub> Output		25	35		—	—	ns	
t <sub>PHL</sub>	MR Input to TC <sub>D</sub> Output		16	22		—	—	ns	
t <sub>PLH</sub>	P <sub>L</sub> Input to Q <sub>n</sub> Output		20	29		27	40	ns	
t <sub>PHL</sub>			25	36		29	40		
t <sub>PLH</sub>	P <sub>L</sub> Input to TC <sub>U</sub> Output		31	45		—	—	ns	
t <sub>PHL</sub>			30	42		—	—		
t <sub>PLH</sub>	P <sub>L</sub> Input to TC <sub>D</sub> Output		30	42		—	—	ns	
t <sub>PHL</sub>			24	34		—	—		
t <sub>s</sub>	Data Set-up Time A-D Input to P <sub>L</sub> Input	Load 1	5.0			—	—	ns	
		Load 0	15			20	—	ns	
t <sub>s</sub>	Set-up Time, P <sub>L</sub> Input to CP <sub>U</sub> or CP <sub>D</sub>		9.0			—	—	ns	
t <sub>s</sub>	Set-up Time, Clear Recovery (In-Active) to CP <sub>U</sub> or CP <sub>D</sub>		5.0			—	—	ns	
t <sub>h</sub>	Data		0			0	—	ns	
t <sub>pw(0)</sub>	Pulse Width	CP <sub>U</sub>	11			20	—	ns	
		CP <sub>D</sub>	11			20	—		
		P <sub>L</sub>	9.0			20	—		
t <sub>pw(1)</sub>	Pulse Width	MR	15			20	—	ns	
f <sub>max</sub>	Maximum Clock Frequency, Count Up or Down (Note 1)		35	45		25	32	MHz	

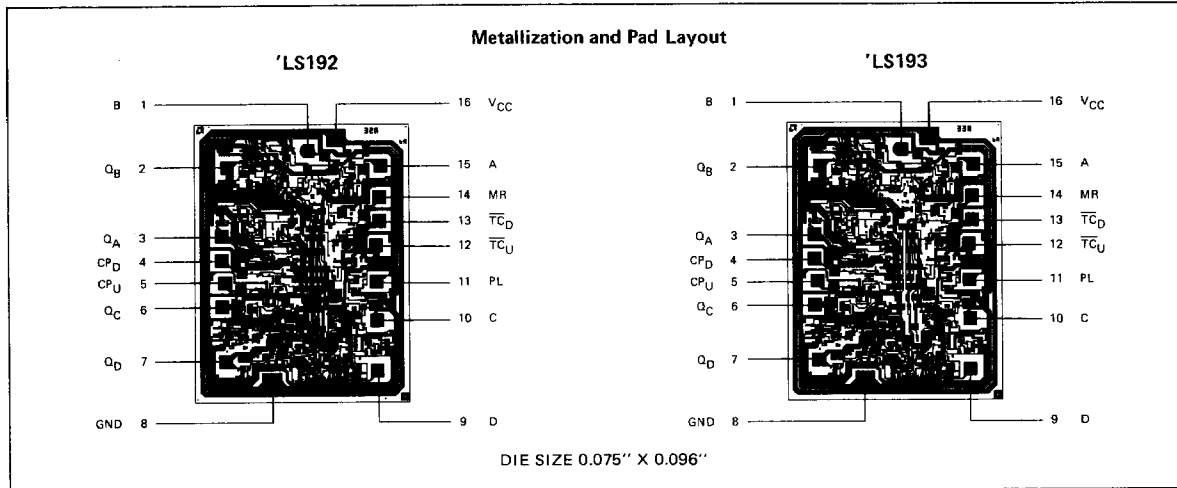
Note 1. Per industry convention, f<sub>max</sub> is the worst case value of the maximum device operating frequency with no constraints on t<sub>r</sub>, t<sub>f</sub>, pulse width or duty cycle.

# Am25LS/54LS/74LS192/193

## Am25LS192, Am25LS193 ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE\*

Parameters	Description	Am25LS COM'L		Am25LS MIL		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub>	CP <sub>U</sub> or CP <sub>D</sub> to Q <sub>n</sub>		44		52	ns	C <sub>L</sub> = 50pF R <sub>L</sub> = 2.0kΩ
			54		67		
t <sub>PLH</sub>	CP <sub>U</sub> to TC <sub>U</sub>		22		26	ns	
			23		27		
t <sub>PLH</sub>	CP <sub>D</sub> to TC <sub>D</sub>		22		26	ns	
			23		27		
t <sub>PLH</sub>	A-D to Q <sub>n</sub> Output		26		31	ns	
			52		63		
t <sub>PLH</sub>	A-D to TC <sub>U</sub> Output		66		80	ns	
			38		46		
t <sub>PLH</sub>	A-D to TC <sub>D</sub> Output		50		60	ns	
			54		66		
t <sub>PHL</sub>	MR Input to Q <sub>n</sub> Output		41		50	ns	
t <sub>PLH</sub>	MR Input to TC <sub>U</sub> Output		49		60	ns	
t <sub>PHL</sub>	MR Input to TC <sub>D</sub> Output		32		38	ns	
t <sub>PLH</sub>	P <sub>L</sub> Input to Q <sub>n</sub> Output		41		50	ns	
			53		67		
t <sub>PLH</sub>	P <sub>L</sub> Input to TC <sub>U</sub> Output		63		79	ns	
			60		75		
t <sub>PLH</sub>	P <sub>L</sub> Input to TC <sub>D</sub> Output		60		75	ns	
			48		60		
t <sub>s</sub>	Data Set-up Time A-D Input to P <sub>L</sub> Input	Load 1	5.0		5.0	ns	
		Load 0	20		23		
t <sub>s</sub>	Set-up Time, P <sub>L</sub> Input to CP <sub>U</sub> or CP <sub>D</sub>		13		18	ns	
t <sub>s</sub>	Set-up Time, Clear Recovery (In-Active) to CP <sub>U</sub> or CP <sub>D</sub>		7.0		9.0	ns	
t <sub>h</sub>	Data		0		0	ns	
t <sub>pw(0)</sub>	Pulse Width	CP <sub>U</sub>	15		17	ns	
		CP <sub>D</sub>	15		17		
		P <sub>L</sub>	13		17		
t <sub>pw(1)</sub>	Pulse Width	MR	18		21		
f <sub>max</sub>	Maximum Clock Frequency, Count Up or Down (Note 1)		25		20	MHz	

\* AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.



## FUNCTION TABLE

INPUTS								OUTPUTS						Conditions
Clock		Clear	Load	Data				Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Borrow	Carry	
Up	Down			A	B	C	D							
X	L	H	X	X	X	X	X	L	L	L	L	L	H	Clear
X	H	H	X	X	X	X	X	L	L	L	L	H	H	
X	X	L	L	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	X	X	Load
H	↑	L	H	X	X	X	X	Count Down				H	H	Except at borrow
H	L	L	H	X	X	X	X	L	L	L	L	L	H	Borrow
H	H	L	H	X	X	X	X	L	L	L	L	H	H	
↑	H	L	H	X	X	X	X	Count up				H	H	Except at carry
L	H	L	H	X	X	X	X	H	H	H	H	H	L	Carry (193 only)
H	H	L	H	X	X	X	X	H	H	H	H	H	H	
L	H	L	H	X	X	X	X	H	L	L	H	H	L	Carry (192 only)
H	H	L	H	X	X	X	X	H	L	L	H	H	H	

H = HIGH    X = Don't care  
L = LOW    ↑ = LOW-to-HIGH transition

D = A LOW or a HIGH and the respective output will assume the same state.

## DEFINITION OF FUNCTIONAL TERMS

**MR** Clear. The clear input to the counter overrides all other inputs. When the clear input is HIGH, the Q outputs are set LOW independent of the other inputs.

**PL** Load. The load input performs asynchronous parallel load of the data on the A, B, C, and D inputs. When the load input is LOW, the Q<sub>i</sub> outputs will follow the parallel inputs regardless of the clock inputs.

**A, B, C, D** The four parallel inputs to the counter flip-flops.

**CP<sub>U</sub>** Count up. A clock input causing the counter to change state in an increasing binary number direction. Counting occurs on the LOW-to-HIGH transition of the clock.

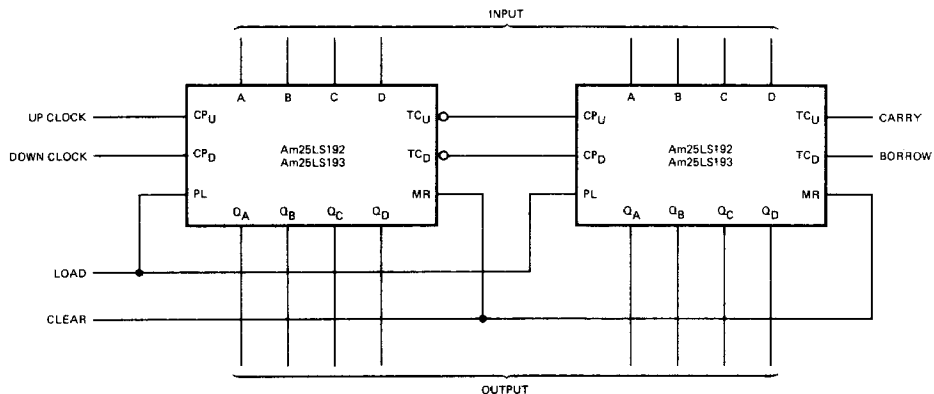
**CP<sub>D</sub>** Count down. A clock input causing the counter to change state in a decreasing binary number direction. The state change occurs on the LOW-to-HIGH transition.

**Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, Q<sub>D</sub>** The four outputs of the counter representing the LSB to MSB, respectively.

**TC<sub>U</sub>** Carry output. A clock output that indicates the maximum upper binary number has been reached. For the 'LS192, TC<sub>U</sub> indicates that the "9" state has been reached and the up clock is LOW. For the 'LS193, TC<sub>U</sub> indicates that the "15" state has been reached and the up clock is LOW.

**TC<sub>D</sub>** Borrow output. A clock output indicating that the "0" state has been reached and the down clock is LOW.

## APPLICATION



8-Bit Up/Down Counter with Parallel Load