

Am25LS299 • Am54LS/74LS299

8-Bit Universal Shift/Storage Register

DISTINCTIVE CHARACTERISTICS

- Four operational modes: shift left, shift right, parallel load, hold
- Common input/output pins
- Three-state outputs
- Buffered asynchronous master clear
- Separate shift right serial input and shift left serial input for easy cascadability
- Am25LS devices offer the following improvements over Am54/74LS
 - Higher speed
 - 50mV lower V_{OL} at $I_{OL} = 8mA$
 - Twice the fan-out over military range
 - 440 μA source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

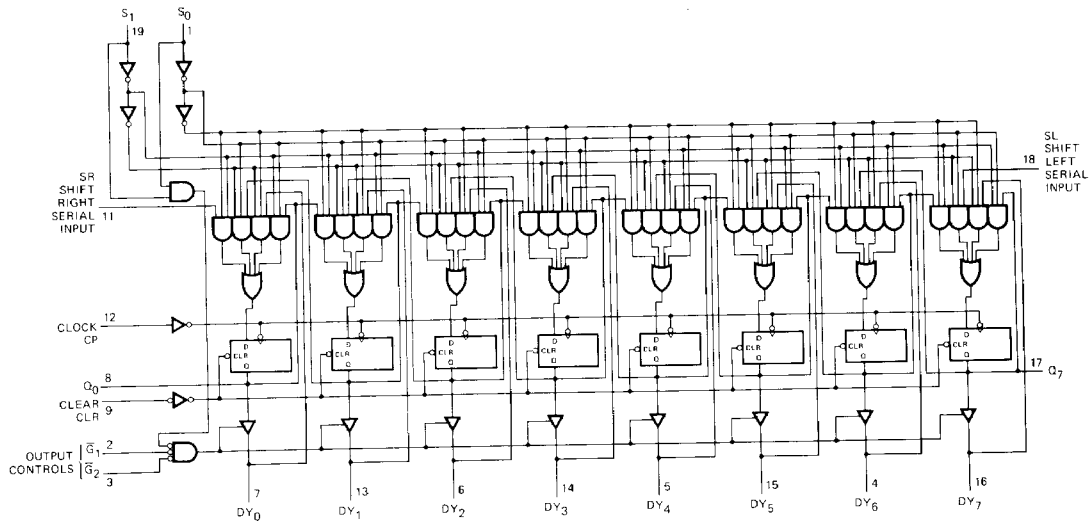
The Am25LS299 and Am54LS/74LS299 are eight-bit universal shift/storage registers with three-state outputs. Four modes of operation are possible: hold (store), shift left, shift right, and load data.

Parallel load inputs and register outputs are multiplexed to reduce the total number of package pins. Separate continuous outputs are also provided for flip-flop A and H. These devices can be cascaded to N-bit words easily.

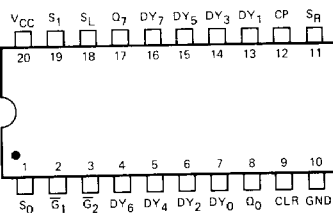
A separate active low asynchronous clear input is used to reset the register. Whenever the clear input is LOW, all internal flip-flops are set LOW independent of all other inputs. See the Am25LS23 for the identical logic function to the Am25LS299 and Am54LS/74LS299, but with synchronous clear capability.

Note: The Advanced Micro Devices' LS299 products were designed prior to publication of data sheets by T.I. Review specifications for possible differences.

LOGIC DIAGRAM

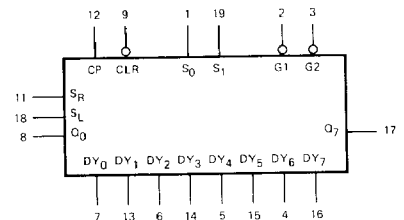


CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

Am25LS299

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 5\%$ MIN. = 4.75V MAX. = 5.25VMIL $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{MIN.}$ $V_{IN} = V_{IH}$ or V_{IL}	Q ₀ , Q ₇	$I_{OH} =$ -440 μA	MIL	2.5		Volts
					COM'L	2.7		
		DY ₀ -DY ₇	MIL, $I_{OH} = -1.0\text{mA}$		2.4			
			COM'L, $I_{OH} = -2.6\text{mA}$		2.4			
V_{OL}	Output LOW Voltage	$V_{CC} = \text{MIN.}$ $V_{IN} = V_{IH}$ or V_{IL}		$I_{OL} = 4.0\text{mA}$		0.25	0.4	Volts
				$I_{OL} = 8.0\text{mA}$		0.35	0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL		0.7	Volts	
				COM'L		0.8		
V_I	Input Clamp Voltage	$V_{CC} = \text{MIN.}$, $I_{IN} = -18\text{mA}$					-1.5	Volts
I_{IL}	Input LOW Current	$V_{CC} = \text{MAX.}$, $V_{IN} = 0.4\text{V}$		S ₀ , S ₁		-0.8	mA	
				All Others		-0.4		
I_{IH}	Input HIGH Current (Except DY _j)	$V_{CC} = \text{MAX.}$, $V_{IN} = 2.7\text{V}$		S ₀ , S ₁		40	μA	
				All Others		20		
I_I	Input HIGH Current (Except DY _j)	$V_{CC} = \text{MAX.}$	$V_{IN} = 7.0\text{V}$ $V_{IN} = 5.5\text{V}$	S ₀ , S ₁		0.2	mA	
				$\bar{G}_1, \bar{G}_2, \text{CLR}, \text{CP}$		0.1		
				All Others		0.1		
I_{OZ}	Off-State (High-Impedance) Output Current at DY _j	$V_{CC} = \text{MAX.}$		$V_O = 0.4\text{V}$		-100	μA	
				$V_O = 2.4\text{V}$		40		
I_{SC}	Output Short Circuit Current (Note 3)	$V_{CC} = \text{MAX.}$			-15		-85	mA
I_{CC}	Power Supply Current (Note 4)	$V_{CC} = \text{MAX.}$				38	60	mA

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical limits are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
 4. I_{CC} measured with clock input HIGH and output controls HIGH.

Am25LS • Am54LS/74LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	-0.5V to +V _{CC} max.
DC Input Voltage ($\bar{G}_1, \bar{G}_2, \text{CLR}, \text{CP}, \text{S}_0, \text{S}_1$)	-0.5V to +7.0V
DC Input Voltage (Others)	-0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	-30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{V } +5\%$ MIN. = 4.75V MAX. = 5.25V
 MIL $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V } +10\%$ MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

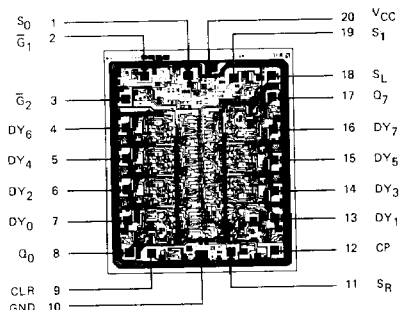
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{MIN.}$ $V_{IN} = V_{IH}$ or V_{IL}	Q_0, Q_7	$I_{OH} = -400\mu\text{A}$	MIL 2.5		Volts	
					COM'L 2.7			
		DY_0-DY_7	MIL, $I_{OH} = -1.0\text{mA}$	2.4				
			COM'L, $I_{OH} = -2.6\text{mA}$	2.4				
V_{OL}	Output LOW Voltage	$V_{CC} = \text{MIN.}$ $V_{IN} = V_{IH}$ or V_{IL}		$I_{OL} = 4.0\text{mA}$		0.25	0.4	Volts
				$I_{OL} = 8.0\text{mA}$ 74LS only		0.35	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0		Volts	
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL		0.7	Volts	
				COM'L		0.8		
V_I	Input Clamp Voltage	$V_{CC} = \text{MIN.}, I_{IN} = -18\text{mA}$					-1.5	Volts
I_{IL}	Input LOW Current	$V_{CC} = \text{MAX.}, V_{IN} = 0.4\text{V}$		S_0, S_1		-0.8	mA	
				All Others		-0.4		
I_{IH}	Input HIGH Current (Except DY_i)	$V_{CC} = \text{MAX.}, V_{IN} = 2.7\text{V}$		S_0, S_1		40	μA	
				All Others		20		
I_I	Input HIGH Current (Except DY_i)	$V_{CC} = \text{MAX.}, V_{IN} = 5.5\text{V}$		S_0, S_1		0.2	mA	
				All Others		0.1		
I_{OZ}	Off-State (High-Impedance) Output Current at DY_i	$V_{CC} = \text{MAX.}$		$V_O = 0.4\text{V}$		-100	μA	
				$V_O = 2.4\text{V}$		40		
I_{SC}	Output Short Circuit Current (Note 3)	$V_{CC} = \text{MAX.}$			-15		-100	mA
I_{CC}	Power Supply Current (Note 4)	$V_{CC} = \text{MAX.}$				35	60	mA

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical limits are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
 4. I_{CC} measured with clock input HIGH and output controls HIGH.

DEFINITION OF FUNCTIONAL TERMS

- SR** Shift right data input to Q_0
SL Shift left data input to Q_7
Clear Active LOW synchronous input forcing the Q_0 through Q_7 register to see LOW conditions, visible only if outputs are enabled
Clock A LOW-to-HIGH transition will result in the register changing state to next state as described by mode and input data condition
 S_0, S_1 Mode selection control lines used to control input (output during load) conditions
 \bar{G}_1, \bar{G}_2 Active LOW input to control three-state output in active LOW AND configuration
 Q_0, Q_7 The only two direct outputs; used to cascade shift operations
 DY_0-DY_7 Input/Output line dependent on mode and output control. Input only with mode select LOAD. Output in all other modes but subject to output select (G_1, G_2).

Metallization and Pad Layout



DIE SIZE 0.096" X 0.112"

WITCHING CHARACTERISTICS

 $T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

Parameters	Description	Am25LS			Am54LS/74LS			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Clock to Q_i		18	26			30	ns	$C_L = 15\text{pF}$ $R_L = 2.0\text{k}\Omega$
t_{PHL}			22	28			34		
t_{PLH}	Clock to DY_i		18	26			30	ns	
t_{PHL}			22	28			34		
t_{PHL}	Clear to $DY_0 - DY_7$		25	35			35	ns	
t_{PHL}	Clear to Q_0 or Q_7		25	35			35	ns	
t_{pw}	Pulse Width (Clock)	15			20			ns	
t_s	S_1, S_0 Set-up Time	12			15			ns	
t_s	DY_i or S_R, S_L Data Set-up Time	12			15			ns	
t_h	Hold Time	3.0			3.0			ns	
t_{ZH}	$S_1, S_0, \bar{G}_1, \bar{G}_2$ to DY_i		20	30			40	ns	
t_{ZL}			20	30			40		
t_{LZ}	$S_1, S_0, \bar{G}_1, \bar{G}_2$ to DY_i		22	33			40	ns	$C_L = 5.0\text{pF}$ $R_L = 2.0\text{k}\Omega$
t_{HZ}			15	23			30		
f_{max}	Maximum Clock Frequency (Note 1)	30	45		25			MHz	

1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

n25LS ONLY
WITCHING CHARACTERISTICS
OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L		Am25LS MIL		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{PLH}	Clock to Q_i		38		44	ns	$C_L = 50\text{pF}$ $R_L = 2.0\text{k}\Omega$
t_{PHL}			41		47		
t_{PLH}	Clock to DY_i		38		44	ns	
t_{PHL}			41		47		
t_{PHL}	Clear to $DY_0 - DY_7$		50		57	ns	
t_{PHL}	Clear to $Q_0 - Q_7$		50		57	ns	
t_{pw}	Pulse Width (Clock)	24		27		ns	
t_s	S_1, S_0 Set-up Time	20		23		ns	
t_s	DY_i or S_R, S_L Data Set-up Time	20		23		ns	
t_h	Hold Time	8		9		ns	
t_{ZH}	$S_1, S_0, \bar{G}_1, \bar{G}_2$ to DY_i		43		50	ns	
t_{ZL}			43		50		
t_{LZ}	$S_1, S_0, \bar{G}_1, \bar{G}_2$ to DY_i		43		50	ns	$C_L = 5.0\text{pF}$ $R_L = 2.0\text{k}\Omega$
t_{HZ}			34		39		
f_{max}	Maximum Clock Frequency (Note 1)	23		20		MHz	

* Performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

TRUTH TABLE

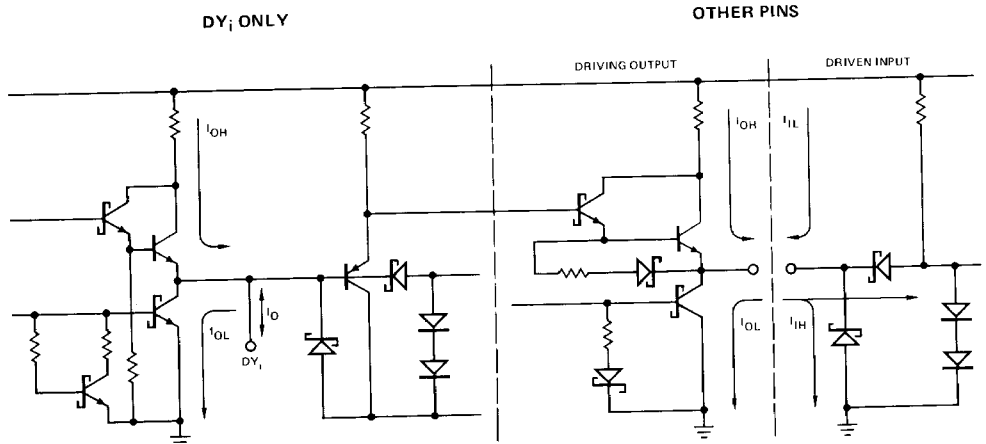
FUNCTION		INPUTS								OUTPUTS		INPUTS/OUTPUTS							
		S _R	S _L	CLEAR	CLOCK	S ₀	S ₁	\bar{G}_1	\bar{G}_2	Q ₀	Q ₇	DY ₀	DY ₁	DY ₂	DY ₃	DY ₄	DY ₅	DY ₆	DY ₇
Clear		X	X	L	X	(Note 1)		L	L	L	L	L	L	L	L	L	L	L	L
Output Control		X	X	X	X	X	X	H	L	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	L	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	H	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
M O D E	Hold	X	X	H	X	L	L	L	L	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Load (Note 2)	X	X	H	↑	H	H	X	X	A	H	A	B	C	D	E	F	G	H
	Shift Right	L	X	H	↑	H	L	L	L	L	DY ₆	L	DY ₀	DY ₁	DY ₂	DY ₃	DY ₄	DY ₅	DY ₆
	Shift Right	H	X	H	↑	H	L	L	L	H	DY ₆	H	DY ₀	DY ₁	DY ₂	DY ₃	DY ₄	DY ₅	DY ₆
	Shift Left	X	L	H	↑	L	H	L	L	DY ₁	L	DY ₁	DY ₂	DY ₃	DY ₄	DY ₅	DY ₆	DY ₇	L
	Shift Left	X	H	H	↑	L	H	L	L	DY ₁	H	DY ₁	DY ₂	DY ₃	DY ₄	DY ₅	DY ₆	DY ₇	H

L = LOW Z = High Impedance ↑ = Transition LOW to-HIGH
 H = HIGH X = Don't Care NC = No Change

Notes: 1. Either LOW to observe output
 2. In this mode DY_i are inputs.

When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

Am25LS • Am54LS/74LS
 LOW-POWER SCHOTTKY INPUT/OUTPUT
 CURRENT INTERFACE CONDITIONS

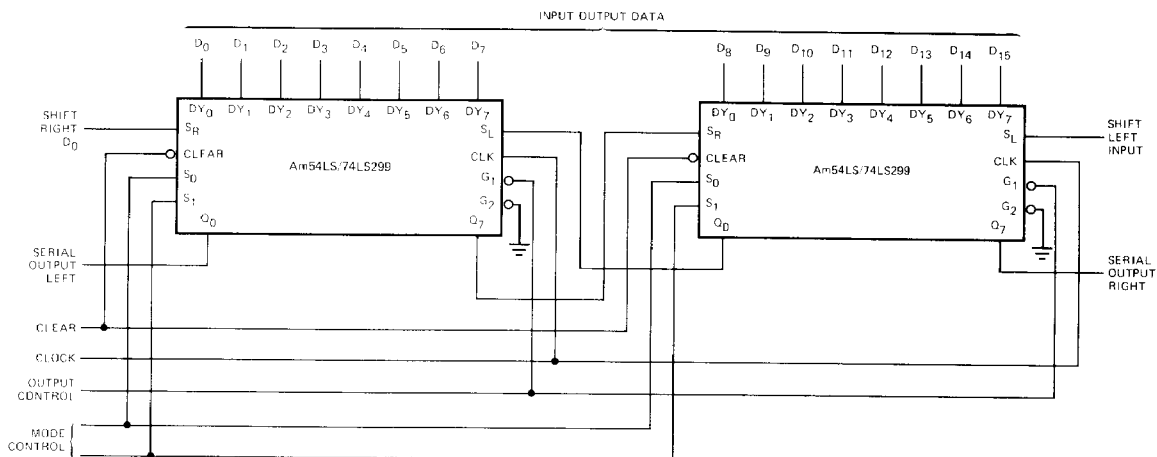


Note: Actual current flow direction shown.

ORDERING INFORMATION

Package Type	Temperature Range	Am25LS299 Order Number	Am54LS/74LS299 Order Number
Molded DIP	0°C to +75°C	AM25LS299PC	SN74LS299N
Hermetic DIP	0°C to +75°C	AM25LS299DC	SN74LS299J
Dice	0°C to +75°C	AM25LS299XC	SN74LS299X
Hermetic DIP	-55°C to +125°C	AM25LS299DM	SN54LS299J
Hermetic Flat Pak	-55°C to +125°C	AM25LS299FM	SN54LS299W
Dice	-55°C to +125°C	AM25LS299XM	SN54LS299X

APPLICATION



16-Bit Cascaded Parallel Load/Unload Shift Right/Left Register.