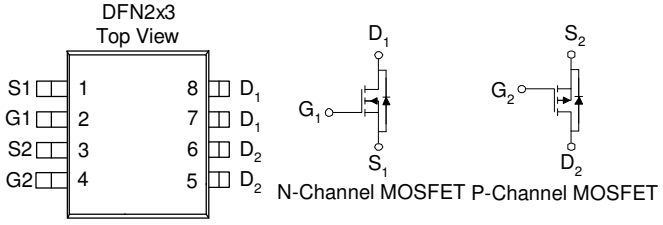
N & P-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN2X3 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.058 @ V_{GS} = 4.5V	5
	0.077 @ V_{GS} = 2.5V	4.3
-20	0.064 @ V_{GS} = -4.5V	-4.7
	0.085 @ V_{GS} = -2.5V	-4.1



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		**Symbol**	**N-Channel**	**P-Channel**	**Units**
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	±8	±8	
Continuous Drain Current[a]	T_A=25°C	I_D	5	-4.7	A
	T_A=70°C		4.1	-3.9	
Pulsed Drain Current[b]		I_{DM}	8	-8	
Continuous Source Current (Diode Conduction)[a]		I_S	4.5	-4.5	A
Power Dissipation[a]	T_A=25°C	P_D	2.1		W
	T_A=70°C		1.3		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Ambient[a]	t <= 10 sec	$R_{\theta JA}$	62.5	°C/W
	Steady State		80	°C/W

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

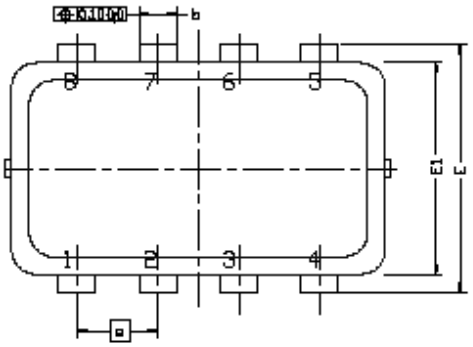
Parameter	Symbol	Test Conditions	Limits Ch	Min	Typ	Max	Unit
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 uA	N	1			V
		V_{GS} = V_{DS}, I_D = -250 uA	P	-1			
Gate-Body Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 8 V	N			100	µA
		V_{DS} = 0 V, V_{GS} = -8 V	P			-100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V	N			1	µA
		V_{DS} = -16 V, V_{GS} = 0 V	P			-1	
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55°C	N			10	µA
		V_{DS} = -16 V, V_{GS} = 0 V, T_J = 55°C	P			-10	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	N	5			A
		V_{DS} = -5 V, V_{GS} = -4.5 V	P	-5			
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 1 A	N			0.058	Ω
		V_{GS} = -4.5 V, I_D = 1 A	P			0.077	
		V_{GS} = 2.5 V, I_D = 1 A	N			0.064	
		V_{GS} = -2.5 V, I_D = -1 A	P			0.085	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 5 V, I_D = 1 A	N		10		S
		V_{DS} = -5 V, I_D = 1 A	P		5		
Diode Forward Voltage[A]	V_{SD}	I_S = 1 A, V_{GS} = 0 V	N		0.80		S
		I_S = -1 A, V_{GS} = 0 V	P		-0.83		
Dynamic[b]							
Total Gate Charge	Q_g	N-Channel V_{DS}=15V, V_{GS}=4.5V, I_D=1A P-Channel V_{DS}=-15V, V_{GS}=-4.5V, I_D=-1A	N		2		nC
			P		7		
Gate-Source Charge	Q_{gs}		N		0.4		
			P		1		
Gate-Drain Charge	Q_{gd}		N		0.7		
			P		2		
Turn-On Delay Time	$t_{d(on)}$	N-Chaneel V_{DD}=15V, V_{GS}=4.5V, I_D=1A , R_{GEN}=15Ω, P-Channel V_{DD}=-15V, V_{GS}=-4.5V, I_D=-1A R_{GEN}=15Ω	N		6		nS
			P		10		
Rise Time	t_r		N		9		
			P		1		
Turn-Off Delay Time	$t_{d(off)}$		N		5		
			P		11		
Fall-Time	t_f		N		16		
			P		12		

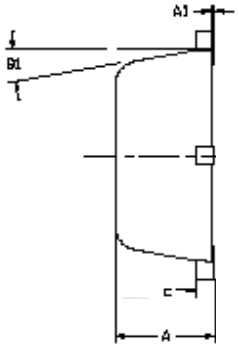
Notes

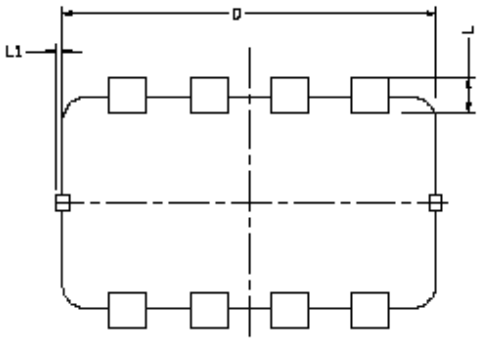
a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information







DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.08	0.152	0.25	0.003	0.006	0.010
D	3.00 BSC			0.118 BSC		
E	2.00 BSC			0.079 BSC		
E1	1.70 BSC			0.067 BSC		
e	0.65 BSC			0.026 BSC		
L	0.20	0.275	0.400	0.008	0.011	0.0157
L1	0	---	0.100	0	---	0.004
θ1	0°	10°	12°	0°	10°	12°