Final

Am6112

Microprocessor-Compatible 12-Bit A/D Converter

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

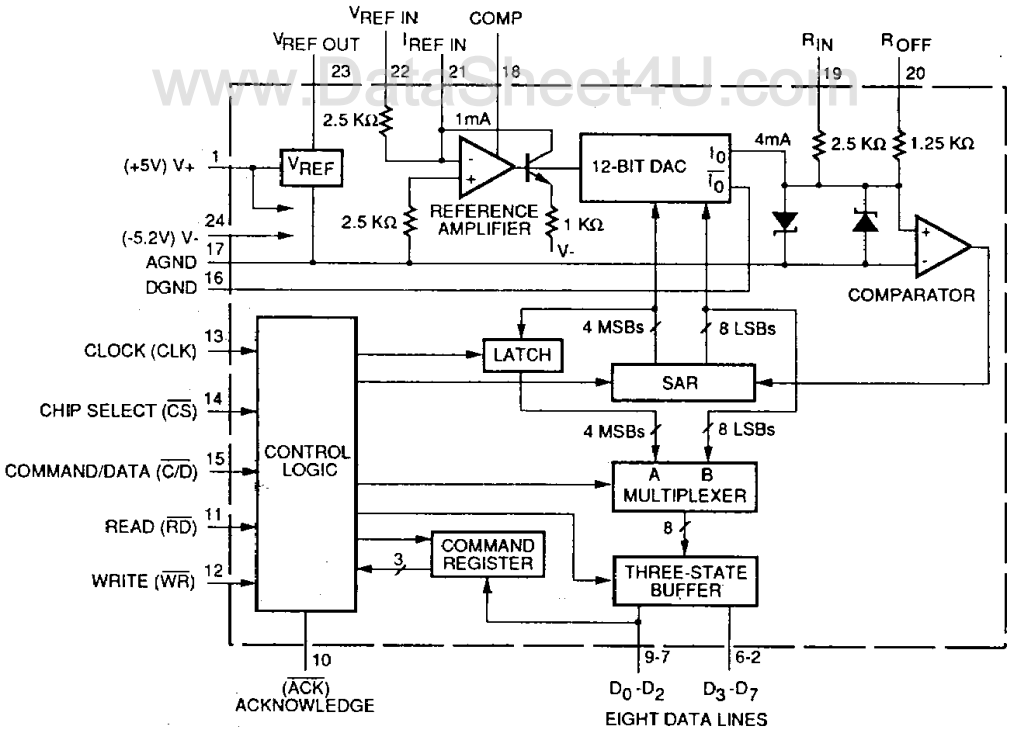
- First totally monolithic, high-speed 12-bit ADC
- 6 µs typical conversion time
- Internal precision voltage reference
- No missing codes
- Easy interfacing with 8- and 16-bit microprocessors
- Internal command register for programmable modes of operation
- Offset binary or two's complement output code
- 0 to 10 V, or ±5 V input range
- 24-pin package
- Segmented DAC architecture for monotonic operation
- Available in two accuracy ranges

GENERAL DESCRIPTION

The Am6112 is a fully monolithic microprocessor-compatible 12-bit high-speed analog-to-digital converter. The Am6112 high-speed ADC contains a precision reference, DAC, comparator, SAR, scale resistors, output three-state buffers and comprehensive control logic, enabling the device to be interfaced with a variety of microprocessors. The Am6112 is capable of completing a 12-bit conversion in typically 6 µs and can handle input voltage ranges of 0 to +10 V, and ±5 V without external components.

The Am6112 has four modes of microprocessor operation, and a stand-alone mode. These modes are software programmable, except for the stand-alone mode. Applications include analog I/O subsystems, servo-control, and high-speed digital signal processing of analog events.

BLOCK DIAGRAM



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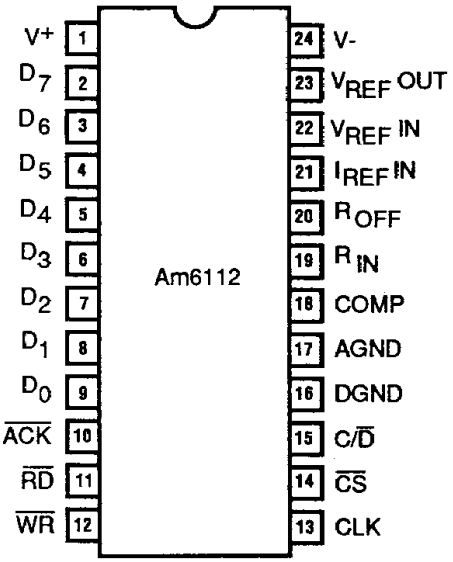
CONNECTION DIAGRAM
Top View

D-24-1



Note: Pin 1 is marked for orientation.

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ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

Am6112 **D** **C**

e. OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
D = 24-Pin Ceramic DIP (CD 024)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am6112
Microprocessor-Compatible 12-Bit A/D Converter

Valid Combinations	
Am6112	DC, DCB
Am6112-10	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$\overline{ACK}$

Active-LOW digital open-collector output used to indicate conversion complete and data valid. In Modes 0, 1, and 2 $\overline{ACK}$ is gated internally with $\overline{RD}$ and $\overline{WR}$ in order to generate WAIT states for the host processor. In Modes 3 and 4 $\overline{ACK}$ is ungated and reflects the converter status at all times.

$\overline{ACK}$ = 1 means a conversion is in progress.

$\overline{ACK}$ = 0 means that conversion is complete.

AGND

Analog ground.

C/$\overline{D}$

Digital input used in conjunction with $\overline{WR}$ to load command register and in conjunction with $\overline{RD}$ (except for Mode 2) to select HIGH or LOW byte for READ. When C/$\overline{D}$ is HIGH and $\overline{WR}$ is asserted, data present on $D_0 - D_2$ are loaded into the command register to set up output code and conversion mode. When C/$\overline{D}$ is LOW and $\overline{RD}$ is asserted, the lower byte (8 LSBs) is output to $D_0 - D_7$ (D_0 is the LSB). When C/$\overline{D}$ is HIGH and $\overline{RD}$ is asserted, the upper byte (4 MSBs) is output to $D_0 - D_3$. In Mode 2 the output data control is done internally and is not accessible via the C/$\overline{D}$ pin.

CLK

Clock input controls the internal ADC conversion process.

COMP

Compensation pin for the internal reference amplifier. Connect a 0.01 µF capacitor to V–.

$\overline{CS}$

Active-LOW digital input used to enable the Am6112 for I/O operations and to initiate conversions in Mode 2 (see Status Truth Table). If the Am6112 has been initialized for Mode 2, $\overline{CS}$ HIGH will hold the SAR reset and the HIGH-to-LOW transition of $\overline{CS}$ will start the first conversion. After $\overline{CS}$ is LOW and the first conversion is completed in Mode 2, subsequent conversions are initiated by $\overline{RD}$.

$D_0 - D_7$

Three-state data lines. $D_0 - D_2$ are bidirectional data lines, while $D_3 - D_7$ are strictly output data lines. Data is loaded into the internal command register via $D_0 - D_2$ to select one of four modes of operation. $D_0 - D_7$ are used to output the eight LSBs ($B_0 - B_7$). $D_0 - D_3$ are used to output the four MSBs ($B_8 - B_{11}$) of the 12-bit data. $D_4 - D_7$ output the sign bit (B_{11}) when two's complement output code is selected. D_0 is the LSB and D_7 is the MSB in this format.

DGND

Digital ground.

$I_{REF}IN$

External reference current input.

$\overline{RD}$

Active-LOW digital input which starts conversions in Modes 1 and 2 and reads the SAR data in all modes. When used in conjunction with $\overline{WR}$, $\overline{RD}$ forces the Am6112 into a Mode 4 (stand-alone) conversion cycle. SAR data is read in two bytes. The reading of the HIGH byte ($B_8 - B_{11}$) or LOW byte is user-selectable via the C/$\overline{D}$ pin (see Status Truth Table) except during Mode 2 (DMA-Compatible Mode).

R_{IN}

Analog voltage input.

R_{OFF}

Offset voltage input. Leave open or ground for unipolar operation. Connect to AGND for high-speed unipolar operation. Connect to $V_{REF}OUT$ (buffered) for bipolar operation.

V+

+5-V power supply input.

V–

–5.2-V power supply input.

$V_{REF}OUT$

2.5-V internal voltage reference output.

$V_{REF}IN$

Connected to an external voltage reference or $V_{REF}OUT$ to establish a reference current for the DAC bit currents.

$\overline{WR}$

Active-LOW digital input which resets the SAR and starts a conversion cycle in Modes 0 and 3. When used in conjunction with $\overline{RD}$, $\overline{WR}$ forces the Am6112 into a Mode 4 (stand-alone) conversion cycle. When $\overline{WR}$ is asserted with the C/$\overline{D}$ pin held HIGH, data present on D_0, D_1, and D_2 (pins 9, 8, and 7 respectively) are loaded into the command register to set up output code (offset binary or two's complement) and conversion mode (Modes 0 – 3).

MAXIMUM RATINGS

Storage Temperature	–65 to +150°C
Lead Temperature (Soldering 60 sec)	300°C
Max Package Dissipation	1 W
V+ to DGND	–0.3 to +7.0 V
V– to DGND	+0.3 to –7.0 V
Max Differential V+ to V–	±12 V
Digital Inputs to DGND	–0.5 to +6.0 V
AGND to DGND	±1 V
V_{REF} Max Output Current	15 mA
Max Input Current at $I_{REF}IN$	2 mA
Voltage at $V_{REF}IN$, $I_{REF}IN$	V– to V+
Voltage at R_{IN}, R_{OFF}	±18 V
Open-Collector Voltage	V+

Stresses above those listed under MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Operating Temperature	0 to +70°C
Die Size	0.142 x 0.176 in.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(These specifications apply for V+ = +5 V ±5%, V– = –5.2 V +5%, V_{REF} connected per test circuit, T_A = 0 to +70°C, f_{CLOCK} = 150 kHz, 0 to 10-V input range, R_{OFF} connected to AGND stand-alone mode, unless otherwise stated.)

Parameter	Description		Test Conditions	Min.	Typ.	Max.	Unit
Transfer Characteristics							
Symbol	Resolution			12	12	12	Bits
DNL	Differential Nonlinearity	Am6112	T_A = +25°C		±0.5	±1	LSB
					±0.5	±2	
		Am6112-10	T_A = +25°C		±1.0	±2	
					±1.0	±3	
LIN	Linearity	Am6112	T_A = +25°C		±0.8	±2	LSB
					±0.8	±2	
		Am6112-10	T_A = +25°C		±0.8	±2	
					±0.8	±3	
	Inherent Quantization Error					±1/2	LSB
	Unipolar Gain Error		V_{IN} = 0 to +10 V		±5	±20	LSB
	Unipolar Offset Error				±2	±10	LSB
	Bipolar Gain Error R_{OFF} Connected to V_{REFOUT}		V_{IN} = –5 V to +5 V		±5	±20	LSB
	Bipolar Offset Error R_{OFF} Connected to V_{REFOUT}				±2	±20	LSB
+PSR	Positive Power Supply Sensitivity		V+ = +5 V ±5%		0.02	0.3	%FS
–PSR	Negative Power Supply Sensitivity		V– = –5.2 V ±5%		0.02	0.15	%FS
Internal Reference							
V_{REF}	Reference Voltage V_{REFOUT} Connected to V_{REFIN}		I_{REF} = 1 mA	2.490	2.5	2.510	V
$\Delta V_{REF}/V_{REF}$	Load Regulation		I_{REF} = 0 mA to 4 mA		0.04	0.2	$\%V_{REF}$
$\Delta V_{REF}/V_{REF}$	Line Regulation		V+ = +5 V ±5%, –5.2 V ±5%		0.02	0.3	$\%V_{REF}$
Analog Input (Pin 19)							
R_{IN}	**Input Resistance**						
	±5 V				2.5		kΩ
	0 to 10 V				2.5		kΩ
C_{IN}	**Input Capacitance**						
	R_{IN}, R_{OFF}, V_{REFIN}				4		pF
Digital Inputs							
	Logic Level Input Voltage						
V_{IH}	Logic 1			2.0			V
V_{IL}	Logic 0					0.8	V
	Logic Level Input Current						
I_{IH}	Logic 1		V_{IN} = 2.7 V		1.0	10	µA
I_{IL}	Logic 0		V_{IN} = 0.4 V		0.1	5	µA
C_{IN}	CLOCK				4		pF
Digital Outputs							
	Logic Level Output Voltages						
V_{OH}	Logic 1		I_{OH} = –400 µA	2.4	3.5		V
V_{OL}	Logic 0		I_{OL} = 4 mA		0.38	0.5	V
I_{SC}	Output Short-Circuit Current		V_O = 2.4 V		–35		mA
I_{OZH}	Three-State Leakage HIGH D_3 to D_7		V_O = 2.4 V		0.01	2	µA
I_{OZL}	Three-State Leakage LOW D_3 to D_7		V_O = 0.4 V		0.1	2	µA
I_{OZH}	Three-State Leakage HIGH D_0 to D_2		V_O = 2.4 V		1.0	10	µA
I_{OZL}	Three-State Leakage LOW D_0 to D_2		V_O = 0.4 V		0.1	5	µA
Power Requirements							
I+	Positive Supply Current				30	45	mA
I–	Negative Supply Current			–75	–50		mA
P_D	Power Dissipation				410	646	mW
V+	Positive Supply Range			4.75	5.00	5.25	V
V–	Negative Supply Range			–4.94	–5.20	–5.46	V

SYSTEM TIMING

(These specifications apply for V+ = +5 V, V– = –5.2 V, V_{REF} connected per test circuit, T_A = +25°C, 0 to +10-V input range, unles otherwise stated.)

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_{CONV}	Conversion Time R_{OFF} Connected to AGND (unipolar)		6	10*	µs
t_{CONV}	Conversion Time R_{OFF} Open (unipolar)		15		µs
CLK T_{THL}	CLK HIGH to LOW			100	ns
CLK T_{TLH}	CLK LOW to HIGH		5	10	ns
CLK Duty Cycle	% Time for which CLK is HIGH	30	50	70	%
CLK Freq	CLK Frequency R_{OFF} Connected to AGND (unipolar)		2 • 0		MHz

*This parameter is not tested in production but is instead guaranteed by design.

DEFINITION OF TERMS

Resolution: The number of possible analog input levels an A/D will resolve. Expressed as either the number of output bits, or 1 part in 2^n where n is the number of bits.

Differential Nonlinearity: The deviation between the actual code width of an A/D from the ideal code width. The code width is defined as the range of analog input which produces a given digital output code. An ideal value of a code width is equivalent to FSR/2^n, where FSR is full-scale range and n is the number of bits.

Linearity: The deviation of each individual code from an ideal straight line transfer curve between zero and full scale, with the straight line measured from the middle of each particular code.

Inherent Quantization Error: Quantization Error is a direct consequence of the resolution of the A/D. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an *inherent* ±1/2 LSB conversion error even for a perfect A/D.

Gain Error: Defined as the difference between the analog input levels required to produce the first and the last digital output code transitions with gain error as a measure of the deviation between the actual gain from the ideal gain.

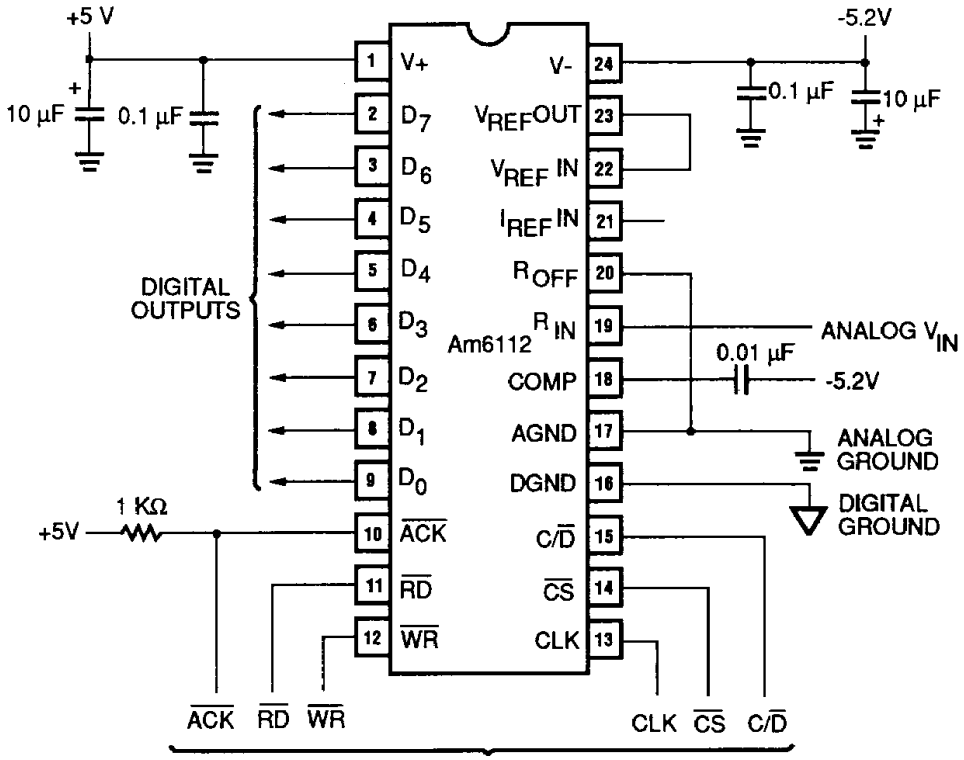
Unipolar Offset Error: Difference between the ideal (+1/2 LSB) and the actual analog input level required to produce the first digital code transition (00 . . . .00 to 00 . . . . 01) over the complete temperature range.

Bipolar Offset Error: Difference between the ideal (1/2 FSR – 1/2 LSB) and the actual analog input level required to produce the major carry output digital code transition (from 01 . . . . 11 to 10 . . . . 00).

Power Supply Sensitivity: A measure of the change in gain of the A/D resulting from a change in supply voltage. Usually expressed in total %FS for a percentage change in supply voltage.

Conversion Time: The measure of how long it takes for the A/D to arrive at the correct digital output code. It is the time between $\overline{ACK}$ HIGH to $\overline{ACK}$ LOW which signifies that the conversion is completed.

TEST CIRCUIT—Top View
Unipolar—Stand Alone—R_{OFF} Connected to Analog Ground



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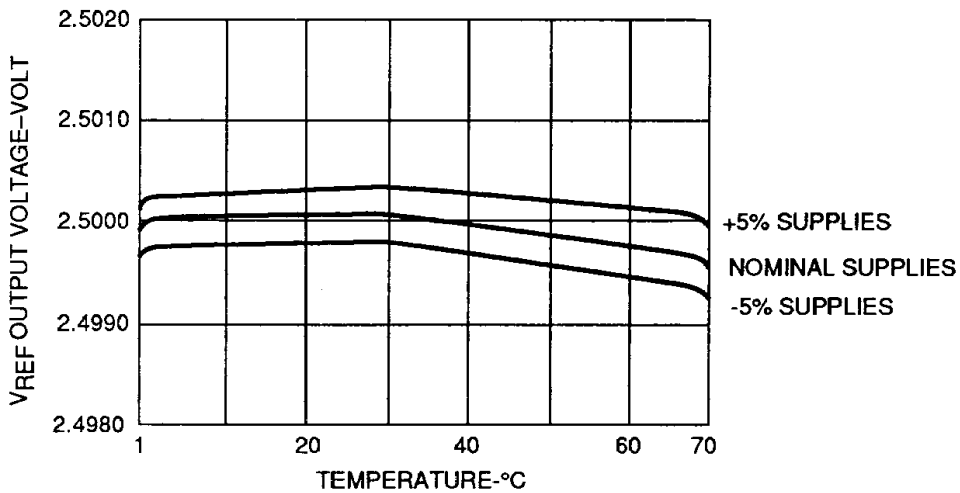
CHARACTERISTIC CURVES
Typical Reference Voltage vs Temperature and Power Supply



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CALIBRATION

Unipolar Configuration (Figure 1)

The Am6112 contains all the active components required to perform a complete 12-bit A/D conversion (except clock). All that is necessary, in most situations, is the connection of the power supplies (+5 V and –5.2 V), analog input, and conversion initiation command, discussed later. The Am6112 has a nominal 1/2 LSB offset so that the exact analog input for a given code will be in the middle of the code. If the gain error (full-scale) trim is not required, short pin 22 to 23 and delete R_5. If offset trim is not required delete R_1, R_2, and R_3.

Unipolar Calibration (Figure 1)

The initial offset error can be trimmed by R_3. The first A/D transition (0000 0000 0000 to 0000 0000 0001) should occur for an input level of +1/2 LSB (1.22 mV). While continuously monitoring the A/D output, adjust R_3 for 50% duty cycle of the LSB (D_0).

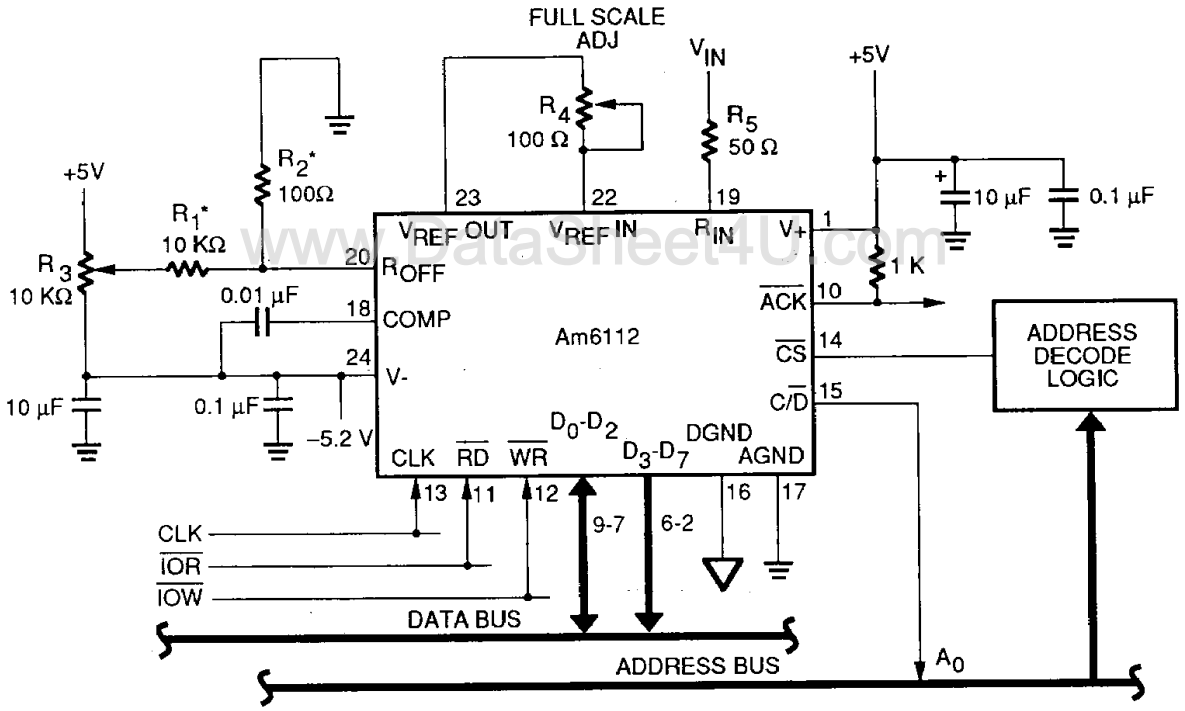
The gain error (full-scale) trim is done by applying a signal 1-1/2 LSBs below the nominal full scale (9.9963 V for a 10-V input range). R_4 is trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111). While continuously monitoring the A/D output, adjust R_4 for 50% duty cycle of the LSB (D_0).

Bipolar Configuration (Figure 2)

If calibration is not required delete R_1, R_2, and R_3.

Bipolar Calibration (Figure 2)

Bipolar calibration is similar to unipolar calibration. First, a signal +1/2 LSB (–4.9976 V) above negative full-scale (–4.9988 V for the ±5 V input range) is applied to R_3 and potentiometer R_1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1/2 LSB (4.9963 V) below positive full-scale (4.9976 V), is applied and potentiometer R_2 is trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).



*Remove R_2 and make R_1 = 1 MΩ for lowest noise, medium speed operation.

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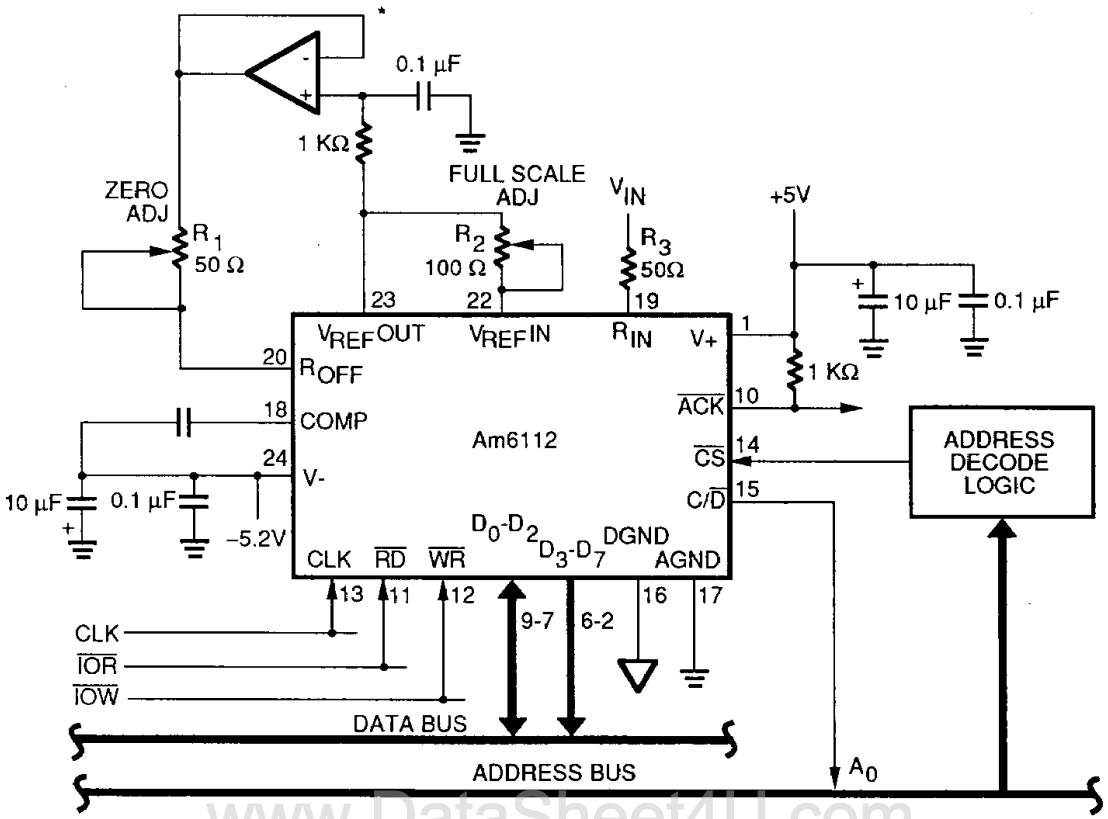
Figure 1. Am6112 Unipolar Configuration (R_{OFF} low impedance → high speed)



*A low impedance Op Amp is recommended for optimum performance due to fast switching currents appearing at R_{OFF}.

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Figure 2. Am6112 Unipolar Configuration

THEORY OF OPERATION

The Am6112 is a fully microprocessor-compatible programmable 12-bit A/D converter. The device is initialized by writing a 3-bit word into the internal command register via the bidirectional data pins $D_0 - D_2$; in this operation, bits D_1 and D_2 configure the converter into one of four modes, while D_0 provides the choice of either offset-binary or two's complement output code. A fifth mode is a unique stand-alone mode in which the internal command register is programmed whenever the control inputs Read ($\overline{RD}$) and Write ($\overline{WR}$) are LOW together.

The Am6112 has the standard microprocessor peripheral control lines, Chip Select ($\overline{CS}$), Write ($\overline{WR}$), Read ($\overline{RD}$), plus one additional line, Command/Data (C/$\overline{D}$). The C/$\overline{D}$ control qualifies both the read and write operations. It defines a write operation as either an initialization or an external start conversion command, and during read cycles it steers either the upper or lower data byte to the data outputs.

The Am6112 requires an external clock (CLK) to control the conversion speed. The status output acknowledge ($\overline{ACK}$) indicates whether a conversion is in progress (HIGH) or completed (LOW). Conversion starts on the next falling edge of the clock after the triggering event. Conversion finishes 12.5 clock cycles later.

The Successive Approximation Register performs the analog-to-digital conversion by sequentially testing the effect of removing the bit currents (B_{11} to B_0) of the D/A converter, which are all steered to the A/D summing node. The bit currents are binary scaled versions of the reference current flowing into the D/A converter reference amplifier, and the voltage comparator decides whether the bit currents should be removed or retained. The reference current is obtained from the internal reference voltage source using the scale resistor connected to $V_{REF}OUT$. The Am6112 contains the necessary gain and range selection resistors enabling bipolar signals between –5 V and +5 V, and unipolar signals from 0 to +10 V to be digitized. The device operates from +5 V and –5.2 V supplies.

STATUS TRUTH TABLE

Control Logic Inputs				Am6112 Status
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	C/$\overline{D}$	
1	X	X	X	Output Data Lines ($D_7 - D_0$) in High-Impedance State
0	0	0	0	Forced to Stand-Alone Mode Operation
0	1	0	1	Write into Command Register to Select Mode of Operation
0	0	1	0	Read eight LSBs (Low Byte), Except in Mode 2
0	0	1	1	Read four MSBs (High Byte), Except in Mode 2
0	1	0	0	Start Conversion (Modes 0, 3 and Stand-Alone)
0	0	1	0	Start Conversion, (Modes 1, 2)

APPLICATIONS INFORMATION

Depending on the processor used and throughput rate required, the user can select up to five operating modes.

In Mode 0, the conversion cycle is started by an active write ($\overline{WR}$) and the next two read ($\overline{RD}$) commands send the data out. The status of the command/data (C/$\overline{D}$) line determines whether the output data consists of the eight LSBs or four MSBs. In this mode, as well as Modes 1 and 2, the $\overline{ACK}$ line reflects the ADC's status during an active read period. $\overline{ACK}$ can then be used to extend the I/O read cycle if desired.

In Mode 1, a conversion cycle is started by an active read. This mode is well-suited to microprocessors such as the Z80* and Z8000* which have data-block transfer as part of their repertoire. $\overline{ACK}$ only reflects the ADC's status when $\overline{CS}$, $\overline{RD}$, and C/$\overline{D}$ are LOW. The first conversion after initialization is invalid.

Mode 2 puts the A/D converter under control of a DMA controller such as the Am9517A. During DMA transfer, the microprocessor is disabled, and the Am9517A provides all the signals to control the conversion process. In Mode 2, the A/D converter internally controls the output of the data bytes. The first read signal sends out the eight LSBs and simultaneously saves the four MSBs into an internal latch. The LOW-to-HIGH transition of the first read initiates another conversion cycle. A second read cycle sends out the latched MSBs at the same time the A/D converter is performing the next conversion. C/$\overline{D}$ is ignored. The first conversion after initialization is triggered by $\overline{CS}$ and should be ignored.

Mode 3 is similar to Mode 0 except that the $\overline{ACK}$ line reflects the A/D converter's true status. This difference in the decoding of the $\overline{ACK}$ line provides flexibility in the microprocessor hand-shaking. Although tying the $\overline{ACK}$ line to the microprocessor's Wait input pin might reduce throughput, by adding additional Wait states, it does guarantee full 12-bit conversion cycles.

Mode 4 is a unique and stand-alone mode, in which the internal command register is preprogrammed to operate with offset binary data output format. Mode 4 is programmed whenever $\overline{RD}$ and $\overline{WR}$ are LOW together. This situation is an illegal state with any microprocessor-based system.

*Z80 and Z800 are trademarks of Zilog, Inc.

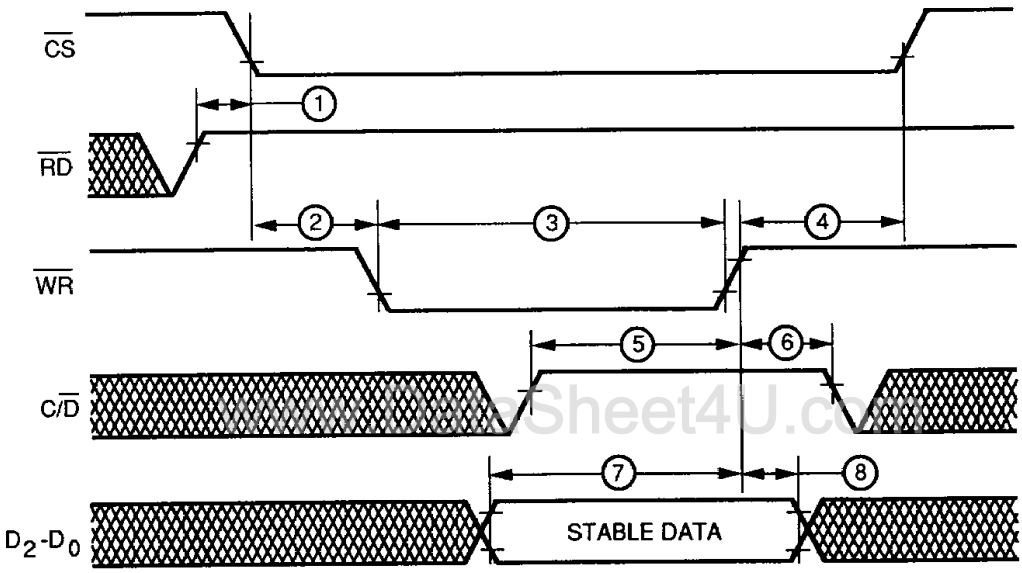
To summarize, the Am6112 has five operating modes, two possible output codes (Two's complement or offset binary) and two possible input modes (unipolar or bipolar). Four of the operating modes are microprocessor-compatible and one operating mode is stand-alone. Before using one of the microprocessor-compatible modes, the Am6112 must first be initialized to the appropriate operating mode and output code by asserting $\overline{WR}$ and bringing C/$\overline{D}$ HIGH with the appropriate data present on $D_0 - D_2$. This initialization need be done only once for any given mode and code. Conversions may be triggered by $\overline{WR}$ or by $\overline{RD}$. Modes 0 and 3 are triggered by $\overline{WR}$ and differ only in their treatment of $\overline{ACK}$. In Mode 0 $\overline{ACK}$ is gated by $\overline{RD}$. The typical application for this mode is with a microprocessor, where one command ($\overline{WR}$) will start conversion and two reads; ($\overline{RD}$) will get the digitized data. The gated $\overline{ACK}$ is used to insert Wait states on read. Modes 1 and 2 are triggered by $\overline{RD}$ and gate $\overline{ACK}$ with $\overline{RD}$, as in Mode 0. Mode 2 (DMA compatible) is the fastest throughput mode.

Stand-alone mode conversions are triggered by asserting $\overline{WR}$ and $\overline{RD}$, as shown in the Timing Diagram. $\overline{ACK}$ reflects true converter status in stand-alone mode, as it does in Mode 3.

INITIALIZATION TIMING TABLE

Number	Parameters	Description	Min.	Typ.	Max.	Unit
1	$t_{\overline{RD}-\overline{CS}}$	$\overline{RD}$ HIGH to CS LOW ($\overline{RD}$ Setup)	10			ns
2	$t_{\overline{SCS}-\overline{WR}}$	$\overline{CS}$ LOW to $\overline{WR}$ LOW ($\overline{CS}$ Setup)	10			ns
3	$t_{\overline{WR}}$	$\overline{WR}$ Pulse Width	100			ns
4	$t_{\overline{WR}-\overline{CS}}$	$\overline{WR}$ HIGH to $\overline{CS}$ LOW ($\overline{WR}$ Hold)	10			ns
5	$t_{SC/\overline{D}-\overline{WR}}$	C/$\overline{D}$ HIGH to $\overline{WR}$ HIGH (C/$\overline{D}$ Setup)	100	30		ns
6	$t_{HC/\overline{D}-\overline{WR}}$	$\overline{WR}$ HIGH to C/$\overline{D}$ HIGH (C/$\overline{D}$ Hold)	10			ns
7	$t_{SD-\overline{WR}}$	Data Setup Time	100			ns
8	$t_{HD-\overline{WR}}$	Data Hold Time	20			ns

INITIALIZATION TIMING DIAGRAM



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Am6112 COMMAND REGISTER DECODING

Command Bits				Mode Description		
D_2	D_1	D_0	Mode	Conversions Started by	$\overline{ACK}$ Output Gated with	C/$\overline{D}$ Function
0	0	0/1	0	$\overline{WR}$	$\overline{RD} \cdot \overline{CS}$	Read LOW or HIGH Byte
0	1	0/1	1	$\overline{RD}$	$\overline{RD} \cdot \overline{CS} \cdot C/\overline{D}$	Read LOW or HIGH Byte
1	0	0/1	2	$\overline{RD}$	$\overline{RD} \cdot \overline{CS}$	Ignored
1	1	0/1	3	$\overline{WR}$	$\overline{CS}$	Read LOW or HIGH Byte
X	X	X*	4	$\overline{WR}$	$\overline{CS}$	Read LOW or HIGH Byte

Notes: D_0 – 1 — Two's complement output code
D_0 = 0 — Offset binary output code
X = Don't care
*Mode 4 always uses offset binary output code.

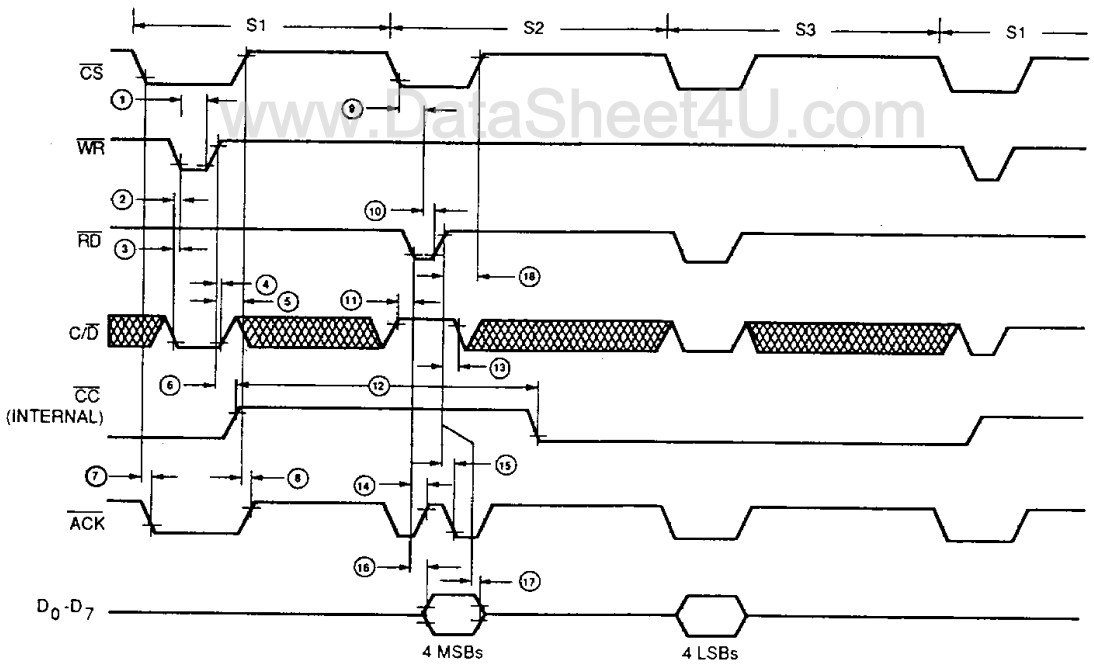
MODE 0 TIMING TABLE

Number	Parameters	Descriptions	Min.	Typ.	Max.	Unit
1	$t_{\overline{WRL}}$	$\overline{WR}$ LOW	100			ns
2	$t_{C/\overline{D}L-WL}$	C/$\overline{D}$ LOW to $\overline{WR}$ LOW Setup	10			ns
3	$t_{\overline{CS}L-WL}$	$\overline{CS}$ LOW to $\overline{WR}$ LOW Setup	20			ns
4	$t_{WH-C/\overline{D}L}$	$\overline{WR}$ HIGH to C/$\overline{D}$ LOW Hold	10			ns
5	$t_{WH-\overline{CS}H}$	$\overline{WR}$ HIGH to $\overline{CS}$ HIGH Hold	20			ns
6	$t_{WH-\overline{CC}H}$	$\overline{WR}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
7	$t_{\overline{CS}L-\overline{ACK}L}$	$\overline{CS}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
8	$t_{\overline{CS}H-\overline{ACK}H}$	$\overline{CS}$ HIGH to $\overline{ACK}$ HIGH Delay	40	75	150	ns
9	$t_{\overline{CS}L-\overline{RD}L}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW	20			ns
10	$t_{\overline{RD}L}$	$\overline{RD}$ LOW	100			ns
11	$t_{C/\overline{D}-\overline{RD}L}$	C/$\overline{D}$ to $\overline{RD}$ LOW Setup	20			ns
12	t_{CONV}	Conversion Time			12 • 5	t_{CLK}*
13	$t_{RH-C/\overline{D}}$	$\overline{RD}$ HIGH to C/$\overline{D}$ Hold	10			ns
14	$t_{\overline{RD}L-\overline{ACK}H}$	$\overline{RD}$ LOW to $\overline{ACK}$ HIGH Delay		100	200	ns
15	$t_{RH-\overline{ACK}L}$	$\overline{RD}$ HIGH to $\overline{ACK}$ LOW Delay		50	100	ns
16	$t_{\overline{RD}L-DTVLD}$	$\overline{RD}$ LOW to Data Delay		50	100	ns
17	$t_{\overline{CS}H-DTVLD}$	$\overline{RD}$ HIGH to Data Hold	20	60	75	ns
18	$t_{RH-\overline{CS}H}$	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH	20			ns

*Note: t_{CLK} = One Clock Period.

Note 1. $\overline{CC}$ is an internal line and is shown for clarity.

MODE 0 TIMING DIAGRAM



01910-008A

S_1 — Start a conversion cycle with an active $\overline{WR}$.

S_2 — Read first data byte. The four MSBs become valid six clock periods after $\overline{CC}$ goes HIGH. Therefore, the four MSBs may be read during S_2 while the conversion cycle is in progress. If conversion is done ($\overline{CC}$ going LOW) prior to S_2, then either the four MSBs or the eight LSBs may be read first and the $\overline{ACK}$ signal during S_2 and S_3 is the same as during S_1. If the conversion time is longer than S_1 + S_2, then the $\overline{ACK}$ signal can be used to extend the active part of S_2.

S_3 — Read second data byte.

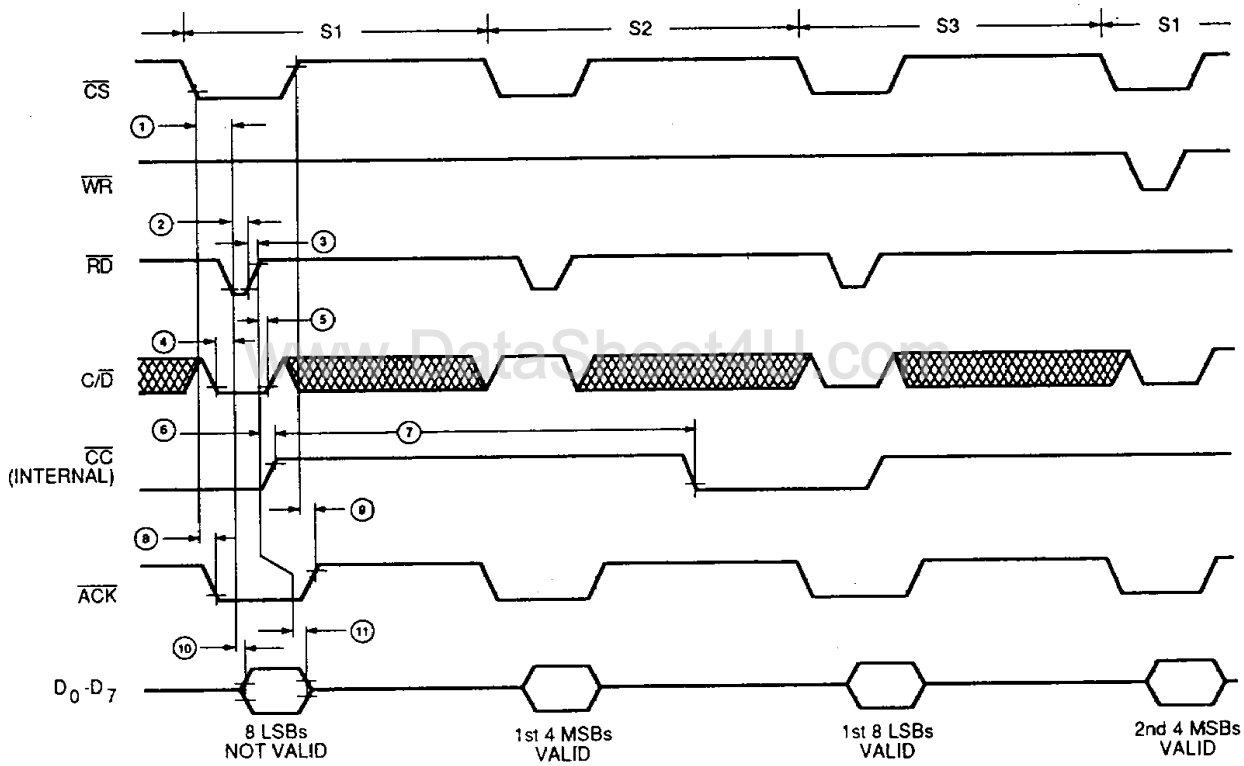
MODE 1 TIMING TABLE

Number	Parameters	Description	Min.	Typ.	Max.	Unit
1	$t_{\overline{CSL}-RL}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup	20			ns
2	$t_{\overline{RDL}}$	$\overline{RD}$ LOW	100			ns
3	$t_{RH-\overline{CSH}}$	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH	20			ns
4	$t_{C/\overline{D}-\overline{CSL}}$	C/$\overline{D}$ to $\overline{RD}$ LOW Setup	10			ns
5	$t_{RH-C/\overline{D}}$	$\overline{RD}$ HIGH to C/$\overline{D}$ Hold	10			ns
6	$t_{RH-\overline{CCH}}$	$\overline{RD}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
7	t_{CONV}	Conversion Time			12 • 5	ns
8	$t_{\overline{CSL}-\overline{ACKL}}$	$\overline{CS}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
9	$t_{\overline{CSH}-\overline{ACKH}}$	$\overline{CS}$ HIGH to $\overline{ACK}$ HIGH Delay		75	150	ns
10	$t_{RL-DTHLY}$	$\overline{RD}$ HIGH to Data Delay		50	100	ns
11	$t_{RH-DTDLY}$	$\overline{RD}$ HIGH to Data Hold	20	60	75	ns

*Note: t_{CLK} = One Clock Period.

Note 1. $\overline{CC}$ is an internal line and is shown for clarity.

MODE 1 TIMING DIAGRAM



01910-009A

S_1 — Start the first conversion cycle with an active $\overline{RD}$. The 8 LSBs read are not valid.

S_2 — Read the first four MSBs. The four MSBs become valid six clock periods after $\overline{CC}$ goes high. Therefore, the four MSBs may be read *during* S_2 while the conversion cycle is in progress. If conversion ends prior to S_2, then either the four MSBs or the 8 LSBs may be read first and the $\overline{ACK}$ signal during S_2 is the same as during S_1. If the conversion time is longer than S_2, then the $\overline{ACK}$ signal can be used to extend the active part of S_2. C/$\overline{D}$ must be LOW to give a valid $\overline{ACK}$ signal.

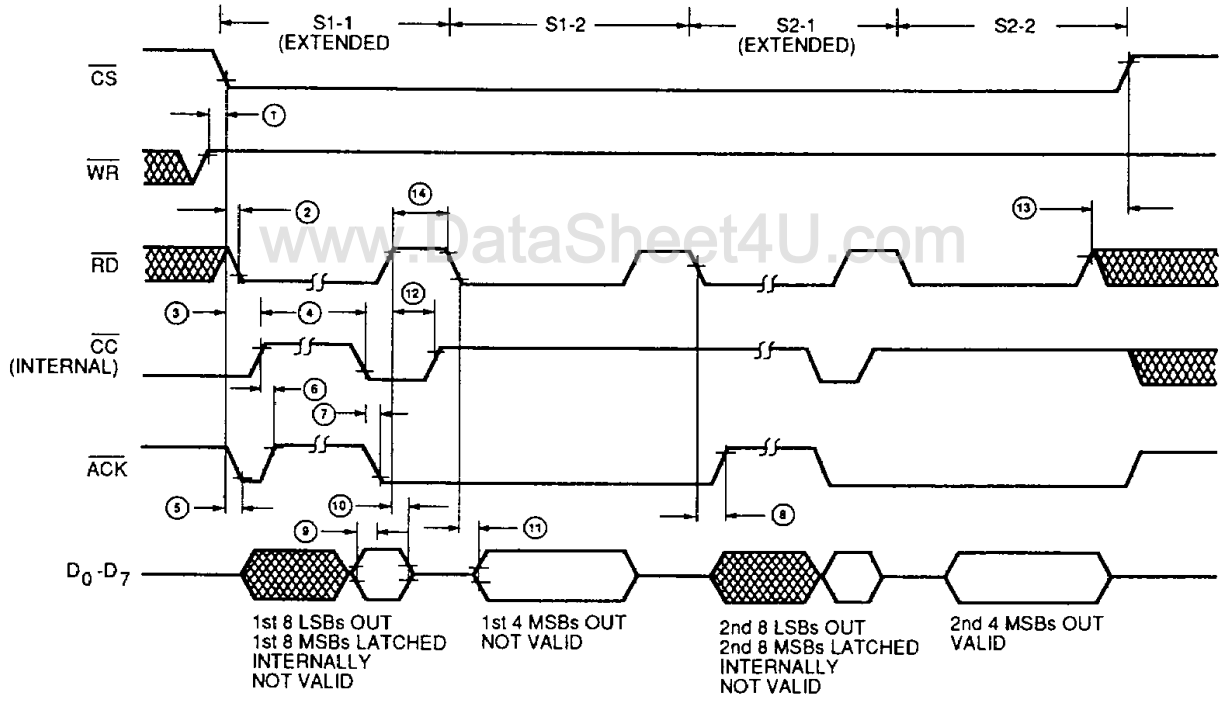
S_3 and S_1 — Read the first eight LSBs and start the next conversion cycle.

MODE 2 TIMING TABLE

Number	Parameters	Description	Min.	Typ.	Max.	Unit
1	$t_{WH-\overline{CSL}}$	$\overline{WR}$ HIGH to $\overline{CS}$ LOW Setup	10			ns
2	$t_{\overline{CSL}-\overline{RDL}}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup	10			ns
3	$t_{\overline{CSL}-\overline{CCH}}$	$\overline{CS}$ LOW to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
4	t_{CONV}	Conversion Time			12 • 5	t_{CLK}*
5	$t_{\overline{CSL}-\overline{ACKL}}$	$\overline{CS}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
6	$t_{\overline{CCH}-\overline{ACKH}}$	$\overline{CC}$ HIGH to $\overline{ACK}$ HIGH Delay (Note 1)		50	100	ns
7	$t_{\overline{CCL}-\overline{ACKL}}$	$\overline{CC}$ LOW to $\overline{ACK}$ LOW Delay (Note 1)		50	100	ns
8	$t_{RL-\overline{ACKH}}$	$\overline{RD}$ LOW to $\overline{ACK}$ HIGH Delay		100	200	ns
9	$t_{LB-\overline{ACKL}}$	Data to $\overline{ACK}$ LOW	20	50		ns
10	$t_{RH-DTHLD}$	$\overline{RD}$ HIGH to Data Hold	20	60	75	ns
11	$t_{RL-DTDLY}$	$\overline{RD}$ LOW to Data Delay		50	100	ns
12	$t_{RH-\overline{CCH}}$	$\overline{RD}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
13	$t_{RH-\overline{CSH}}$	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH	10			ns
14	t_{RH}	$\overline{RD}$ HIGH	50			ns

*Note: t_{CLK} = One Clock Period.
Note 1. $\overline{CC}$ is an internal line and is shown for clarity.

MODE 2 TIMING DIAGRAM



01910-010A

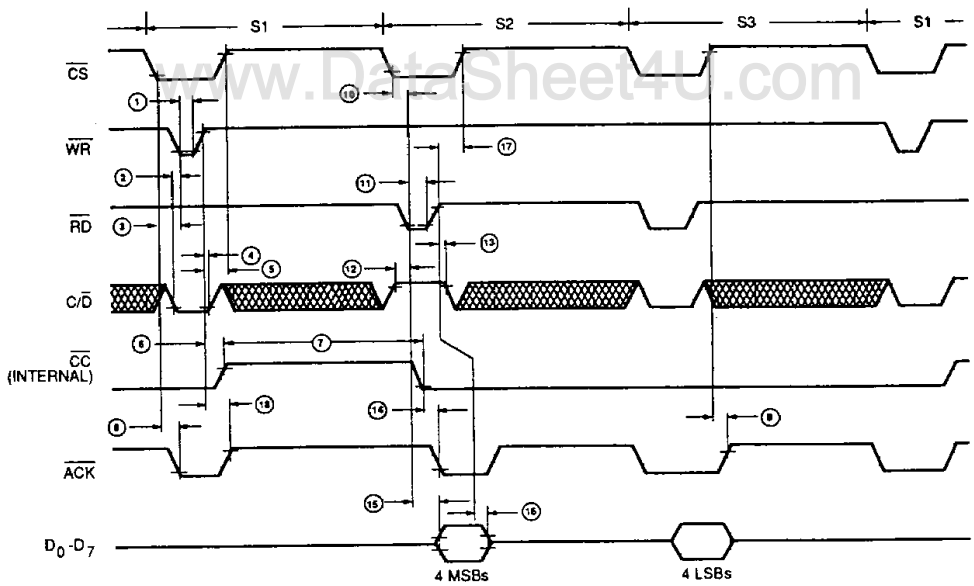
S_{1-1} — Start first conversion with $\overline{CS}$ going LOW. First four MSBs are latched internally. First eight LSBs are valid when $\overline{CC}$ goes LOW. Note that S_{1-1} cycle is extended by the insertion of wait states using the $\overline{ACK}$ signal. Second conversion starts after $\overline{RD}$ goes HIGH. Data is invalid.
S_{1-2} — Read first four MSBs. Note that this cycle is not extended. Data is invalid.
S_{2-1} — This cycle is similar to the S_{1-1} cycle.
S_{2-2} — This cycle is similar to the S_{1-2} cycle except that conversion cycles are inhibited after $\overline{CS}$ goes HIGH.

MODE 3 TIMING TABLE

Number	Parameters	Description	Min.	Typ.	Max.	Unit
1	$t_{\overline{WR}L}$	$\overline{WR}$ LOW	100			ns
2	$t_{C/\overline{D}-\overline{WL}}$	C/$\overline{D}$ LOW to $\overline{WR}$ LOW Setup	10			ns
3	$t_{\overline{CS}L-\overline{WL}}$	$\overline{CS}$ LOW to $\overline{WR}$ LOW Setup	20			ns
4	$t_{WH-C/\overline{D}L}$	$\overline{WR}$ HIGH to C/$\overline{D}$ LOW Hold	10			ns
5	$t_{WH-\overline{CS}H}$	$\overline{WR}$ HIGH to $\overline{CS}$ HIGH Setup	20			ns
6	$t_{WH-\overline{CC}H}$	$\overline{WR}$ HIGH to $\overline{CC}$ HIGH Delay (Note 1)			t_{CLK} + 50*	ns
7	t_{CONV}	Conversion Time			12 • 5	t_{CLK}*
8	$t_{\overline{CS}L-\overline{ACK}L}$	$\overline{CS}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns
9	$t_{\overline{CS}H-\overline{ACK}H}$	$\overline{CS}$ HIGH to $\overline{ACK}$ HIGH Delay	40	75	150	ns
10	$t_{\overline{CS}L-RL}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup	20			ns
11	$t_{\overline{RD}L}$	$\overline{RD}$ LOW	100			ns
12	$t_{C/\overline{D}H-RL}$	C/$\overline{D}$ HIGH to $\overline{RD}$ LOW Setup	10			ns
13	$t_{RH-C/\overline{D}H}$	$\overline{RD}$ HIGH to C/$\overline{D}$ HIGH Hold	10			ns
14	$t_{\overline{CC}L-\overline{ACK}L}$	$\overline{CC}$ LOW to $\overline{ACK}$ LOW Delay (Note 1)		50	100	ns
15	$t_{RL-DTDLY}$	$\overline{RD}$ LOW to Data Delay		50	100	ns
16	$t_{\overline{CS}H-DTHLD}$	$\overline{RD}$ HIGH to Data Hold	20	60	75	ns
17	$t_{RH-\overline{CS}H}$	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH	10			ns
18	$t_{WH-\overline{ACK}H}$	$\overline{WR}$ HIGH to $\overline{ACK}$ HIGH Delay	t_{CLK} + 40	t_{CLK} + 75	t_{CLK} + 150	ns

*Note: t_{CLK} = One Clock Period.
Note 1. $\overline{CC}$ is an internal line and is shown for clarity.

MODE 3 TIMING DIAGRAM



01910-011A

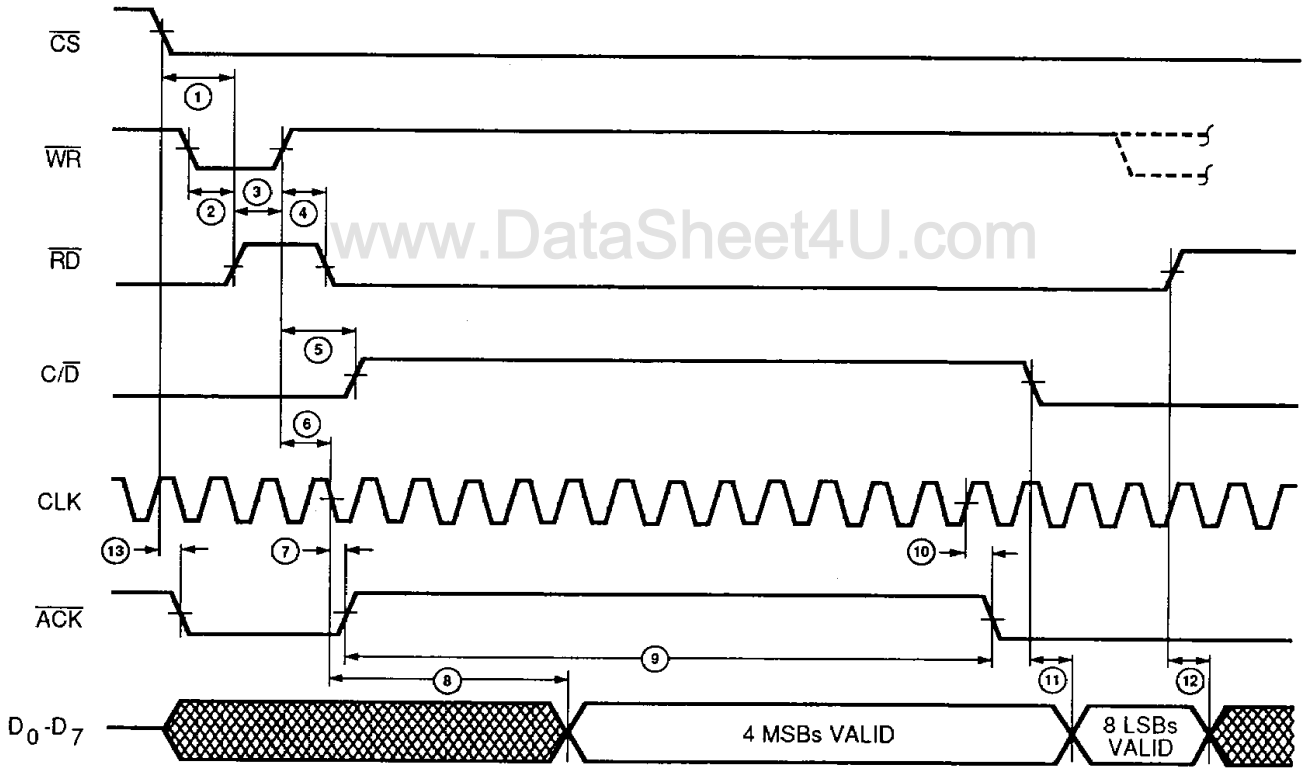
S_1 — Start a conversion cycle with an active $\overline{WR}$.
S_2 — Read first data byte. The four MSBs become valid six clock periods after $\overline{CC}$ goes HIGH. Therefore, the four MSBs may be read during S_2 while conversion cycle is in progress. If conversion is done ($\overline{CC}$ has gone LOW) prior to S_2, then either the four MSBs or the eight LSBs may be read first and the $\overline{ACK}$ signal during S_2 and S_3 is the same as during S_1. If conversion ends during active part of S_2 ($\overline{CS}$ LOW) $\overline{ACK}$ output is as shown above. If the conversion time is longer than S_1 + S_2, then the $\overline{ACK}$ output can be used to extend the active part of S_2.
S_3 — Read second data byte.

Am6112 STAND-ALONE MODE TIMING

Number	Parameters	Description	Min.	Typ.	Max.	Unit
1	$t_{\overline{CSL}-RL}$	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup	100			ns
2	t_{WL-RL}	$\overline{WR}$ LOW to $\overline{RD}$ LOW Setup	100			ns
3	t_{RH-WH}	$\overline{RD}$ HIGH to $\overline{WR}$ HIGH Setup	10			ns
4	t_{WH-RH}	$\overline{WR}$ HIGH to $\overline{RD}$ HIGH Hold	20			ns
5	$t_{\overline{WH}-C/\overline{D}L}$	$\overline{WR}$ HIGH to C/$\overline{D}$ LOW Hold	10		1 t_{CLK}*	ns
6	$t_{WH-CLKL}$	$\overline{WR}$ HIGH to $\overline{CLK}$ LOW Setup	50			ns
7	$t_{CLK-\overline{ACK}H}$	CLK LOW to $\overline{ACK}$ HIGH Delay		100	200	ns
8	$t_{CLKL-UBVLD}$	CLK LOW to Upper Byte Valid		4.5 t_{CLK}* + 130	4.5 t_{CLK}* + 200	ns
9	t_{CONV}	Conversion Time			12 • 5	t_{CLK}*
10	$t_{CLK-\overline{ACK}L}$	CLK HIGH to $\overline{ACK}$ LOW		50	100	ns
11	$t_{C/\overline{D}L-LBVLD}$	C/$\overline{D}$ LOW to Lower Byte Valid		50	150	ns
12	$t_{RH-DTHLD}$	$\overline{RD}$ HIGH to Data Hold	20			ns
13	$t_{\overline{CSL}-\overline{ACK}L}$	$\overline{CS}$ LOW to $\overline{ACK}$ LOW Delay		50	100	ns

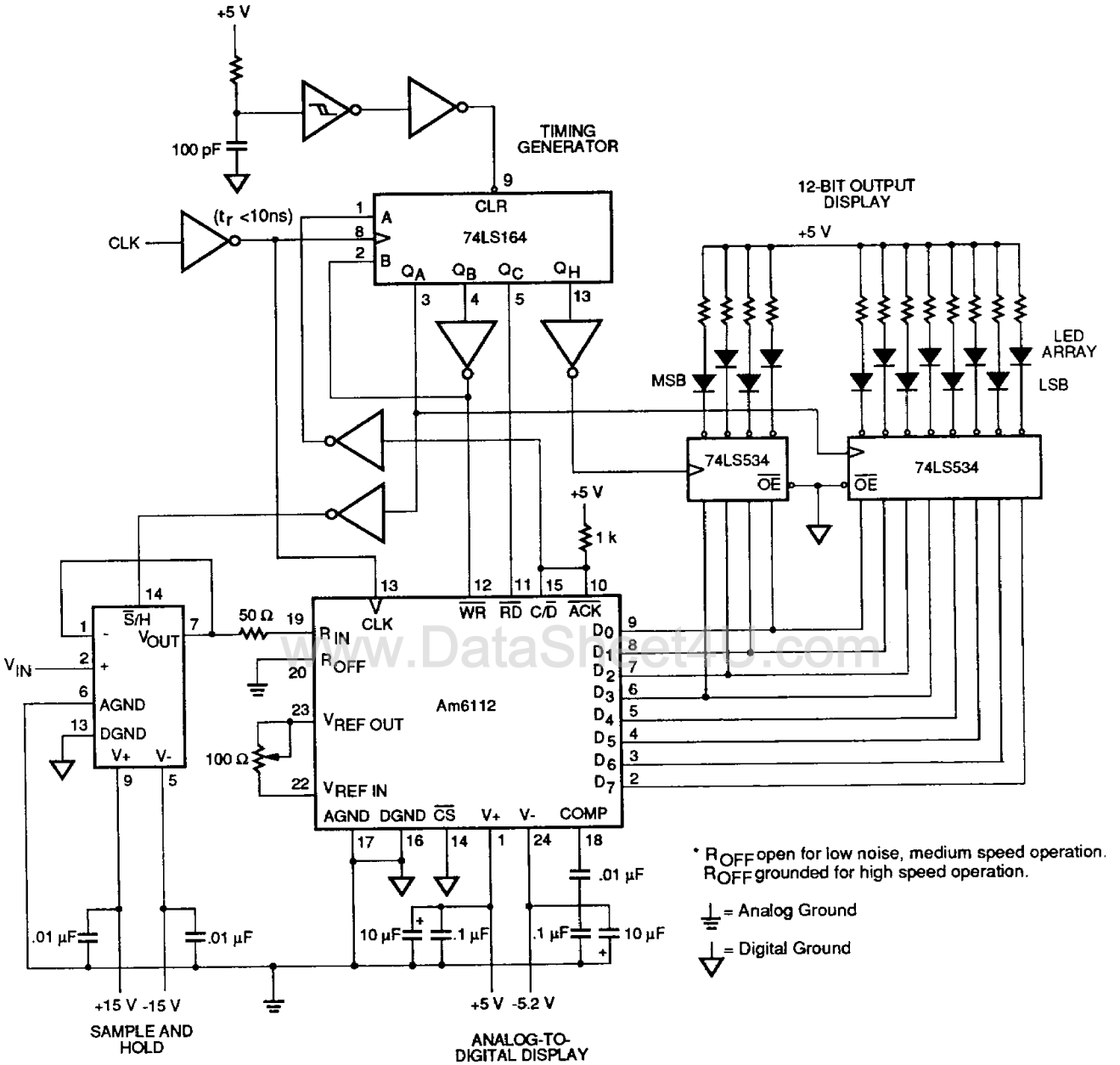
*Note: t_{CLK} = One Clock Period.

STAND-ALONE TIMING DIAGRAM



01910-012A

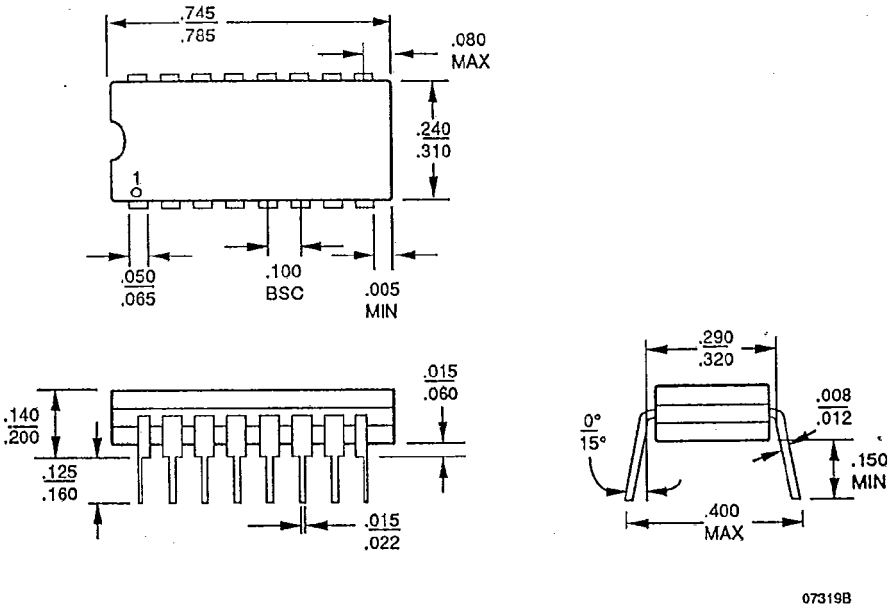
AM6112 STAND-ALONE APPLICATION CIRCUIT
UNIPOLAR MODE



01910-013A

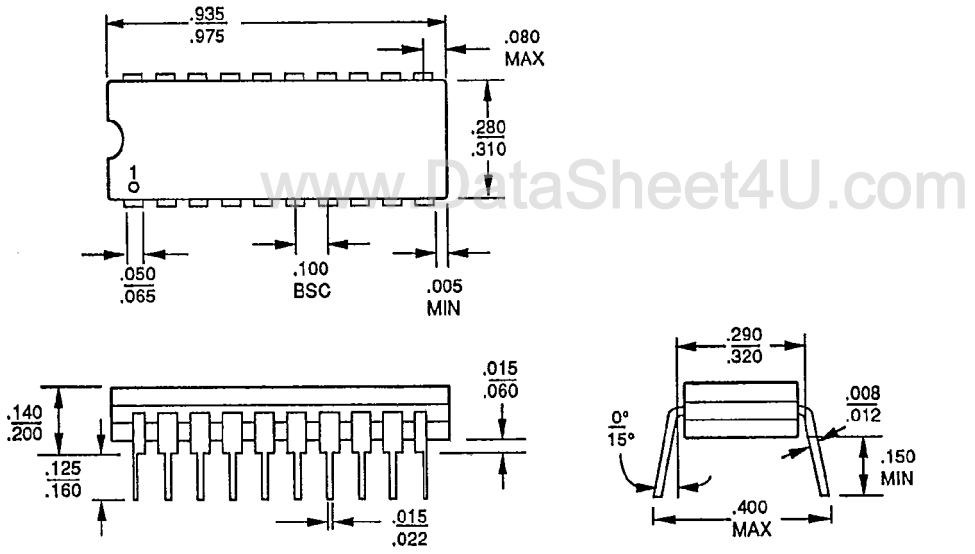
T-90-20

PHYSICAL DIMENSIONS
CD 016



07319B

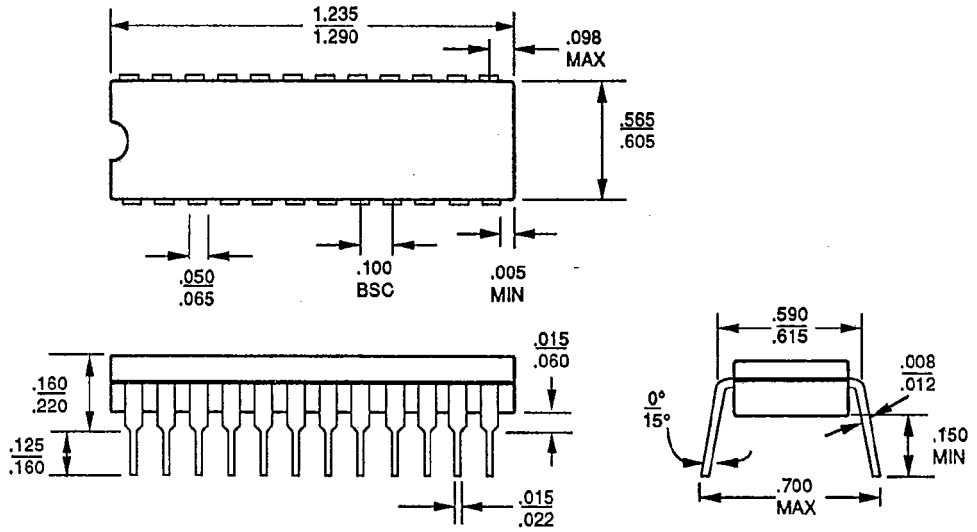
CD 020



03941-004C

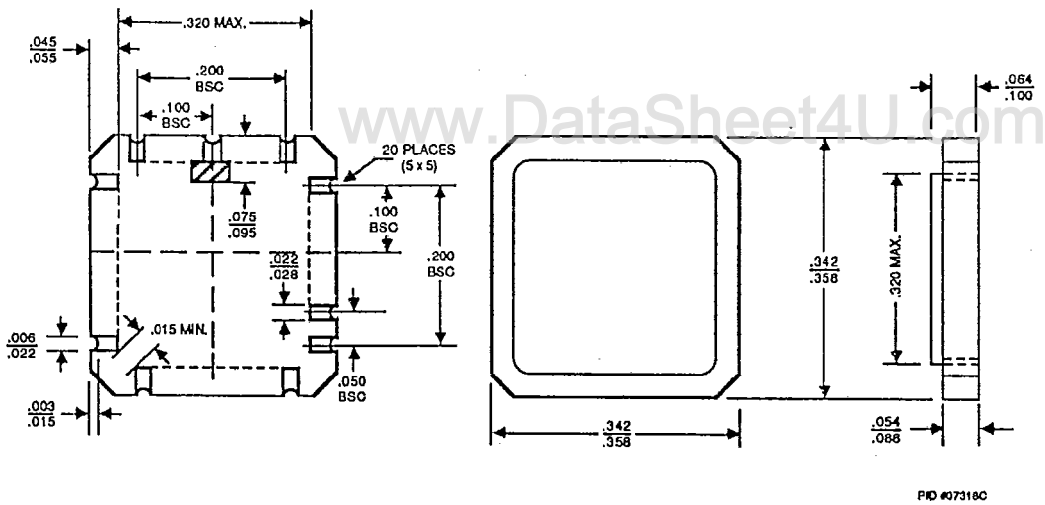
T-90-20

PHYSICAL DIMENSIONS (continued)
CD 024



03067-008A

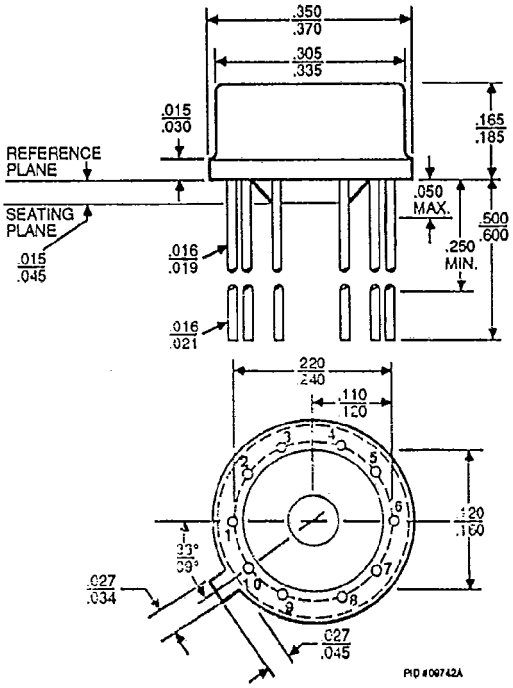
CL 020



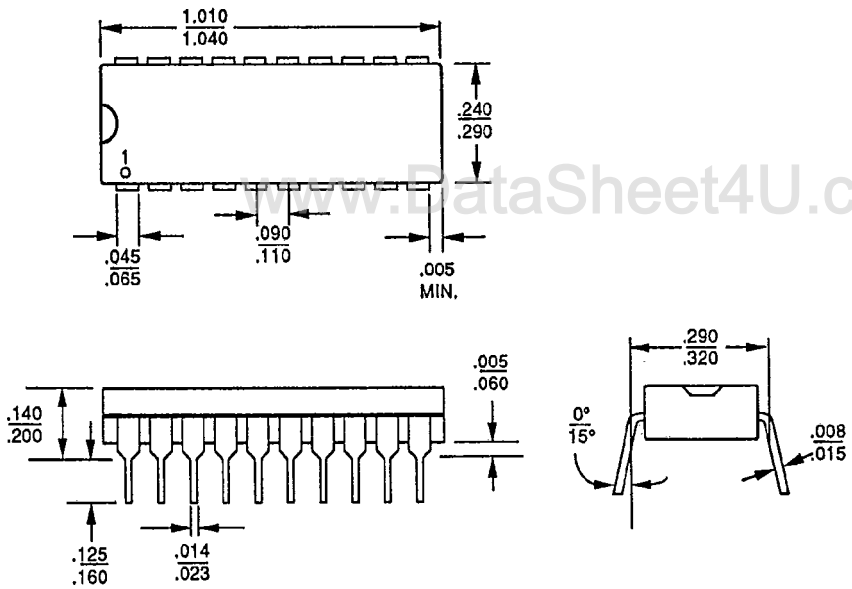
PID #07318C

PHYSICAL DIMENSIONS (continued)

MC 010



PD 020



03941-005C