TEXAS INSTRUMENTS
AM6442, AM6441, AM6422, AM6421, AM6412, AM6411
SPRSP56F – JANUARY 2021 – REVISED OCTOBER 2023

AM64x Sitara™ Processors

1 Features

Processor cores:

- 1× Dual 64-bit Arm® Cortex®-A53 microprocessor subsystem at up to 1.0 GHz
  - Dual-core Cortex-A53 cluster with 256KB L2 shared cache with SECDED ECC
  - Each A53 Core has 32KB L1 DCache with SECDED ECC and 32KB L1 ICache with Parity protection
- Up to 2× Dual-core Arm® Cortex®-R5F MCU subsystems at up to 800 MHz, integrated for real-time processing
  - Dual-core Arm® Cortex®-R5F supports dual-core and single-core modes
  - 32KB ICache, 32KB DCache and 64KB TCM per each R5F core for a total of 256KB TCM with SECDED ECC on all memories
- 1× Single-core Arm® Cortex®-M4F MCU at up to 400 MHz
  - 256KB SRAM with SECDED ECC

Industrial subsystem:

- 2× gigabit Industrial Communication Subsystems (PRU_ICSSG)
  - Supports Profinet IRT, Profinet RT, EtherNet/IP, EtherCAT, Time-Sensitive Networking (TSN), and more
  - Backward compatibility with 10/100Mb PRU_ICSS
  - Each PRU_ICSSG contains:
    - 2× Ethernet ports
      - MII (10/100)
      - RGMII (10/100/1000)
    - 6 PRU RISC cores per PRU_ICSSG each core having:
      - Instruction RAM with ECC
      - Broadside RAM
      - Multiplier with optional accumulator (MAC)
      - CRC16/32 hardware accelerator
      - Byte swap for Big/Little Endian conversion
      - SUM32 hardware accelerator for UDP checksum
      - Task Manager for preemption support
    - Three Data RAMs with ECC
    - 8 banks of 30 × 32-bit register scratchpad memory
    - Interrupt controller and task manager
    - Two 64-bit Industrial Ethernet Peripherals (IEPs) for time stamping and other time synchronization functions
    - 18× Sigma-Delta filters
      - Short circuit logic
      - Over-current logic
    - 6× Multi-protocol position encoder interfaces
    - One Enhanced Capture Module (ECAP)
    - 16550-compatible UART with a dedicated 192-MHz clock to support 12-Mbps PROFIBUS

Memory subsystem:

- Up to 2MB of On-chip RAM (OCSRAM) with SECDED ECC:
  - Can be divided into smaller banks in increments of 256KB for as many as 8 separate memory banks
  - Each memory bank can be allocated to a single core to facilitate software task partitioning
- DDR Subsystem (DDRSS)
  - Supports LPDDR4, DDR4 memory types
  - 16-Bit data bus with inline ECC
  - Supports speeds up to 1600 MT/s
- 1× General-Purpose Memory Controller (GPMC)
  - 16-Bit parallel bus with 133 MHz clock or
  - 32-Bit parallel bus with 100 MHz clock
  - Error Location Module (ELM) support

System on Chip (SoC) Services:

- Device Management Security Controller (DMSC-L)
  - Centralized SoC system controller
  - Manages system services including initial boot, security, and clock/reset/power management
  - Communication with various processing units over message manager
  - Simplified interface for optimizing unused peripherals
- Data Movement Subsystem (DMSS)
  - Block Copy DMA (BCDMA)
  - Packet DMA (PKTDMA)
  - Secure Proxy (SEC_PROXY)
  - Ring Accelerator (RINGACC)

Security:

- Secure boot supported
  - Hardware-enforced Root-of-Trust (RoT)
  - Support to switch RoT via backup key
  - Support for takeover protection, IP protection, and anti-roll back protection

- Trusted Execution Environment (TEE) supported
  - Arm TrustZone® based TEE
  - Secure watchdog/timer/IPC
  - Extensive firewall support for isolation
  - Secure storage support
  - Replay Protected Memory Block (RPMB) support
- Security co-processor (DMSC-L) for key and security management, with dedicated device level interconnect for security
- Cryptographic acceleration supported
  - Session-aware cryptographic engine with ability to auto-switch key-material based on incoming data stream
    - Supports cryptographic cores
  - AES – 128-/192-/256-Bit key sizes
  - SHA2 – 224-/256-/384-/512-Bit key sizes
  - DRBG with true random number generator
  - PKA (Public Key Accelerator) to Assist in RSA/ECC processing for secure boot
- Debugging security
  - Secure software controlled debug access
  - Security aware debugging

High-speed interfaces:

- 1× Integrated Ethernet switch (CPSW3G) supporting:
  - Up to 2 Ethernet ports
    - RMII (10/100)
    - RGMII (10/100/1000)
  - IEEE 1588 (2008 Annex D, Annex E, Annex F) with 802.1AS PTP
  - Clause 45 MDIO PHY management
  - Energy efficient Ethernet (802.3az)
- 1× PCI-Express® Gen2 controller (PCIE)
  - Supports Gen2 operation
  - Supports Single Lane operation
- 1× USB 3.1 Dual-Role Device (DRD) Subsystem (USBSS)
  - Port configurable as USB host,
    USB device, or
    USB Dual-Role device
  - USB device: High-speed (480 Mbps), and Full-speed (12Mbps)
  - USB host: SuperSpeed Gen 1 (5 Gbps),
    High-speed (480 Mbps),
    Full-speed (12 Mbps), and
    Low-speed (1.5 Mbps)

General connectivity:

- 6× Inter-Integrated Circuit (I2C) ports
- 9× configurable Universal Asynchronous Receive/Transmit (UART) modules
- 1× Flash Subsystem (FSS) that can be configured as Octal SPI (OSPI) flash interfaces or one Quad SPI (QSPI)
- 1× 12-Bit Analog-to-Digital Converters (ADC)
  - Up to 4 MSPS
  - 8× multiplexed analog inputs
- 7× Multichannel Serial Peripheral Interfaces (MCSPI) controllers
- 6× Fast Serial Interface Receiver (FSI_RX) cores
- 2× Fast Serial Interface Transmitter (FSI_TX) cores
- 3× General-Purpose I/O (GPIO) modules

Control interfaces:

- 9x Enhanced Pulse-Width Modulator (EPWM) modules
- 3× Enhanced Capture (ECAP) modules
- 3× Enhanced Quadrature Encoder Pulse (EQEP) modules
- 2× Modular Controller Area Network (MCAN) modules with or without full CAN-FD support

Media and data storage:

- 2× Multi-Media Card/Secure Digital (MMC/SD/SDIO) interfaces
  - One 4-bit for SD/SDIO;
  - One 8-bit for eMMC
  - Integrated analog switch for voltage switching between 3.3V to 1.8V for high-speed cards

Power management:

- Simplified power sequence
- Integrated SDIO LDO for handling automatic voltage transition for SD interface
- Integrated voltage supervisor for safety monitoring of over-under voltage conditions
- Integrated power supply glitch detector for detecting fast supply transients

Functional Safety:

- Functional Safety-Compliant targeted
  - Developed for functional safety applications
  - Documentation will be available to aid IEC 61508 functional safety system design
  - Systematic capability up to SIL 3 targeted
  - Hardware integrity up to SIL 2 targeted
  - Safety-related certification
    - IEC 61508 certification planned
- Functional Safety Features
  - ECC or parity on calculation-critical memories
  - ECC and parity on select internal bus interconnect
  - Built-In Self-Test (BIST) for CPU and on-chip RAM
  - Error Signaling Module (ESM) with error pin
  - Runtime safety diagnostics, voltage, temperature, and clock monitoring, windowed watchdog timers, CRC engine for memory integrity checks
  - Dedicated MCU domain memory, interfaces, and M4F core capable of being isolated from the larger SoC with Freedom From Interference (FFI) features
    - Separate interconnect
    - Firewalls and timeout gaskets
    - Dedicated PLL
    - Dedicated I/O supply
    - Separate reset

SoC architecture:

- Supports primary boot from UART, I2C, OSPI/QSPI Flash, SPI Flash, parallel NOR Flash, parallel NAND Flash, SD, eMMC, USB, PCIe, and Ethernet interfaces
- 16-nm FinFET technology
- 17.2 mm × 17.2 mm, 0.8-mm pitch, 441-pin BGA package

2 Applications

- Programmable Logic Controller (PLC)
- Motor Drives
- Remote I/O
- Industrial Robots
- Condition-Monitoring Gateway

3 Description

AM64x is an extension of the Sitara™ Industrial-grade family of heterogeneous Arm® processors. AM64x is built for industrial applications, such as motor drives and Programmable Logic Controllers (PLCs), which require a unique combination of real-time processing and communications with applications processing. AM64x combines two instances of the Sitara device's gigabit TSN-enabled PRU-ICSSG with up to two Arm® Cortex®-A53 cores, up to four Cortex-R5F MCUs, and a Cortex-M4F MCU.

AM64x is architected to provide real-time performance through the high-performance R5Fs, Tightly-Coupled Memory banks, configurable SRAM partitioning, and dedicated low-latency paths to and from peripherals for rapid data movement in and out of the SoC. This deterministic architecture allows for AM64x to handle the tight control loops found in servo drives while the peripherals like FSI, GPMC, PWMs, sigma delta decimation filters, and absolute encoder interfaces help enable a number of different architectures found in these systems.

The Cortex-A53s provide the powerful computing elements necessary for Linux applications. Linux, and Real-time (RT) Linux, is provided through TI's Processor SDK Linux which stays updated to the latest Long Term Support (LTS) Linux kernel, bootloader and Yocto file system on an annual basis. AM64x helps bridge the Linux world with the real-time world by enabling isolation between Linux applications and real-time streams through configurable memory partitioning. The Cortex-A53s can be assigned to work strictly out of DDR for Linux, and the internal SRAM can be broken up into various sizes for the Cortex-R5Fs to use together or independently.

The AM64x provides flexible industrial communications capability including full protocol stacks for EtherCAT SubDevice, PROFINET device, EtherNet/IP adapter, and IO-Link Master. The PRU-ICSSG further provides capability for gigabit and TSN based protocols. In addition, the PRU-ICSSG also enables additional interfaces in the SoC including sigma delta decimation filters and absolute encoder interfaces.

Functional safety features can be enabled through the integrated Cortex-M4F along with dedicated peripherals which can all be isolated from the rest of the SoC. AM64x also supports secure boot.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AM6442	ALV (FCBGA, 441)	17.2 mm × 17.2 mm
AM6441	ALV (FCBGA, 441)	17.2 mm × 17.2 mm
AM6422	ALV (FCBGA, 441)	17.2 mm × 17.2 mm
AM6421	ALV (FCBGA, 441)	17.2 mm × 17.2 mm
AM6412	ALV (FCBGA, 441)	17.2 mm × 17.2 mm
AM6411	ALV (FCBGA, 441)	17.2 mm × 17.2 mm

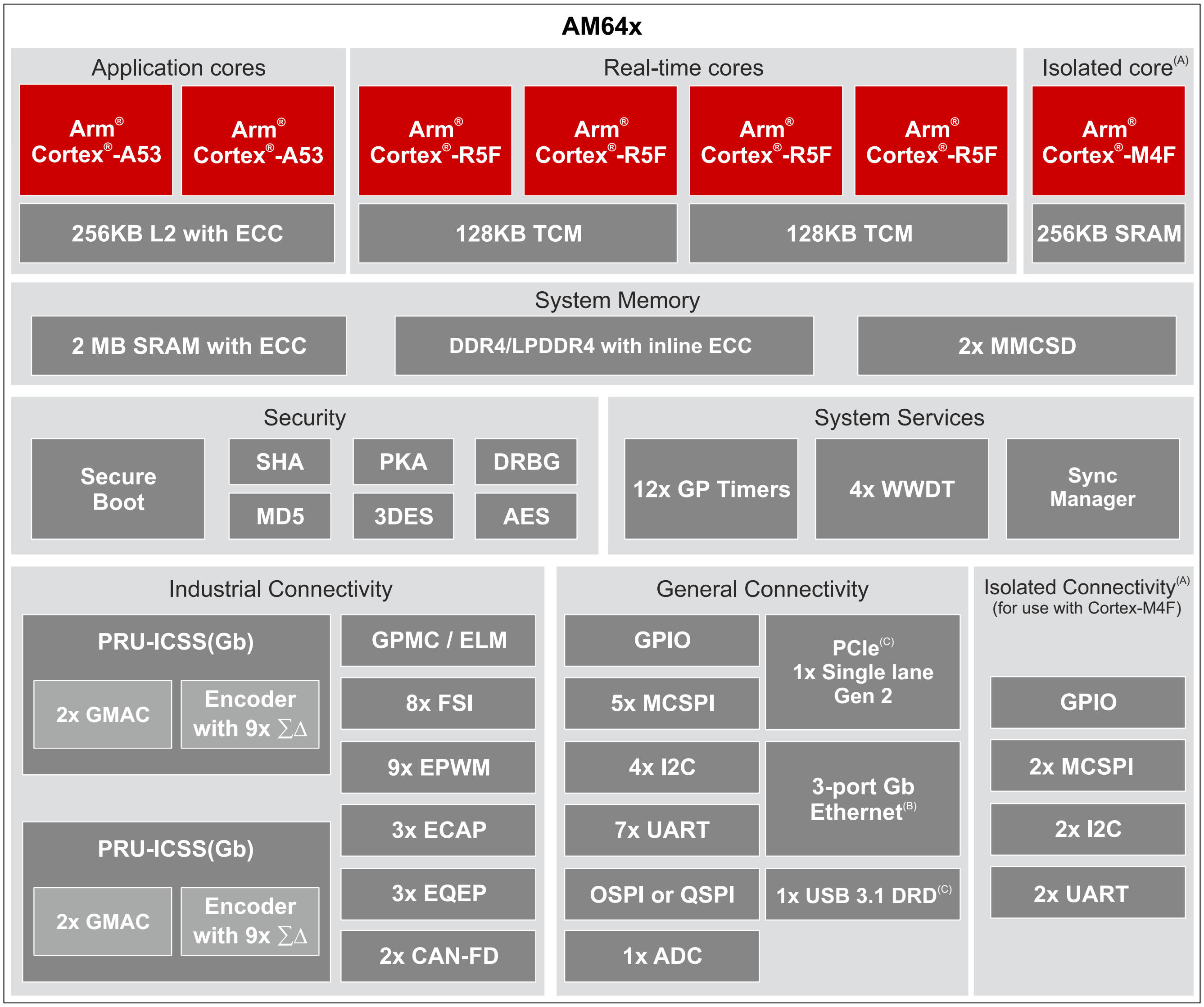
(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

3.1 Functional Block Diagram

Figure 3-1 is functional block diagram for the device.

Note

To understand what device features are currently supported by TI Software Development Kits (SDKs), search for the *AM64x Software Build Sheet* located in the Downloads tab option provided at Processor-SDK-AM64x.



A. Isolation of peripherals and M4F core is an optional feature.
B. One port is internally connected only; not connected to any pins.
C. USB SuperSpeed and PCIe share a common SerDes PHY. Therefore, USB will be limited to non-SuperSpeed modes when using the SerDes PHY for PCIe.

Figure 3-1. Functional Block Diagram

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4 Revision History

Changes from September 22, 2022 to October 31, 2023 (from Revision E (SEPTEMBER 2022) to Revision F (OCTOBER 2023)) Page

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- (Package Information): Updated the table to match the new content standard 4
- (Functional Block Diagram): Updated URL for Software Build Sheet 5
- (Device Comparison): Updated URL for Software Build Sheet 10
- (Device Comparison): Corrected the name of the JTAG User ID register 10
- (Device Comparison): Defined the R5F cores enabled in each device and changed the R5F TCM memory size from "256KB" to "4 x 64KB" in the 2 x Dual Core devices, and "2 x 128KB" in the 2 x Single Core devices 10
- (Device Comparison): Added Functional Safety Optional for AM6422 10
- (Device Comparison): Changed General-Purpose Memory Controller (GPMC) address range from 1GB to 128MB 10
- (GPMC0 Signal Descriptions): Moved the GPMC0_FCLK_MUX signal from System Signal Descriptions to GPMC0 Signal Descriptions 59
- (System Signal Descriptions): Moved the GPMC0_FCLK_MUX signal from System Signal Descriptions to GPMC0 Signal Descriptions 59
- (Pin Connectivity Requirements): Updated the second paragraph of the note following the Connectivity Requirements table. The update clarifies the operation of configurable device IOs and includes precautions that must be taken to prevent floating signals from damaging device input buffers 94
- (Specifications): Remove note that says specifications are preliminary 99
- (Power-On Hours): Updated the table to match the new content standard 101
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- (I2C OD FS Electrical Characteristics): Changed the I_{OL} minimum value from 20 to 10 for both 1.8 V and 3.3 V modes 104
- (DDR Electrical Characteristics): Added references to the respective JEDEC standards 109
- (System Timing): Removed the Timing Conditions table from this section and added separate Timing Conditions tables to each of the Reset Timing, Safety Signal Timing, and Clock Timing sections 118
- (Reset Timing): Added Timing Conditions table to define conditions specific to reset inputs and outputs 118
- (MCU_RESETSTATz, and RESETSTATz Switching Characteristics): Changed the minimum value of parameter RST8 from "4040*S" to "966*S" and the minimum value of parameter RST9 from "301200" to "4040*S" 118
- (MCU_RESETSTATz, and RESETSTATz Switching Characteristics): Changed the minimum value of parameter RST13 from "0" to "960" 118
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- (Safety Signal Timing): Added Timing Conditions table to define conditions specific to MCU_SAFETY_ERRORn output 123
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- (OSPI0 Switching Characteristics – PHY DDR Mode): Updated Note 1 and Note 4, where "in ns" was added to the OSPI_CLK cycle time reference in Note 1 and "refclk" was changed to "reference clock" in Note 4 so it matches the clock name used in the TRM.......... 203

- (OSPI0 Timing Requirements – Tap SDR Mode): Updated the constant values associated with the minimum setup and minimum hold formulas in parameters O19 and O20. Note 2 was also updated to change "refclk" to "reference clock" so it matches the clock name used in the TRM..205
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- (OSPI0 Timing Requirements – Tap DDR Mode): Updated the constant values associated with the minimum setup and minimum hold formulas in parameters O13 and O14. Note 2 was also updated to change "refclk" to "reference clock" so it matches the clock name used in the TRM..207
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5 Device Comparison

Table 5-1 shows a comparison between devices, highlighting the differences.

Note

Availability of features listed in this table are a function of shared IO pins, where IO signals associated with many of the features are multiplexed to a limited number of pins. The SysConfig tool should be used to assign signal functions to pins. This will provide a better understanding of limitations associated with pin multiplexing.

Note

To understand what device features are currently supported by TI Software Development Kits (SDKs), search for the *AM64x Software Build Sheet* located in the Downloads tab option provided at Processor-SDK-AM64x.

Table 5-1. Device Comparison

FEATURES	REFERENCE NAME	AM6442	AM6441	AM6422	AM6421	AM6412	AM6411
CTRL_MMR_CFG0_JTAG_USER_ID[31:13](1) Register bit values by device "Features" code (See Nomenclature Description table for more information on device features)							
	C:	–	–	–	–	0x19403	0x19203
	D:	0x19464	0x19264	0x19424	0x19224	–	–
	E:	0x19465	0x19265	–	0x19225	–	–
	F:	0x19466	0x19266	–	0x19226	–	–
PROCESSORS AND ACCELERATORS							
Speed Grades (See Table 7-1)		S				S, K	
Arm Cortex-A53 Microprocessor Subsystem	Arm A53	Dual Core	Single Core	Dual Core	Single Core	Dual Core	Single Core
Arm Cortex-R5F	Arm R5F	2 × Dual Core R5FSS0_CORE0 R5FSS0_CORE1 R5FSS1_CORE0 R5FSS1_CORE1		2 × Single Core R5FSS0_CORE0 R5FSS1_CORE0		Single Core R5FSS0_CORE0	
Arm Cortex-M4F	Arm M4F	Single Core Functional Safety Optional(4)				Single Core	
Device Management Security Controller	DMSC-L	Yes					
Crypto Accelerators	Security	Yes					
PROGRAM AND DATA STORAGE							
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	2MB					
R5F Tightly Coupled Memory (TCM)	TCM	4 x 64KB		2 x 128KB		1 x 128KB	
On-Chip Shared Memory (RAM) in M4F Domain	MCU_MSRAM	256KB					
DDR4/LPDDR4 DDR Subsystem	DDRSS	Up to 2GB (16-bit data) with inline ECC					
General-Purpose Memory Controller	GPMC	Up to 128MB with ECC					
PERIPHERALS							
Modular Controller Area Network Interface	MCAN	2					
Full CAN-FD Support(2)	MCAN	Optional	Optional	No	Optional	No	No
General-Purpose I/O	GPIO	Up to 198					
Inter-Integrated Circuit Interface	I2C	6					
Analog-to-Digital Converter	ADC	1				No	
Multichannel Serial Peripheral Interface	MCSPI	7					
Multi-Media Card/ Secure Digital Interface	MMCSD0	eMMC (8-bits)					
	MMCSD1	SD/SDIO (4-bits)					
Fast Serial Interface	FSI_TX	2					
	FSI_RX	6					
Flash Subsystem (FSS)(3)	OSPI0/QSPI0	Yes					

Table 5-1. Device Comparison (continued)

FEATURES	REFERENCE NAME	AM6442	AM6441	AM6422	AM6421	AM6412	AM6411
PCI Express Port with Integrated SerDes PHY	PCIE0	Single Lane[7]					
Programmable Real-Time Unit Subsystem[5]	PRU_ICSSG	2					
PRU_ICSSG Industrial Communication Support[6]	PRU_ICSSG	Optional	Optional	Yes	Optional	No	No
Gigabit Ethernet Interface	CPSW3G	Yes					
General-Purpose Timers	TIMER	16 (4 in MCU Channel)					
Enhanced Pulse-Width Modulator Module	EPWM	9					
Enhanced Capture Module	ECAP	3					
Enhanced Quadrature Encoder Pulse Module	EQEP	3					
Universal Asynchronous Receiver and Transmitter	UART	9					
Universal Serial Bus (USB3.1 Gen1) SuperSpeed Dual-Role-Device (DRD) Ports with SS SerDes PHY and USB 2.0 PHY	USB0	Yes[7]					

(1) For more details about the CTRL_MMR_CFG0_JTAG_USER_ID register and DEVICE_ID bit field, see the device TRM.
(2) Full CAN-FD Support is available when selecting an orderable part number that includes a feature code of E or F. Refer to Nomenclature Description table for the definition of feature codes.
(3) One flash interface, configured as OSPI0 or QSPI0.
(4) Functional Safety is available when selecting an orderable part number that includes a feature code of F. Refer to Nomenclature Description table for the definition of feature codes.
(5) Orderable part numbers with a feature code of C support using PRU_ICSSG for use cases other than industrial communication. Refer to Nomenclature Description table for the definition of feature codes.
(6) PRU_ICSSG industrial communication includes Ethernet networking (MII/RGMII, MDIO), Sigma-Delta (SD) decimation, and three channel peripheral interface (EnDat 2.2 and BiSS). PRU_ICSSG industrial communication support is available when selecting an orderable part number that includes a feature code of D, E, or F. Refer to Nomenclature Description table for the definition of feature codes.
(7) USB SuperSpeed and PCIe share a common SerDes PHY. Therefore, USB will be limited to non-SuperSpeed modes when using the SerDes PHY for PCIe.

5.1 Related Products

Sitara™ processors Broad family of scalable processors based on Arm® Cortex®-A cores with flexible accelerators, peripherals, connectivity and unified software support – perfect for sensors to servers. Sitara processors have the reliability needed for use in industrial applications.

AM64x Sitara™ processors AM6x processors enable gigabit industrial Ethernet networks, robust operation with extensive ECC on memories, and enhanced security features. Additional features such as an integrated lockstep MCU subsystem and diagnostic libraries help enable functional safety systems.

Sitara™ processors - Applications Sitara™ processors provide scalable solutions for a wide range of applications from HMIs and gateways to more complex equipment such as drives and substation automation equipment. Sitara processors also offer multi-protocol support for industrial communication protocols such as EtherCAT®, Ethernet/IP, and Profinet.

Sitara™ processors - Reference designs TI provides many reference designs containing ‘building block’ solutions to enable customers to rapidly develop their own unique products and solutions.

Companion Products for AM64x Review products that are frequently purchased or used in conjunction with this product to complete your design.

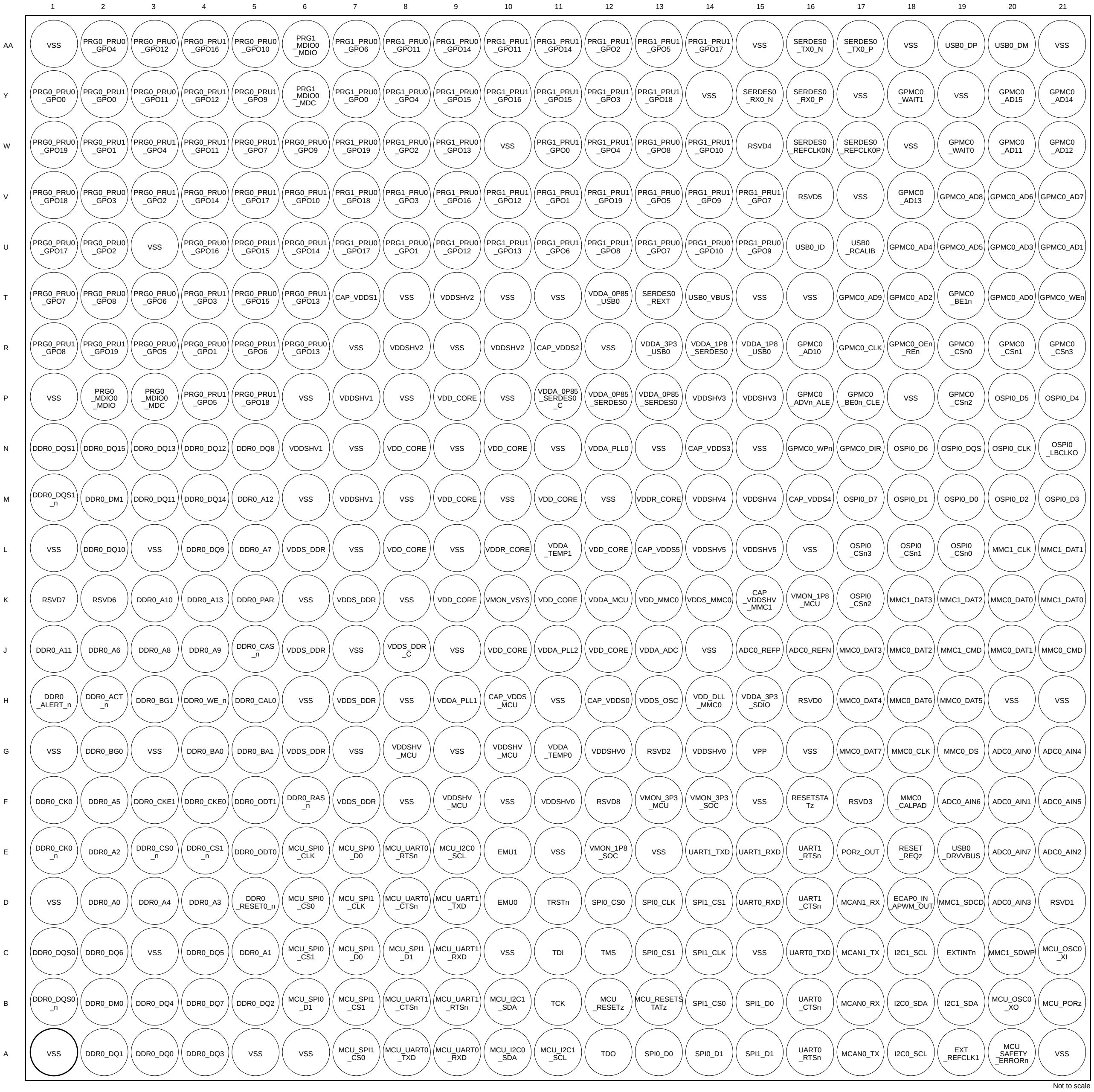
6 Terminal Configuration and Functions

6.1 Pin Diagrams

Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

Figure 6-1 shows the ball locations for the 441-ball flip chip ball grid array (FCBGA) package to quickly locate signal names and ball grid numbering. This figure is used in conjunction with Table 6-1 through Table 6-80 (*Pin Attributes table and all Signal Descriptions tables, including the Connectivity Requirements table*).



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
AA	VSS	PRG0_PRU0_GPO4	PRG0_PRU0_GPO12	PRG0_PRU1_GPO16	PRG0_PRU0_GPO10	PRG1_MDIO0_MDIO	PRG1_PRU0_GPO6	PRG1_PRU0_GPO11	PRG1_PRU0_GPO14	PRG1_PRU1_GPO11	PRG1_PRU1_GPO14	PRG1_PRU1_GPO2	PRG1_PRU1_GPO5	PRG1_PRU1_GPO17	VSS	SERDES0_TX0_N	SERDES0_TX0_P	VSS	USB0_DP	USB0_DM	VSS
Y	PRG0_PRU0_GPO0	PRG0_PRU1_GPO0	PRG0_PRU0_GPO11	PRG0_PRU1_GPO12	PRG0_PRU1_GPO9	PRG1_MDIO0_MDC	PRG1_PRU0_GPO0	PRG1_PRU0_GPO4	PRG1_PRU0_GPO15	PRG1_PRU1_GPO16	PRG1_PRU1_GPO15	PRG1_PRU1_GPO3	PRG1_PRU1_GPO18	VSS	SERDES0_RX0_N	SERDES0_RX0_P	VSS	GPMC0_WAIT1	VSS	GPMC0_AD15	GPMC0_AD14
W	PRG0_PRU0_GPO19	PRG0_PRU1_GPO1	PRG0_PRU1_GPO4	PRG0_PRU1_GPO11	PRG0_PRU1_GPO7	PRG0_PRU0_GPO9	PRG1_PRU0_GPO19	PRG1_PRU0_GPO2	PRG1_PRU0_GPO13	VSS	PRG1_PRU1_GPO0	PRG1_PRU1_GPO4	PRG1_PRU0_GPO8	PRG1_PRU1_GPO10	RSVD4	SERDES0_REFCLK0N	SERDES0_REFCLK0P	VSS	GPMC0_WAIT0	GPMC0_AD11	GPMC0_AD12
V	PRG0_PRU0_GPO18	PRG0_PRU0_GPO3	PRG0_PRU1_GPO2	PRG0_PRU0_GPO14	PRG0_PRU1_GPO17	PRG0_PRU1_GPO10	PRG1_PRU0_GPO18	PRG1_PRU0_GPO3	PRG1_PRU0_GPO16	PRG1_PRU1_GPO12	PRG1_PRU1_GPO1	PRG1_PRU1_GPO19	PRG1_PRU0_GPO5	PRG1_PRU1_GPO9	PRG1_PRU1_GPO7	RSVD5	VSS	GPMC0_AD13	GPMC0_AD8	GPMC0_AD6	GPMC0_AD7
U	PRG0_PRU0_GPO17	PRG0_PRU0_GPO2	VSS	PRG0_PRU0_GPO16	PRG0_PRU1_GPO15	PRG0_PRU1_GPO14	PRG1_PRU0_GPO17	PRG1_PRU0_GPO1	PRG1_PRU0_GPO12	PRG1_PRU1_GPO13	PRG1_PRU1_GPO6	PRG1_PRU1_GPO8	PRG1_PRU0_GPO7	PRG1_PRU0_GPO10	PRG1_PRU0_GPO9	USB0_ID	USB0_RCALIB	GPMC0_AD4	GPMC0_AD5	GPMC0_AD3	GPMC0_AD1
T	PRG0_PRU0_GPO7	PRG0_PRU0_GPO8	PRG0_PRU0_GPO6	PRG0_PRU1_GPO3	PRG0_PRU0_GPO15	PRG0_PRU1_GPO13	CAP_VDDS1	VSS	VDDSHV2	VSS	VSS	VDDA_0P85_USB0	SERDES0_REXT	USB0_VBUS	VSS	VSS	GPMC0_AD9	GPMC0_AD2	GPMC0_BE1n	GPMC0_AD0	GPMC0_WEn
R	PRG0_PRU1_GPO8	PRG0_PRU1_GPO19	PRG0_PRU0_GPO5	PRG0_PRU0_GPO1	PRG0_PRU1_GPO6	PRG0_PRU0_GPO13	VSS	VDDSHV2	VSS	VDDSHV2	CAP_VDDS2	VSS	VDDA_3P3_USB0	VDDA_1P8_SERDES0	VDDA_1P8_USB0	GPMC0_AD10	GPMC0_CLK	GPMC0_OEn_REn	GPMC0_CSn0	GPMC0_CSn1	GPMC0_CSn3
P	VSS	PRG0_MDIO0_MDIO	PRG0_MDIO0_MDC	PRG0_PRU1_GPO5	PRG0_PRU1_GPO18	VSS	VDDSHV1	VSS	VDD_CORE	VSS	VDDA_0P85_SERDES0_C	VDDA_0P85_SERDES0	VDDA_0P85_SERDES0	VDDSHV3	VDDSHV3	GPMC0_ADVn_ALE	GPMC0_BE0n_CLE	VSS	GPMC0_CSn2	OSPI0_D5	OSPI0_D4
N	DDR0_DQS1	DDR0_DQ15	DDR0_DQ13	DDR0_DQ12	DDR0_DQ8	VDDSHV1	VSS	VDD_CORE	VSS	VDD_CORE	VSS	VDDA_PLL0	VSS	CAP_VDDS3	VSS	GPMC0_WPn	GPMC0_DIR	OSPI0_D6	OSPI0_DQS	OSPI0_CLK	OSPI0_LBCLKO
M	DDR0_DQS1_n	DDR0_DM1	DDR0_DQ11	DDR0_DQ14	DDR0_A12	VSS	VDDSHV1	VSS	VDD_CORE	VSS	VDD_CORE	VSS	VDDR_CORE	VDDSHV4	VDDSHV4	CAP_VDDS4	OSPI0_D7	OSPI0_D1	OSPI0_D0	OSPI0_D2	OSPI0_D3
L	VSS	DDR0_DQ10	VSS	DDR0_DQ9	DDR0_A7	VDDS_DDR	VSS	VDD_CORE	VSS	VDDR_CORE	VDDA_TEMP1	VDD_CORE	CAP_VDDS5	VDDSHV5	VDDSHV5	VSS	OSPI0_CSn3	OSPI0_CSn1	OSPI0_CSn0	MMC1_CLK	MMC1_DAT1
K	RSVD7	RSVD6	DDR0_A10	DDR0_A13	DDR0_PAR	VSS	VDDS_DDR	VSS	VDD_CORE	VMON_VSYS	VDD_CORE	VDDA_MCU	VDD_MMC0	VDDS_MMC0	CAP_VDDSHV_MMC1	VMON_1P8_MCU	OSPI0_CSn2	MMC1_DAT3	MMC1_DAT2	MMC0_DAT0	MMC1_DAT0
J	DDR0_A11	DDR0_A6	DDR0_A8	DDR0_A9	DDR0_CAS_n	VDDS_DDR	VSS	VDDS_DDR_C	VSS	VDD_CORE	VDDA_PLL2	VDD_CORE	VDDA_ADC	VSS	ADC0_REFP	ADC0_REFN	MMC0_DAT3	MMC0_DAT2	MMC1_CMD	MMC0_DAT1	MMC0_CMD
H	DDR0_ALERT_n	DDR0_ACT_n	DDR0_BG1	DDR0_WE_n	DDR0_CAL0	VSS	VDDS_DDR	VSS	VDDA_PLL1	CAP_VDDS_MCU	VSS	CAP_VDDS0	VDDS_OSC	VDD_DLL_MMC0	VDDA_3P3_SDIO	RSVD0	MMC0_DAT4	MMC0_DAT6	MMC0_DAT5	VSS	VSS
G	VSS	DDR0_BG0	VSS	DDR0_BA0	DDR0_BA1	VDDS_DDR	VSS	VDDSHV_MCU	VSS	VDDSHV_MCU	VDDA_TEMP0	VDDSHV0	RSVD2	VDDSHV0	VPP	VSS	MMC0_DAT7	MMC0_CLK	MMC0_DS	ADC0_AIN0	ADC0_AIN4
F	DDR0_CK0	DDR0_A5	DDR0_CKE1	DDR0_CKE0	DDR0_ODT1	DDR0_RAS_n	VDDS_DDR	VSS	VDDSHV_MCU	VSS	VDDSHV0	RSVD8	VMON_3P3_MCU	VMON_3P3_SOC	VSS	RESETSTATz	RSVD3	MMC0_CALPAD	ADC0_AIN6	ADC0_AIN1	ADC0_AIN5
E	DDR0_CK0_n	DDR0_A2	DDR0_CS0_n	DDR0_CS1_n	DDR0_ODT0	MCU_SPI0_CLK	MCU_SPI0_D0	MCU_UART0_RTSn	MCU_I2C0_SCL	EMU1	VSS	VMON_1P8_SOC	VSS	UART1_TXD	UART1_RXD	UART1_RTSn	PORz_OUT	RESET_REQz	USB0_DRVVBUS	ADC0_AIN7	ADC0_AIN2
D	VSS	DDR0_A0	DDR0_A4	DDR0_A3	DDR0_RESET0_n	MCU_SPI0_CS0	MCU_SPI1_CLK	MCU_UART0_CTSn	MCU_UART1_TXD	EMU0	TRSTn	SPI0_CS0	SPI0_CLK	SPI1_CS1	UART0_RXD	UART1_CTSn	MCAN1_RX	ECAP0_IN_APWM_OUT	MMC1_SDCD	ADC0_AIN3	RSVD1
C	DDR0_DQS0	DDR0_DQ6	VSS	DDR0_DQ5	DDR0_A1	MCU_SPI0_CS1	MCU_SPI1_D0	MCU_SPI1_D1	MCU_UART1_RXD	VSS	TDI	TMS	SPI0_CS1	SPI1_CLK	VSS	UART0_TXD	MCAN1_TX	I2C1_SCL	EXTINTn	MMC1_SDWP	MCU_OSC0_XI
B	DDR0_DQS0_n	DDR0_DM0	DDR0_DQ4	DDR0_DQ7	DDR0_DQ2	MCU_SPI0_D1	MCU_SPI1_CS1	MCU_UART1_CTSn	MCU_UART1_RTSn	MCU_I2C1_SDA	TCK	MCU_RESETz	MCU_RESETSTATz	SPI1_CS0	SPI1_D0	UART0_CTSn	MCAN0_RX	I2C0_SDA	I2C1_SDA	MCU_OSC0_XO	MCU_PORz
A	VSS	DDR0_DQ1	DDR0_DQ0	DDR0_DQ3	VSS	VSS	MCU_SPI1_CS0	MCU_UART0_TXD	MCU_UART0_RXD	MCU_I2C0_SDA	MCU_I2C1_SCL	TDO	SPI0_D0	SPI0_D1	SPI1_D1	UART0_RTSn	MCAN0_TX	I2C0_SCL	EXT_REFCLK1	MCU_SAFETY_ERRORn	VSS

Not to scale

Figure 6-1. ALV FCBGA-N441 Pin Diagram (Bottom View)

6.2 Pin Attributes

The following list describes the contents of each column in Table 6-1, *Pin Attributes*:

1. **BALL NUMBER:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **BALL NAME:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **SIGNAL NAME:** Signal name(s) of all dedicated and pin multiplexed signal functions associated with a ball.

Note

Many device pins support multiple signal functions. Some signal functions are selected via a single layer of multiplexers associated with pins. Other signal functions are selected via two or more layers of multiplexers, where one layer is associated with the pins and other layers are associated with peripheral logic functions.

Table 6-1, *Pin Attributes* only defines signal multiplexing at the pins. For more information, related to signal multiplexing at the pins, see the *Pad Configuration Registers* section in the *Device Configuration* chapter of the device TRM. For information associated with peripheral signal multiplexing, see the respective peripheral chapter in the device TRM.

4. **MUX MODE:** The MUXMODE value associated with each pin multiplexed signal function:
   a. MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.

Note

The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when MCU_PORz is deasserted.

   b. MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only valid values of MUXMODE should be used.
   c. Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz_OUT. These input signal functions are fixed to their respective pins and are not programmable via MUXMODE.
   d. An empty box means Not Applicable.

Note

The following configurations of MUXMODE must be avoided for proper device operation.

- Configuring multiple pins operating as inputs to the same pin multiplexed signal function is not supported as it can yield unexpected results.
- Configuring a pin to an undefined pin multiplexing mode will cause the pin behavior to be undefined.

5. **TYPE:** Signal type and direction:
   - I = Input
   - O = Output
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - PWR = Power
   - GND = Ground
   - CAP = LDO Capacitor.
6. **DSIS:** The deselected input state (DSIS) indicates the state driven to the subsystem input (logic "0", logic "1", or "pad" level) when the pin multiplexed signal function is not selected by MUXMODE.
   - 0: Logic 0 driven to the subsystem input.
   - 1: Logic 1 driven to the subsystem input.
   - pad: Logic state of the pad is driven to the subsystem input.
   - An empty box means Not Applicable.
7. **BALL STATE DURING RESET RX/TX/PULL:** State of the terminal while MCU_PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is disabled.
     - On: The input buffer is enabled.
   - TX (Output buffer)
     - Off: The output buffer is disabled.
     - Low: The output buffer is enabled and drives V_{OL}.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned off.
     - Up: Internal pull-up resistor is turned on.
     - Down: Internal pull-down resistor is turned on.
     - NA: Not Applicable.
   - An empty box means Not Applicable.
8. **BALL STATE AFTER RESET RX/TX/PULL:** State of the terminal after MCU_PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is disabled.
     - On: The input buffer is enabled.
   - TX (Output buffer)
     - Off: The output buffer is disabled.
     - SS: The subsystem selected with MUXMODE determines the output buffer state.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned off.
     - Up: Internal pull-up resistor is turned on.
     - Down: Internal pull-down resistor is turned on.
     - NA: Not Applicable.
   - An empty box means Not Applicable.
9. **MUX MODE AFTER RESET:** The value found in this column defines the default pin multiplexed signal function after MCU_PORz is deasserted.

   An empty box means Not Applicable.

10. **I/O OPERATING VOLTAGE**: This column describes I/O operating voltage options of the respective power supply, when applicable.

    An empty box means Not Applicable.

    For more information, see valid operating voltage range(s) defined for each power supply in Section 7.4, *Recommended Operating Conditions*.

11. **POWER:** The power supply of the associated I/O, when applicable.

    An empty box means Not Applicable.

12. **HYS:** Indicates if the input buffer associated with this I/O has hysteresis:
    - Yes: With hysteresis
    - No: Without hysteresis
    - An empty box means Not Applicable.

    For more information, see the hysteresis values in Section 7.7, *Electrical Characteristics*.

13. **BUFFER TYPE:** This column defines the buffer type associated with a terminal. This information can be used to determine which Electrical Characteristics table is applicable.

    An empty box means Not Applicable.

    For electrical characteristics, refer to the appropriate buffer type table in Section 7.7, *Electrical Characteristics*.

14. **PULL UP/DOWN TYPE:** Indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
    - PU: Internal pull-up
    - PD: Internal pull-down
    - PU/PD: Internal pull-up and pull-down
    - An empty box means No internal pull.

15. **PADCONFIG Register:**Name of the IO pad configuration register associated with Ball.

16. **PADCONFIG Address:**Physical address of the IO pad configuration register associated with Ball.

Table 6-1. Pin Attributes (ALV Package)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
J16	ADC0_REFN	ADC0_REFN		A					1.8 V	VDDA_ADC0		ADC12B	
J15	ADC0_REFP	ADC0_REFP		A					1.8 V	VDDA_ADC0		ADC12B	
G20	ADC0_AIN0	ADC0_AIN0		A					1.8 V	VDDA_ADC0	Yes	ADC12B	
F20	ADC0_AIN1	ADC0_AIN1		A					1.8 V	VDDA_ADC0	Yes	ADC12B	
E21	ADC0_AIN2	ADC0_AIN2		A					1.8 V	VDDA_ADC0	Yes	ADC12B	
D20	ADC0_AIN3	ADC0_AIN3		A					1.8 V	VDDA_ADC0	Yes	ADC12B	
G21	ADC0_AIN4	ADC0_AIN4		A					1.8 V	VDDA_ADC0	Yes	ADC12B	
F21	ADC0_AIN5	ADC0_AIN5		A					1.8 V	VDDA_ADC0	Yes	ADC12B	
F19	ADC0_AIN6	ADC0_AIN6		A					1.8 V	VDDA_ADC0	Yes	ADC12B	
E20	ADC0_AIN7	ADC0_AIN7		A					1.8 V	VDDA_ADC0	Yes	ADC12B	
H12	CAP_VDDS0	CAP_VDDS0		CAP									
T7	CAP_VDDS1	CAP_VDDS1		CAP									
R11	CAP_VDDS2	CAP_VDDS2		CAP									
N14	CAP_VDDS3	CAP_VDDS3		CAP									
M16	CAP_VDDS4	CAP_VDDS4		CAP									
L13	CAP_VDDS5	CAP_VDDS5		CAP									
K15	CAP_VDDSHV_MMC1	CAP_VDDSHV_MMC1		CAP									
H10	CAP_VDDS_MCU	CAP_VDDS_MCU		CAP									
H2	DDR0_ACT_n	DDR0_ACT_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H1	DDR0_ALERT_n	DDR0_ALERT_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J5	DDR0_CAS_n	DDR0_CAS_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K5	DDR0_PAR	DDR0_PAR		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F6	DDR0_RAS_n	DDR0_RAS_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H4	DDR0_WE_n	DDR0_WE_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D2	DDR0_A0	DDR0_A0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
C5	DDR0_A1	DDR0_A1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E2	DDR0_A2	DDR0_A2		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D4	DDR0_A3	DDR0_A3		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D3	DDR0_A4	DDR0_A4		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
F2	DDR0_A5	DDR0_A5		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J2	DDR0_A6	DDR0_A6		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L5	DDR0_A7	DDR0_A7		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J3	DDR0_A8	DDR0_A8		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J4	DDR0_A9	DDR0_A9		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K3	DDR0_A10	DDR0_A10		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J1	DDR0_A11	DDR0_A11		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M5	DDR0_A12	DDR0_A12		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K4	DDR0_A13	DDR0_A13		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G4	DDR0_BA0	DDR0_BA0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G5	DDR0_BA1	DDR0_BA1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G2	DDR0_BG0	DDR0_BG0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H3	DDR0_BG1	DDR0_BG1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H5	DDR0_CAL0	DDR0_CAL0		A					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F1	DDR0_CK0	DDR0_CK0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E1	DDR0_CK0_n	DDR0_CK0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F4	DDR0_CKE0	DDR0_CKE0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F3	DDR0_CKE1	DDR0_CKE1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E3	DDR0_CS0_n	DDR0_CS0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E4	DDR0_CS1_n	DDR0_CS1_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
B2	DDR0_DM0	DDR0_DM0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M2	DDR0_DM1	DDR0_DM1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A3	DDR0_DQ0	DDR0_DQ0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
A2	DDR0_DQ1	DDR0_DQ1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
B5	DDR0_DQ2	DDR0_DQ2		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
A4	DDR0_DQ3	DDR0_DQ3		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
B3	DDR0_DQ4	DDR0_DQ4		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
C4	DDR0_DQ5	DDR0_DQ5		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
C2	DDR0_DQ6	DDR0_DQ6		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
B4	DDR0_DQ7	DDR0_DQ7		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N5	DDR0_DQ8	DDR0_DQ8		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L4	DDR0_DQ9	DDR0_DQ9		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L2	DDR0_DQ10	DDR0_DQ10		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M3	DDR0_DQ11	DDR0_DQ11		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N4	DDR0_DQ12	DDR0_DQ12		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N3	DDR0_DQ13	DDR0_DQ13		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M4	DDR0_DQ14	DDR0_DQ14		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N2	DDR0_DQ15	DDR0_DQ15		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
C1	DDR0_DQS0	DDR0_DQS0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
B1	DDR0_DQS0_n	DDR0_DQS0_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N1	DDR0_DQS1	DDR0_DQS1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M1	DDR0_DQS1_n	DDR0_DQS1_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E5	DDR0_ODT0	DDR0_ODT0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F5	DDR0_ODT1	DDR0_ODT1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
D5	DDR0_RESET0_n	DDR0_RESET0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D18	ECAP0_IN_APWM_OUT PADCONFIG: PADCONFIG156 0x000F4270	ECAP0_IN_APWM_OUT	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SYNC0_OUT	1	O									
		CPTS0_RFT_CLK	2	I	0								
		CP_GEMAC_CPTS0_RFT_CLK	5	I	0								
		SPI4_CS3	6	IO	1								
		GPIO1_68	7	IO	pad								
D10	EMU0 PADCONFIG: MCU_PADCONFIG31 0x0408407C	EMU0	0	IO	1	On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
E10	EMU1 PADCONFIG: MCU_PADCONFIG32 0x04084080	EMU1	0	IO	1	On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_OBSCLK0	15	O									
C19	EXTINTn PADCONFIG: PADCONFIG158 0x000F4278	EXTINTn	0	I	1	Off / Off / NA	Off / Off / NA	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OD FS	
		GPIO1_70	7	IOD	pad								
A19	EXT_REFCLK1 PADCONFIG: PADCONFIG157 0x000F4274	EXT_REFCLK1	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SYNC1_OUT	1	O									
		SPI2_CS3	2	IO	1								
		CLKOUT0	5	O									
		GPIO1_69	7	IO	pad								
P16	GPMC0_ADVn_ALE PADCONFIG: PADCONFIG33 0x000F4084	GPMC0_ADVn_ALE	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX5_CLK	1	I	0								
		UART5_RXD	2	I	1								
		EHRPWM_TZn_IN3	3	I	0								
		TRC_DATA15	6	O									
		GPIO0_32	7	IO	pad								
		PRG0_PWM3_TZ_IN	9	I	0								
R17	GPMC0_CLK PADCONFIG: PADCONFIG31 0x000F407C	GPMC0_CLK	0	O	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX4_CLK	1	I	0								
		UART4_RTSn	2	O									
		EHRPWM3_SYNCO	3	O									
		GPMC0_FCLK_MUX	4	O									
		TRC_DATA14	6	O									
		GPIO0_31	7	IO	pad								
		PRG0_PWM3_TZ_OUT	9	O									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
N17	GPMC0_DIR PADCONFIG: PADCONFIG41 0x000F40A4	GPMC0_DIR	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		EQEP0_B	3	I	0								
		GPIO0_40	7	IO	pad								
		EHRPWM6_B	8	IO	0								
		PRG1_PWM2_B0	9	IO	1								
R18	GPMC0_OEn_REn PADCONFIG: PADCONFIG34 0x000F4088	GPMC0_OEn_REn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX5_D0	1	I	0								
		UART5_TXD	2	O									
		EHRPWM4_A	3	IO	0								
		TRC_DATA16	6	O									
		GPIO0_33	7	IO	pad								
		PRG0_PWM3_A1	9	IO	0								
T21	GPMC0_WEn PADCONFIG: PADCONFIG35 0x000F408C	GPMC0_WEn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX5_D1	1	I	0								
		UART5_RTSn	2	O									
		EHRPWM4_B	3	IO	0								
		TRC_DATA17	6	O									
		GPIO0_34	7	IO	pad								
		PRG0_PWM3_B1	9	IO	1								
N16	GPMC0_WPn PADCONFIG: PADCONFIG40 0x000F40A0	GPMC0_WPn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_TX1_CLK	1	O									
		EQEP0_A	3	I	0								
		GPMC0_A22	4	OZ									
		TRC_DATA22	6	O									
		GPIO0_39	7	IO	pad								
		EHRPWM6_A	8	IO	0								
		PRG1_PWM2_A0	9	IO	0								
T20	GPMC0_AD0 PADCONFIG: PADCONFIG15 0x000F403C	GPMC0_AD0	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX2_CLK	1	I	0								
		UART2_RXD	2	I	1								
		EHRPWM0_SYNCI	3	I	0								
		TRC_CLK	6	O									
		GPIO0_15	7	IO	pad								
		BOOTMODE00	Bootstrap	I									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
U21	GPMC0_AD1 PADCONFIG: PADCONFIG16 0x000F4040	GPMC0_AD1	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX2_D0	1	I	0								
		UART2_TXD	2	O									
		EHRPWM0_SYNCO	3	O									
		TRC_CTL	6	O									
		GPIO0_16	7	IO	pad								
		PRG0_PWM2_TZ_OUT	9	O									
		BOOTMODE01	Bootstrap	I									
T18	GPMC0_AD2 PADCONFIG: PADCONFIG17 0x000F4044	GPMC0_AD2	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX2_D1	1	I	0								
		UART2_RTSn	2	O									
		EHRPWM_TZn_IN0	3	I	0								
		TRC_DATA0	6	O									
		GPIO0_17	7	IO	pad								
		PRG0_PWM2_TZ_IN	9	I	0								
		BOOTMODE02	Bootstrap	I									
U20	GPMC0_AD3 PADCONFIG: PADCONFIG18 0x000F4048	GPMC0_AD3	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX3_CLK	1	I	0								
		UART3_RXD	2	I	1								
		EHRPWM0_A	3	IO	0								
		TRC_DATA1	6	O									
		GPIO0_18	7	IO	pad								
		PRG0_PWM2_A0	9	IO	0								
		BOOTMODE03	Bootstrap	I									
U18	GPMC0_AD4 PADCONFIG: PADCONFIG19 0x000F404C	GPMC0_AD4	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX3_D0	1	I	0								
		UART3_TXD	2	O									
		EHRPWM0_B	3	IO	0								
		TRC_DATA2	6	O									
		GPIO0_82	7	IO	pad								
		PRG0_PWM2_B0	9	IO	1								
		BOOTMODE04	Bootstrap	I									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
U19	GPMC0_AD5 PADCONFIG: PADCONFIG20 0x000F4050	GPMC0_AD5	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX3_D1	1	I	0								
		UART3_RTSn	2	O									
		EHRPWM1_A	3	IO	0								
		TRC_DATA3	6	O									
		GPIO0_83	7	IO	pad								
		PRG0_PWM2_A1	9	IO	0								
		BOOTMODE05	Bootstrap	I									
V20	GPMC0_AD6 PADCONFIG: PADCONFIG21 0x000F4054	GPMC0_AD6	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX4_D0	1	I	0								
		UART4_RXD	2	I	1								
		EHRPWM1_B	3	IO	0								
		TRC_DATA4	6	O									
		GPIO0_21	7	IO	pad								
		PRG0_PWM2_B1	9	IO	1								
		BOOTMODE06	Bootstrap	I									
V21	GPMC0_AD7 PADCONFIG: PADCONFIG22 0x000F4058	GPMC0_AD7	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX4_D1	1	I	0								
		UART4_TXD	2	O									
		EHRPWM_TZn_IN1	3	I	0								
		EHRPWM8_A	4	IO	0								
		TRC_DATA5	6	O									
		GPIO0_22	7	IO	pad								
		PRG1_PWM2_A2	9	IO	0								
		BOOTMODE07	Bootstrap	I									
V19	GPMC0_AD8 PADCONFIG: PADCONFIG23 0x000F405C	GPMC0_AD8	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX0_CLK	1	I	0								
		UART2_CTSn	2	I	1								
		EHRPWM2_A	3	IO	0								
		TRC_DATA6	6	O									
		GPIO0_23	7	IO	pad								
		PRG0_PWM2_A2	9	IO	0								
		BOOTMODE08	Bootstrap	I									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
T17	GPMC0_AD9 PADCONFIG: PADCONFIG24 0x000F4060	GPMC0_AD9	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX0_D0	1	I	0								
		UART3_CTSn	2	I	1								
		EHRPWM2_B	3	IO	0								
		TRC_DATA7	6	O									
		GPIO0_24	7	IO	pad								
		PRG0_PWM2_B2	9	IO	1								
		BOOTMODE09	Bootstrap	I									
R16	GPMC0_AD10 PADCONFIG: PADCONFIG25 0x000F4064	GPMC0_AD10	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX0_D1	1	I	0								
		UART4_CTSn	2	I	1								
		EHRPWM_TZn_IN2	3	I	0								
		EHRPWM8_B	4	IO	0								
		TRC_DATA8	6	O									
		GPIO0_25	7	IO	pad								
		PRG1_PWM2_B2	9	IO	1								
		BOOTMODE10	Bootstrap	I									
W20	GPMC0_AD11 PADCONFIG: PADCONFIG26 0x000F4068	GPMC0_AD11	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX1_CLK	1	I	0								
		UART5_CTSn	2	I	1								
		EQEP1_A	3	I	0								
		TRC_DATA9	6	O									
		GPIO0_26	7	IO	pad								
		EHRPWM7_A	8	IO	0								
		BOOTMODE11	Bootstrap	I									
W21	GPMC0_AD12 PADCONFIG: PADCONFIG27 0x000F406C	GPMC0_AD12	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX1_D0	1	I	0								
		UART6_CTSn	2	I	1								
		EQEP1_B	3	I	0								
		TRC_DATA10	6	O									
		GPIO0_27	7	IO	pad								
		EHRPWM7_B	8	IO	0								
		BOOTMODE12	Bootstrap	I									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
V18	GPMC0_AD13 PADCONFIG: PADCONFIG28 0x000F4070	GPMC0_AD13	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX1_D1	1	I	0								
		EHRPWM3_A	3	IO	0								
		TRC_DATA11	6	O									
		GPIO0_28	7	IO	pad								
		PRG0_PWM3_A0	9	IO	0								
		BOOTMODE13	Bootstrap	I									
Y21	GPMC0_AD14 PADCONFIG: PADCONFIG29 0x000F4074	GPMC0_AD14	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_TX0_D0	1	O									
		UART6_RXD	2	I	1								
		EHRPWM3_B	3	IO	0								
		TRC_DATA12	6	O									
		GPIO0_29	7	IO	pad								
		PRG0_PWM3_B0	9	IO	1								
		BOOTMODE14	Bootstrap	I									
Y20	GPMC0_AD15 PADCONFIG: PADCONFIG30 0x000F4078	GPMC0_AD15	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_TX0_D1	1	O									
		UART6_TXD	2	O									
		EHRPWM3_SYNCI	3	I	0								
		TRC_DATA13	6	O									
		GPIO0_30	7	IO	pad								
		BOOTMODE15	Bootstrap	I									
P17	GPMC0_BE0n_CLE PADCONFIG: PADCONFIG36 0x000F4090	GPMC0_BE0n_CLE	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_TX1_D0	1	O									
		UART6_RTSn	2	O									
		EHRPWM_TZn_IN4	3	I	0								
		EHRPWM7_A	5	IO	0								
		TRC_DATA18	6	O									
		GPIO0_35	7	IO	pad								
		PRG1_PWM2_A1	9	IO	0								
T19	GPMC0_BE1n PADCONFIG: PADCONFIG37 0x000F4094	GPMC0_BE1n	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_TX0_CLK	1	O									
		EHRPWM5_A	3	IO	0								
		TRC_DATA19	6	O									
		GPIO0_36	7	IO	pad								
		PRG0_PWM3_A2	9	IO	0								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
R19	GPMC0_CSn0 PADCONFIG: PADCONFIG42 0x000F40A8	GPMC0_CSn0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		EQEP0_S	3	IO	0								
		TRC_DATA23	6	O									
		GPIO0_41	7	IO	pad								
		EHRPWM6_SYNCI	8	I	0								
R20	GPMC0_CSn1 PADCONFIG: PADCONFIG43 0x000F40AC	GPMC0_CSn1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		EQEP0_I	3	IO	0								
		EHRPWM_TZn_IN2	5	I	0								
		GPIO0_42	7	IO	pad								
		EHRPWM6_SYNCO	8	O									
		PRG1_PWM2_TZ_OUT	9	O									
P19	GPMC0_CSn2 PADCONFIG: PADCONFIG44 0x000F40B0	GPMC0_CSn2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C2_SCL	1	IOD	1								
		TIMER_IO8	2	IO	0								
		EQEP1_S	3	IO	0								
		EHRPWM_TZn_IN4	5	I	0								
		GPIO0_43	7	IO	pad								
		PRG1_PWM2_TZ_IN	9	I	0								
R21	GPMC0_CSn3 PADCONFIG: PADCONFIG45 0x000F40B4	GPMC0_CSn3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C2_SDA	1	IOD	1								
		TIMER_IO9	2	IO	0								
		EQEP1_I	3	IO	0								
		GPMC0_A20	4	OZ									
		EHRPWM_TZn_IN5	5	I	0								
		GPIO0_44	7	IO	pad								
W19	GPMC0_WAIT0 PADCONFIG: PADCONFIG38 0x000F4098	GPMC0_WAIT0	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		EHRPWM5_B	3	IO	0								
		TRC_DATA20	6	O									
		GPIO0_37	7	IO	pad								
		PRG0_PWM3_B2	9	IO	1								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
Y18	GPMC0_WAIT1 PADCONFIG: PADCONFIG39 0x000F409C	GPMC0_WAIT1	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_TX1_D1	1	O									
		EHRPWM_TZn_IN5	3	I	0								
		GPMC0_A21	4	OZ									
		EHRPWM7_B	5	IO	0								
		TRC_DATA21	6	O									
		GPIO0_38	7	IO	pad								
		PRG1_PWM2_B1	9	IO	1								
A18	I2C0_SCL PADCONFIG: PADCONFIG152 0x000F4260	I2C0_SCL	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OD FS	
		GPIO1_64	7	IOD	pad								
B18	I2C0_SDA PADCONFIG: PADCONFIG153 0x000F4264	I2C0_SDA	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OD FS	
		GPIO1_65	7	IOD	pad								
C18	I2C1_SCL PADCONFIG: PADCONFIG154 0x000F4268	I2C1_SCL	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CPTS0_HW1TSPUSH	1	I	0								
		TIMER_IO0	2	IO	0								
		SPI2_CS1	3	IO	1								
		GPIO1_66	7	IO	pad								
B19	I2C1_SDA PADCONFIG: PADCONFIG155 0x000F426C	I2C1_SDA	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CPTS0_HW2TSPUSH	1	I	0								
		TIMER_IO1	2	IO	0								
		SPI2_CS2	3	IO	1								
		GPIO1_67	7	IO	pad								
B17	MCAN0_RX PADCONFIG: PADCONFIG149 0x000F4254	MCAN0_RX	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART4_TXD	1	O									
		TIMER_IO3	2	IO	0								
		SYNC3_OUT	3	O									
		SPI4_CS2	6	IO	1								
		GPIO1_61	7	IO	pad								
		EQEP2_S	8	IO	0								
		UART0_RIn	9	I	1								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A17	MCAN0_TX PADCONFIG: PADCONFIG148 0x000F4250	MCAN0_TX	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART4_RXD	1	I	1								
		TIMER_IO2	2	IO	0								
		SYNC2_OUT	3	O									
		SPI4_CS1	6	IO	1								
		GPIO1_60	7	IO	pad								
		EQEP2_I	8	IO	0								
		UART0_DTRn	9	O									
D17	MCAN1_RX PADCONFIG: PADCONFIG151 0x000F425C	MCAN1_RX	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		I2C3_SDA	1	IOD	1								
		ECAP2_IN_APWM_OUT	2	IO	0								
		OBSCLK0	3	O									
		TIMER_IO5	4	IO	0								
		UART5_TXD	5	O									
		EHRPWM_SOCB	6	O									
		GPIO1_63	7	IO	pad								
		EQEP2_B	8	I	0								
		UART0_DSRn	9	I	1								
		OBSCLK0	15	O									
C17	MCAN1_TX PADCONFIG: PADCONFIG150 0x000F4258	MCAN1_TX	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		I2C3_SCL	1	IOD	1								
		ECAP1_IN_APWM_OUT	2	IO	0								
		SYSCLKOUT0	3	O									
		TIMER_IO4	4	IO	0								
		UART5_RXD	5	I	1								
		EHRPWM_SOCA	6	O									
		GPIO1_62	7	IO	pad								
		EQEP2_A	8	I	0								
		UART0_DCDn	9	I	1								
E9	MCU_I2C0_SCL PADCONFIG: MCU_PADCONFIG18 0x04084048	MCU_I2C0_SCL	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OD FS	
		MCU_GPIO0_18	7	IOD	pad								
A10	MCU_I2C0_SDA PADCONFIG: MCU_PADCONFIG19 0x0408404C	MCU_I2C0_SDA	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OD FS	
		MCU_GPIO0_19	7	IOD	pad								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A11	MCU_I2C1_SCL	MCU_I2C1_SCL	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG: MCU_PADCONFIG20 0x04084050	MCU_GPIO0_20	7	IO	pad								
B10	MCU_I2C1_SDA	MCU_I2C1_SDA	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG: MCU_PADCONFIG21 0x04084054	MCU_GPIO0_21	7	IO	pad								
C21	MCU_OSC0_XI	MCU_OSC0_XI		I					1.8 V	VDDS_OSC	Yes	HFOSC	
B20	MCU_OSC0_XO	MCU_OSC0_XO		O					1.8 V	VDDS_OSC	Yes	HFOSC	
B21	MCU_PORz PADCONFIG: MCU_PADCONFIG23 0x0408405C	MCU_PORz	0	I				0	1.8 V	VDDS_OSC	Yes	FS RESET	
B13	MCU_RESETSTATz	MCU_RESETSTATz	0	O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG: MCU_PADCONFIG24 0x04084060	MCU_GPIO0_22	7	IO	pad								
B12	MCU_RESETz PADCONFIG: MCU_PADCONFIG22 0x04084058	MCU_RESETz	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
A20	MCU_SAFETY_ERRORn PADCONFIG: MCU_PADCONFIG25 0x04084064	MCU_SAFETY_ERRORn	0	IO		Off / Off / Down	On / SS / Down	0	1.8 V	VDDS_OSC	Yes	LVCMOS	PU/PD
E6	MCU_SPI0_CLK	MCU_SPI0_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG: MCU_PADCONFIG2 0x04084008	MCU_GPIO0_11	7	IO	pad								
D7	MCU_SPI1_CLK	MCU_SPI1_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG: MCU_PADCONFIG7 0x0408401C	MCU_GPIO0_7	7	IO	pad								
D6	MCU_SPI0_CS0	MCU_SPI0_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
	PADCONFIG: MCU_PADCONFIG0 0x04084000	MCU_GPIO0_13	7	IO	pad								
C6	MCU_SPI0_CS1 PADCONFIG: MCU_PADCONFIG1 0x04084004	MCU_SPI0_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_OBSCLK0	1	O									
		MCU_SYSCLKOUT0	2	O									
		MCU_GPIO0_12	7	IO	pad								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
E7	MCU_SPI0_D0 PADCONFIG: MCU_PADCONFIG3 0x0408400C	MCU_SPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_10	7	IO	pad								
B6	MCU_SPI0_D1 PADCONFIG: MCU_PADCONFIG4 0x04084010	MCU_SPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_4	7	IO	pad								
A7	MCU_SPI1_CS0 PADCONFIG: MCU_PADCONFIG5 0x04084014	MCU_SPI1_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_5	7	IO	pad								
B7	MCU_SPI1_CS1 PADCONFIG: MCU_PADCONFIG6 0x04084018	MCU_SPI1_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_EXT_REFCLK0	1	I	0								
		MCU_GPIO0_6	7	IO	pad								
C7	MCU_SPI1_D0 PADCONFIG: MCU_PADCONFIG8 0x04084020	MCU_SPI1_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_8	7	IO	pad								
C8	MCU_SPI1_D1 PADCONFIG: MCU_PADCONFIG9 0x04084024	MCU_SPI1_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_9	7	IO	pad								
D8	MCU_UART0_CTSn PADCONFIG: MCU_PADCONFIG12 0x04084030	MCU_UART0_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO0	1	IO	0								
		MCU_SPI0_CS2	2	IO	1								
		MCU_GPIO0_1	7	IO	pad								
E8	MCU_UART0_RTSn PADCONFIG: MCU_PADCONFIG13 0x04084034	MCU_UART0_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO1	1	IO	0								
		MCU_SPI1_CS2	2	IO	1								
		MCU_GPIO0_0	7	IO	pad								
A9	MCU_UART0_RXD PADCONFIG: MCU_PADCONFIG10 0x04084028	MCU_UART0_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_3	7	IO	pad								
A8	MCU_UART0_TXD PADCONFIG: MCU_PADCONFIG11 0x0408402C	MCU_UART0_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_2	7	IO	pad								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
B8	MCU_UART1_CTSn PADCONFIG: MCU_PADCONFIG16 0x04084040	MCU_UART1_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO2	1	IO	0								
		MCU_SPI0_CS3	2	IO	1								
		MCU_GPIO0_16	7	IO	pad								
B9	MCU_UART1_RTSn PADCONFIG: MCU_PADCONFIG17 0x04084044	MCU_UART1_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO3	1	IO	0								
		MCU_SPI1_CS3	2	IO	1								
		MCU_GPIO0_17	7	IO	pad								
C9	MCU_UART1_RXD PADCONFIG: MCU_PADCONFIG14 0x04084038	MCU_UART1_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_14	7	IO	pad								
D9	MCU_UART1_TXD PADCONFIG: MCU_PADCONFIG15 0x0408403C	MCU_UART1_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_15	7	IO	pad								
F18	MMC0_CALPAD	MMC0_CALPAD		A					1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	
G18	MMC0_CLK	MMC0_CLK		IO		On / Low / Off	On / SS / Off		1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
J21	MMC0_CMD	MMC0_CMD		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
G19	MMC0_DS	MMC0_DS		IO		On / Off / Down	On / Off / Down		1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
L20	MMC1_CLK PADCONFIG: PADCONFIG163 0x000F428C	MMC1_CLK	0	IO		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART2_CTSn	1	I	1								
		TIMER_IO4	2	IO	0								
		UART4_RXD	3	I	1								
		GPIO1_75	7	IO	pad								
J19	MMC1_CMD PADCONFIG: PADCONFIG165 0x000F4294	MMC1_CMD	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART2_RTSn	1	O									
		TIMER_IO5	2	IO	0								
		UART4_TXD	3	O									
		GPIO1_76	7	IO	pad								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
D19	MMC1_SDCD PADCONFIG: PADCONFIG166 0x000F4298	MMC1_SDCD	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART3_CTSn	1	I	1								
		TIMER_IO6	2	IO	0								
		UART5_RXD	3	I	1								
		GPIO1_77	7	IO	pad								
C20	MMC1_SDWP PADCONFIG: PADCONFIG167 0x000F429C	MMC1_SDWP	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART3_RTSn	1	O									
		TIMER_IO7	2	IO	0								
		UART5_TXD	3	O									
		GPIO1_78	7	IO	pad								
K20	MMC0_DAT0	MMC0_DAT0		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
J20	MMC0_DAT1	MMC0_DAT1		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
J18	MMC0_DAT2	MMC0_DAT2		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
J17	MMC0_DAT3	MMC0_DAT3		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
H17	MMC0_DAT4	MMC0_DAT4		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
H19	MMC0_DAT5	MMC0_DAT5		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
H18	MMC0_DAT6	MMC0_DAT6		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
G17	MMC0_DAT7	MMC0_DAT7		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
K21	MMC1_DAT0 PADCONFIG: PADCONFIG162 0x000F4288	MMC1_DAT0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_HW2TSPUSH	1	I	0								
		TIMER_IO3	2	IO	0								
		UART3_TXD	3	O									
		GPIO1_74	7	IO	pad								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
L21	MMC1_DAT1 PADCONFIG: PADCONFIG161 0x000F4284	MMC1_DAT1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_HW1TSPUSH	1	I	0								
		TIMER_IO2	2	IO	0								
		UART3_RXD	3	I	1								
		GPIO1_73	7	IO	pad								
K19	MMC1_DAT2 PADCONFIG: PADCONFIG160 0x000F4280	MMC1_DAT2	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_TS_SYNC	1	O									
		TIMER_IO1	2	IO	0								
		UART2_TXD	3	O									
		GPIO1_72	7	IO	pad								
K18	MMC1_DAT3 PADCONFIG: PADCONFIG159 0x000F427C	MMC1_DAT3	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_TS_COMP	1	O									
		TIMER_IO0	2	IO	0								
		UART2_RXD	3	I	1								
		GPIO1_71	7	IO	pad								
N20	OSPI0_CLK PADCONFIG: PADCONFIG0 0x000F4000	OSPI0_CLK	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_0	7	IO	pad								
N19	OSPI0_DQS PADCONFIG: PADCONFIG2 0x000F4008	OSPI0_DQS	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_2	7	IO	pad								
N21	OSPI0_LBCLKO PADCONFIG: PADCONFIG1 0x000F4004	OSPI0_LBCLKO	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_1	7	IO	pad								
L19	OSPI0_CSn0 PADCONFIG: PADCONFIG11 0x000F402C	OSPI0_CSn0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_11	7	IO	pad								
L18	OSPI0_CSn1 PADCONFIG: PADCONFIG12 0x000F4030	OSPI0_CSn1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_12	7	IO	pad								
K17	OSPI0_CSn2 PADCONFIG: PADCONFIG13 0x000F4034	OSPI0_CSn2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		OSPI0_RESET_OUT1	2	O									
		GPIO0_13	7	IO	pad								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
L17	OSPI0_CSn3 PADCONFIG: PADCONFIG14 0x000F4038	OSPI0_CSn3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		OSPI0_RESET_OUT0	1	O									
		OSPI0_ECC_FAIL	2	I	1								
		GPIO0_14	7	IO	pad								
M19	OSPI0_D0 PADCONFIG: PADCONFIG3 0x000F400C	OSPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_3	7	IO	pad								
M18	OSPI0_D1 PADCONFIG: PADCONFIG4 0x000F4010	OSPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_4	7	IO	pad								
M20	OSPI0_D2 PADCONFIG: PADCONFIG5 0x000F4014	OSPI0_D2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_5	7	IO	pad								
M21	OSPI0_D3 PADCONFIG: PADCONFIG6 0x000F4018	OSPI0_D3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_6	7	IO	pad								
P21	OSPI0_D4 PADCONFIG: PADCONFIG7 0x000F401C	OSPI0_D4	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_7	7	IO	pad								
P20	OSPI0_D5 PADCONFIG: PADCONFIG8 0x000F4020	OSPI0_D5	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_8	7	IO	pad								
N18	OSPI0_D6 PADCONFIG: PADCONFIG9 0x000F4024	OSPI0_D6	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_9	7	IO	pad								
M17	OSPI0_D7 PADCONFIG: PADCONFIG10 0x000F4028	OSPI0_D7	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_10	7	IO	pad								
E17	PORz_OUT PADCONFIG: PADCONFIG171 0x000F42AC	PORz_OUT	0	O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
P3	PRG0_MDIO0_MDC PADCONFIG: PADCONFIG129 0x000F4204	PRG0_MDIO0_MDC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO1_41	7	IO	pad								
		GPMC0_A13	9	OZ									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
P2	PRG0_MDIO0_MDIO PADCONFIG: PADCONFIG128 0x000F4200	PRG0_MDIO0_MDIO	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO1_40	7	IO	pad								
		GPMC0_A12	9	OZ									
Y1	PRG0_PRU0_GPO0 PADCONFIG: PADCONFIG88 0x000F4160	PRG0_PRU0_GPO0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI0	1	I	0								
		PRG0_RGMII1_RD0	2	I	0								
		PRG0_PWM3_A0	3	IO	0								
		GPIO1_0	7	IO	pad								
		UART2_CTSn	10	I	1								
R4	PRG0_PRU0_GPO1 PADCONFIG: PADCONFIG89 0x000F4164	PRG0_PRU0_GPO1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI1	1	I	0								
		PRG0_RGMII1_RD1	2	I	0								
		PRG0_PWM3_B0	3	IO	1								
		GPIO1_1	7	IO	pad								
		UART2_TXD	10	O									
U2	PRG0_PRU0_GPO2 PADCONFIG: PADCONFIG90 0x000F4168	PRG0_PRU0_GPO2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI2	1	I	0								
		PRG0_RGMII1_RD2	2	I	0								
		PRG0_PWM2_A0	3	IO	0								
		GPIO1_2	7	IO	pad								
		GPMC0_A0	9	OZ									
		UART2_RTSn	10	O									
V2	PRG0_PRU0_GPO3 PADCONFIG: PADCONFIG91 0x000F416C	PRG0_PRU0_GPO3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI3	1	I	0								
		PRG0_RGMII1_RD3	2	I	0								
		PRG0_PWM3_A2	3	IO	0								
		GPIO1_3	7	IO	pad								
		UART3_CTSn	10	I	1								
AA2	PRG0_PRU0_GPO4 PADCONFIG: PADCONFIG92 0x000F4170	PRG0_PRU0_GPO4	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI4	1	I	0								
		PRG0_RGMII1_RX_CTL	2	I	0								
		PRG0_PWM2_B0	3	IO	1								
		GPIO1_4	7	IO	pad								
		GPMC0_A1	9	OZ									
		UART3_TXD	10	O									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
R3	PRG0_PRU0_GPO5 PADCONFIG: PADCONFIG93 0x000F4174	PRG0_PRU0_GPO5	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI5	1	I	0								
		PRG0_PWM3_B2	3	IO	1								
		GPIO1_5	7	IO	pad								
		UART3_RTSn	10	O									
T3	PRG0_PRU0_GPO6 PADCONFIG: PADCONFIG94 0x000F4178	PRG0_PRU0_GPO6	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI6	1	I	0								
		PRG0_RGMII1_RXC	2	I	0								
		PRG0_PWM3_A1	3	IO	0								
		GPIO1_6	7	IO	pad								
		UART4_CTSn	10	I	1								
T1	PRG0_PRU0_GPO7 PADCONFIG: PADCONFIG95 0x000F417C	PRG0_PRU0_GPO7	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI7	1	I	0								
		PRG0_IEP0_EDC_LATCH_IN1	2	I	0								
		PRG0_PWM3_B1	3	IO	1								
		CPTS0_HW2TSPUSH	4	I	0								
		CP_GEMAC_CPTS0_HW2TSPUSH	5	I	0								
		TIMER_IO6	6	IO	0								
		GPIO1_7	7	IO	pad								
		UART4_TXD	10	O									
T2	PRG0_PRU0_GPO8 PADCONFIG: PADCONFIG96 0x000F4180	PRG0_PRU0_GPO8	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI8	1	I	0								
		PRG0_PWM2_A1	3	IO	0								
		GPIO1_8	7	IO	pad								
		GPMC0_A2	9	OZ									
		UART4_RTSn	10	O									
W6	PRG0_PRU0_GPO9 PADCONFIG: PADCONFIG97 0x000F4184	PRG0_PRU0_GPO9	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI9	1	I	0								
		PRG0_UART0_CTSn	2	I	1								
		PRG0_PWM3_TZ_IN	3	I	0								
		RGMII1_RX_CTL	4	I	0								
		RMII1_RX_ER	5	I	0								
		PRG0_IEP0_EDIO_DATA_IN_OUT28	6	IO	0								
		GPIO1_9	7	IO	pad								
		UART2_RXD	10	I	1								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AA5	PRG0_PRU0_GPO10 PADCONFIG: PADCONFIG98 0x000F4188	PRG0_PRU0_GPO10	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI10	1	I	0								
		PRG0_UART0_RTSn	2	O									
		PRG0_PWM2_B1	3	IO	1								
		RGMII1_RXC	4	I	0								
		RMII_REF_CLK	5	I	0								
		PRG0_IEP0_EDIO_DATA_IN_OUT29	6	IO	0								
		GPIO1_10	7	IO	pad								
		UART3_RXD	10	I	1								
Y3	PRG0_PRU0_GPO11 PADCONFIG: PADCONFIG99 0x000F418C	PRG0_PRU0_GPO11	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI11	1	I	0								
		PRG0_RGMII1_TD0	2	O									
		PRG0_PWM3_TZ_OUT	3	O									
		GPIO1_11	7	IO	pad								
		UART4_RXD	10	I	1								
AA3	PRG0_PRU0_GPO12 PADCONFIG: PADCONFIG100 0x000F4190	PRG0_PRU0_GPO12	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI12	1	I	0								
		PRG0_RGMII1_TD1	2	O									
		PRG0_PWM0_A0	3	IO	0								
		GPIO1_12	7	IO	pad								
		GPMC0_A14	9	OZ									
R6	PRG0_PRU0_GPO13 PADCONFIG: PADCONFIG101 0x000F4194	PRG0_PRU0_GPO13	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI13	1	I	0								
		PRG0_RGMII1_TD2	2	O									
		PRG0_PWM0_B0	3	IO	1								
		SPI3_D0	6	IO	0								
		GPIO1_13	7	IO	pad								
		GPMC0_A15	9	OZ									
V4	PRG0_PRU0_GPO14 PADCONFIG: PADCONFIG102 0x000F4198	PRG0_PRU0_GPO14	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI14	1	I	0								
		PRG0_RGMII1_TD3	2	O									
		PRG0_PWM0_A1	3	IO	0								
		SPI3_D1	6	IO	0								
		GPIO1_14	7	IO	pad								
		GPMC0_A3	9	OZ									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
T5	PRG0_PRU0_GPO15 PADCONFIG: PADCONFIG103 0x000F419C	PRG0_PRU0_GPO15	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI15	1	I	0								
		PRG0_RGMII1_TX_CTL	2	O									
		PRG0_PWM0_B1	3	IO	1								
		SPI3_CS1	6	IO	1								
		GPIO1_15	7	IO	pad								
		GPMC0_A16	9	OZ									
U4	PRG0_PRU0_GPO16 PADCONFIG: PADCONFIG104 0x000F41A0	PRG0_PRU0_GPO16	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI16	1	I	0								
		PRG0_RGMII1_TXC	2	IO	0								
		PRG0_PWM0_A2	3	IO	0								
		SPI3_CLK	6	IO	0								
		GPIO1_16	7	IO	pad								
		GPMC0_A4	9	OZ									
U1	PRG0_PRU0_GPO17 PADCONFIG: PADCONFIG105 0x000F41A4	PRG0_PRU0_GPO17	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI17	1	I	0								
		PRG0_IEP0_EDC_SYNC_OUT1	2	O									
		PRG0_PWM0_B2	3	IO	1								
		CPTS0_TS_SYNC	4	O									
		CP_GEMAC_CPTS0_TS_SYNC	5	O									
		SPI3_CS0	6	IO	1								
		GPIO1_17	7	IO	pad								
		TIMER_IO11	8	IO	0								
		GPMC0_A17	9	OZ									
V1	PRG0_PRU0_GPO18 PADCONFIG: PADCONFIG106 0x000F41A8	PRG0_PRU0_GPO18	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI18	1	I	0								
		PRG0_IEP0_EDC_LATCH_IN0	2	I	0								
		PRG0_PWM0_TZ_IN	3	I	0								
		CPTS0_HW1TSPUSH	4	I	0								
		CP_GEMAC_CPTS0_HW1TSPUSH	5	I	0								
		EHRPWM8_A	6	IO	0								
		GPIO1_18	7	IO	pad								
		UART4_CTSn	8	I	1								
		GPMC0_A5	9	OZ									
		UART2_RXD	10	I	1								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
W1	PRG0_PRU0_GPO19 PADCONFIG: PADCONFIG107 0x000F41AC	PRG0_PRU0_GPO19	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI19	1	I	0								
		PRG0_IEP0_EDC_SYNC_OUT0	2	O									
		PRG0_PWM0_TZ_OUT	3	O									
		CPTS0_TS_COMP	4	O									
		CP_GEMAC_CPTS0_TS_COMP	5	O									
		EHRPWM8_B	6	IO	0								
		GPIO1_19	7	IO	pad								
		UART4_RTSn	8	O									
		GPMC0_A6	9	OZ									
		UART3_RXD	10	I	1								
Y2	PRG0_PRU1_GPO0 PADCONFIG: PADCONFIG108 0x000F41B0	PRG0_PRU1_GPO0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI0	1	I	0								
		PRG0_RGMII2_RD0	2	I	0								
		GPIO1_20	7	IO	pad								
		EQEP0_A	8	I	0								
		UART5_CTSn	10	I	1								
W2	PRG0_PRU1_GPO1 PADCONFIG: PADCONFIG109 0x000F41B4	PRG0_PRU1_GPO1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI1	1	I	0								
		PRG0_RGMII2_RD1	2	I	0								
		GPIO1_21	7	IO	pad								
		EQEP0_B	8	I	0								
		UART5_TXD	10	O									
V3	PRG0_PRU1_GPO2 PADCONFIG: PADCONFIG110 0x000F41B8	PRG0_PRU1_GPO2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI2	1	I	0								
		PRG0_RGMII2_RD2	2	I	0								
		PRG0_PWM2_A2	3	IO	0								
		GPIO1_22	7	IO	pad								
		EQEP0_S	8	IO	0								
		UART5_RTSn	10	O									
T4	PRG0_PRU1_GPO3 PADCONFIG: PADCONFIG111 0x000F41BC	PRG0_PRU1_GPO3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI3	1	I	0								
		PRG0_RGMII2_RD3	2	I	0								
		GPIO1_23	7	IO	pad								
		EQEP1_A	8	I	0								
		GPMC0_A18	9	OZ									
		UART6_CTSn	10	I	1								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
W3	PRG0_PRU1_GPO4 PADCONFIG: PADCONFIG112 0x000F41C0	PRG0_PRU1_GPO4	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI4	1	I	0								
		PRG0_RGMII2_RX_CTL	2	I	0								
		PRG0_PWM2_B2	3	IO	1								
		GPIO1_24	7	IO	pad								
		EQEP1_B	8	I	0								
		UART6_TXD	10	O									
P4	PRG0_PRU1_GPO5 PADCONFIG: PADCONFIG113 0x000F41C4	PRG0_PRU1_GPO5	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI5	1	I	0								
		GPIO1_25	7	IO	pad								
		EQEP1_S	8	IO	0								
		UART6_RTSn	10	O									
R5	PRG0_PRU1_GPO6 PADCONFIG: PADCONFIG114 0x000F41C8	PRG0_PRU1_GPO6	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI6	1	I	0								
		PRG0_RGMII2_RXC	2	I	0								
		GPIO1_26	7	IO	pad								
		EQEP2_A	8	I	0								
		GPMC0_A19	9	OZ									
		UART4_CTSn	10	I	1								
W5	PRG0_PRU1_GPO7 PADCONFIG: PADCONFIG115 0x000F41CC	PRG0_PRU1_GPO7	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI7	1	I	0								
		PRG0_IEP1_EDC_LATCH_IN1	2	I	0								
		RGMII1_RD0	4	I	0								
		RMII1_RXD0	5	I	0								
		GPIO1_27	7	IO	pad								
		EQEP2_B	8	I	0								
		UART4_TXD	10	O									
R1	PRG0_PRU1_GPO8 PADCONFIG: PADCONFIG116 0x000F41D0	PRG0_PRU1_GPO8	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI8	1	I	0								
		PRG0_PWM2_TZ_OUT	3	O									
		GPIO1_28	7	IO	pad								
		EQEP2_S	8	IO	0								
		UART4_RTSn	10	O									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
Y5	PRG0_PRU1_GPO9 PADCONFIG: PADCONFIG117 0x000F41D4	PRG0_PRU1_GPO9	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI9	1	I	0								
		PRG0_UART0_RXD	2	I	1								
		RGMII1_RD1	4	I	0								
		RMII1_RXD1	5	I	0								
		PRG0_IEP0_EDIO_DATA_IN_OUT30	6	IO	0								
		GPIO1_29	7	IO	pad								
		EQEP0_I	8	IO	0								
		UART5_RXD	10	I	1								
V6	PRG0_PRU1_GPO10 PADCONFIG: PADCONFIG118 0x000F41D8	PRG0_PRU1_GPO10	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI10	1	I	0								
		PRG0_UART0_TXD	2	O									
		PRG0_PWM2_TZ_IN	3	I	0								
		RGMII1_RD2	4	I	0								
		RMII1_TXD0	5	O									
		PRG0_IEP0_EDIO_DATA_IN_OUT31	6	IO	0								
		GPIO1_30	7	IO	pad								
		EQEP1_I	8	IO	0								
		UART6_RXD	10	I	1								
W4	PRG0_PRU1_GPO11 PADCONFIG: PADCONFIG119 0x000F41DC	PRG0_PRU1_GPO11	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI11	1	I	0								
		PRG0_RGMII2_TD0	2	O									
		GPIO1_31	7	IO	pad								
		EQEP2_I	8	IO	0								
		UART4_RXD	10	I	1								
Y4	PRG0_PRU1_GPO12 PADCONFIG: PADCONFIG120 0x000F41E0	PRG0_PRU1_GPO12	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI12	1	I	0								
		PRG0_RGMII2_TD1	2	O									
		PRG0_PWM1_A0	3	IO	0								
		GPIO1_32	7	IO	pad								
		EQEP2_B	8	I	0								
		GPMC0_A7	9	OZ									
		UART4_TXD	10	O									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
T6	PRG0_PRU1_GPO13 PADCONFIG: PADCONFIG121 0x000F41E4	PRG0_PRU1_GPO13	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI13	1	I	0								
		PRG0_RGMII2_TD2	2	O									
		PRG0_PWM1_B0	3	IO	1								
		GPIO1_33	7	IO	pad								
		EQEP0_I	8	IO	0								
		GPMC0_A8	9	OZ									
		UART5_RXD	10	I	1								
U6	PRG0_PRU1_GPO14 PADCONFIG: PADCONFIG122 0x000F41E8	PRG0_PRU1_GPO14	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI14	1	I	0								
		PRG0_RGMII2_TD3	2	O									
		PRG0_PWM1_A1	3	IO	0								
		GPIO1_34	7	IO	pad								
		EQEP1_I	8	IO	0								
		GPMC0_A9	9	OZ									
		UART6_RXD	10	I	1								
U5	PRG0_PRU1_GPO15 PADCONFIG: PADCONFIG123 0x000F41EC	PRG0_PRU1_GPO15	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI15	1	I	0								
		PRG0_RGMII2_TX_CTL	2	O									
		PRG0_PWM1_B1	3	IO	1								
		GPIO1_35	7	IO	pad								
		GPMC0_A10	9	OZ									
		PRG0_ECAP0_IN_APWM_OUT	10	IO	0								
AA4	PRG0_PRU1_GPO16 PADCONFIG: PADCONFIG124 0x000F41F0	PRG0_PRU1_GPO16	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI16	1	I	0								
		PRG0_RGMII2_TXC	2	IO	0								
		PRG0_PWM1_A2	3	IO	0								
		GPIO1_36	7	IO	pad								
		GPMC0_A11	9	OZ									
		PRG0_ECAP0_SYNC_OUT	10	O									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
V5	PRG0_PRU1_GPO17 PADCONFIG: PADCONFIG125 0x000F41F4	PRG0_PRU1_GPO17	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI17	1	I	0								
		PRG0_IEP1_EDC_SYNC_OUT1	2	O									
		PRG0_PWM1_B2	3	IO	1								
		RGMII1_RD3	4	I	0								
		RMII1_TXD1	5	O									
		GPIO1_37	7	IO	pad								
		PRG0_ECAP0_SYNC_OUT	8	O									
		PRG0_ECAP0_SYNC_IN	10	I	0								
P5	PRG0_PRU1_GPO18 PADCONFIG: PADCONFIG126 0x000F41F8	PRG0_PRU1_GPO18	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI18	1	I	0								
		PRG0_IEP1_EDC_LATCH_IN0	2	I	0								
		PRG0_PWM1_TZ_IN	3	I	0								
		MDIO0_MDIO	4	IO	0								
		RMII1_TX_EN	5	O									
		EHRPWM7_A	6	IO	0								
		GPIO1_38	7	IO	pad								
		PRG0_ECAP0_SYNC_IN	8	I	0								
R2	PRG0_PRU1_GPO19 PADCONFIG: PADCONFIG127 0x000F41FC	PRG0_PRU1_GPO19	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI19	1	I	0								
		PRG0_IEP1_EDC_SYNC_OUT0	2	O									
		PRG0_PWM1_TZ_OUT	3	O									
		MDIO0_MDC	4	O									
		RMII1_CRS_DV	5	I	0								
		EHRPWM7_B	6	IO	0								
		GPIO1_39	7	IO	pad								
		PRG0_ECAP0_IN_APWM_OUT	8	IO	0								
Y6	PRG1_MDIO0_MDC PADCONFIG: PADCONFIG87 0x000F415C	PRG1_MDIO0_MDC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MDIO0_MDC	4	O									
		GPIO0_86	7	IO	pad								
AA6	PRG1_MDIO0_MDIO PADCONFIG: PADCONFIG86 0x000F4158	PRG1_MDIO0_MDIO	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MDIO0_MDIO	4	IO	0								
		GPIO0_85	7	IO	pad								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
Y7	PRG1_PRU0_GPO0 PADCONFIG: PADCONFIG46 0x000F40B8	PRG1_PRU0_GPO0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI0	1	I	0								
		PRG1_RGMII1_RD0	2	I	0								
		PRG1_PWM3_A0	3	IO	0								
		GPIO0_45	7	IO	pad								
		GPMC0_AD16	8	IO	0								
U8	PRG1_PRU0_GPO1 PADCONFIG: PADCONFIG47 0x000F40BC	PRG1_PRU0_GPO1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI1	1	I	0								
		PRG1_RGMII1_RD1	2	I	0								
		PRG1_PWM3_B0	3	IO	1								
		GPIO0_46	7	IO	pad								
		GPMC0_AD17	8	IO	0								
W8	PRG1_PRU0_GPO2 PADCONFIG: PADCONFIG48 0x000F40C0	PRG1_PRU0_GPO2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI2	1	I	0								
		PRG1_RGMII1_RD2	2	I	0								
		PRG1_PWM2_A0	3	IO	0								
		GPIO0_47	7	IO	pad								
		GPMC0_AD18	8	IO	0								
V8	PRG1_PRU0_GPO3 PADCONFIG: PADCONFIG49 0x000F40C4	PRG1_PRU0_GPO3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI3	1	I	0								
		PRG1_RGMII1_RD3	2	I	0								
		PRG1_PWM3_A2	3	IO	0								
		GPIO0_48	7	IO	pad								
		GPMC0_AD19	8	IO	0								
Y8	PRG1_PRU0_GPO4 PADCONFIG: PADCONFIG50 0x000F40C8	PRG1_PRU0_GPO4	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI4	1	I	0								
		PRG1_RGMII1_RX_CTL	2	I	0								
		PRG1_PWM2_B0	3	IO	1								
		GPIO0_49	7	IO	pad								
		GPMC0_AD20	8	IO	0								
V13	PRG1_PRU0_GPO5 PADCONFIG: PADCONFIG51 0x000F40CC	PRG1_PRU0_GPO5	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI5	1	I	0								
		PRG1_PWM3_B2	3	IO	1								
		RGMII1_RX_CTL	4	I	0								
		GPIO0_50	7	IO	pad								
		GPMC0_AD21	8	IO	0								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AA7	PRG1_PRU0_GPO6 PADCONFIG: PADCONFIG52 0x000F40D0	PRG1_PRU0_GPO6	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI6	1	I	0								
		PRG1_RGMII1_RXC	2	I	0								
		PRG1_PWM3_A1	3	IO	0								
		GPIO0_51	7	IO	pad								
		GPMC0_AD22	8	IO	0								
U13	PRG1_PRU0_GPO7 PADCONFIG: PADCONFIG53 0x000F40D4	PRG1_PRU0_GPO7	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI7	1	I	0								
		PRG1_IEP0_EDC_LATCH_IN1	2	I	0								
		PRG1_PWM3_B1	3	IO	1								
		CPTS0_HW2TSPUSH	4	I	0								
		CLKOUT0	5	O									
		TIMER_IO10	6	IO	0								
		GPIO0_52	7	IO	pad								
		GPMC0_AD23	8	IO	0								
W13	PRG1_PRU0_GPO8 PADCONFIG: PADCONFIG54 0x000F40D8	PRG1_PRU0_GPO8	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI8	1	I	0								
		PRG1_PWM2_A1	3	IO	0								
		RGMII1_RXC	4	I	0								
		GPIO0_53	7	IO	pad								
		GPMC0_AD24	8	IO	0								
U15	PRG1_PRU0_GPO9 PADCONFIG: PADCONFIG55 0x000F40DC	PRG1_PRU0_GPO9	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI9	1	I	0								
		PRG1_UART0_CTSn	2	I	1								
		PRG1_PWM3_TZ_IN	3	I	0								
		RGMII1_TX_CTL	4	O									
		RMII1_RX_ER	5	I	0								
		PRG1_IEP0_EDIO_DATA_IN_OUT28	6	IO	0								
		GPIO0_54	7	IO	pad								
		GPMC0_AD25	8	IO	0								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
U14	PRG1_PRU0_GPO10 PADCONFIG: PADCONFIG56 0x000F40E0	PRG1_PRU0_GPO10	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI10	1	I	0								
		PRG1_UART0_RTSn	2	O									
		PRG1_PWM2_B1	3	IO	1								
		RGMII1_TXC	4	IO	0								
		RMII_REF_CLK	5	I	0								
		PRG1_IEP0_EDIO_DATA_IN_OUT29	6	IO	0								
		GPIO0_55	7	IO	pad								
		GPMC0_AD26	8	IO	0								
AA8	PRG1_PRU0_GPO11 PADCONFIG: PADCONFIG57 0x000F40E4	PRG1_PRU0_GPO11	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI11	1	I	0								
		PRG1_RGMII1_TD0	2	O									
		PRG1_PWM3_TZ_OUT	3	O									
		GPIO0_56	7	IO	pad								
		GPMC0_AD27	8	IO	0								
U9	PRG1_PRU0_GPO12 PADCONFIG: PADCONFIG58 0x000F40E8	PRG1_PRU0_GPO12	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI12	1	I	0								
		PRG1_RGMII1_TD1	2	O									
		PRG1_PWM0_A0	3	IO	0								
		GPIO0_57	7	IO	pad								
		GPMC0_AD28	8	IO	0								
W9	PRG1_PRU0_GPO13 PADCONFIG: PADCONFIG59 0x000F40EC	PRG1_PRU0_GPO13	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI13	1	I	0								
		PRG1_RGMII1_TD2	2	O									
		PRG1_PWM0_B0	3	IO	1								
		GPIO0_58	7	IO	pad								
		GPMC0_AD29	8	IO	0								
AA9	PRG1_PRU0_GPO14 PADCONFIG: PADCONFIG60 0x000F40F0	PRG1_PRU0_GPO14	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI14	1	I	0								
		PRG1_RGMII1_TD3	2	O									
		PRG1_PWM0_A1	3	IO	0								
		GPIO0_59	7	IO	pad								
		GPMC0_AD30	8	IO	0								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
Y9	PRG1_PRU0_GPO15 PADCONFIG: PADCONFIG61 0x000F40F4	PRG1_PRU0_GPO15	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI15	1	I	0								
		PRG1_RGMII1_TX_CTL	2	O									
		PRG1_PWM0_B1	3	IO	1								
		GPIO0_60	7	IO	pad								
		GPMC0_AD31	8	IO	0								
V9	PRG1_PRU0_GPO16 PADCONFIG: PADCONFIG62 0x000F40F8	PRG1_PRU0_GPO16	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI16	1	I	0								
		PRG1_RGMII1_TXC	2	IO	0								
		PRG1_PWM0_A2	3	IO	0								
		GPIO0_61	7	IO	pad								
		GPMC0_BE2n	8	O									
U7	PRG1_PRU0_GPO17 PADCONFIG: PADCONFIG63 0x000F40FC	PRG1_PRU0_GPO17	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI17	1	I	0								
		PRG1_IEP0_EDC_SYNC_OUT1	2	O									
		PRG1_PWM0_B2	3	IO	1								
		CPTS0_TS_SYNC	4	O									
		TIMER_IO7	6	IO	0								
		GPIO0_62	7	IO	pad								
		GPMC0_A0	8	OZ									
V7	PRG1_PRU0_GPO18 PADCONFIG: PADCONFIG64 0x000F4100	PRG1_PRU0_GPO18	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI18	1	I	0								
		PRG1_IEP0_EDC_LATCH_IN0	2	I	0								
		PRG1_PWM0_TZ_IN	3	I	0								
		CPTS0_HW1TSPUSH	4	I	0								
		TIMER_IO8	6	IO	0								
		GPIO0_63	7	IO	pad								
		GPMC0_A1	8	OZ									
W7	PRG1_PRU0_GPO19 PADCONFIG: PADCONFIG65 0x000F4104	PRG1_PRU0_GPO19	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI19	1	I	0								
		PRG1_IEP0_EDC_SYNC_OUT0	2	O									
		PRG1_PWM0_TZ_OUT	3	O									
		CPTS0_TS_COMP	4	O									
		TIMER_IO9	6	IO	0								
		GPIO0_64	7	IO	pad								
		GPMC0_A2	8	OZ									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
W11	PRG1_PRU1_GPO0 PADCONFIG: PADCONFIG66 0x000F4108	PRG1_PRU1_GPO0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI0	1	I	0								
		PRG1_RGMII2_RD0	2	I	0								
		RGMII2_RD0	4	I	0								
		RMII2_RXD0	5	I	0								
		GPIO0_65	7	IO	pad								
		GPMC0_A3	8	OZ									
V11	PRG1_PRU1_GPO1 PADCONFIG: PADCONFIG67 0x000F410C	PRG1_PRU1_GPO1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI1	1	I	0								
		PRG1_RGMII2_RD1	2	I	0								
		RGMII2_RD1	4	I	0								
		RMII2_RXD1	5	I	0								
		GPIO0_66	7	IO	pad								
		GPMC0_A4	8	OZ									
AA12	PRG1_PRU1_GPO2 PADCONFIG: PADCONFIG68 0x000F4110	PRG1_PRU1_GPO2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI2	1	I	0								
		PRG1_RGMII2_RD2	2	I	0								
		PRG1_PWM2_A2	3	IO	0								
		RGMII2_RD2	4	I	0								
		GPIO0_67	7	IO	pad								
		GPMC0_A5	8	OZ									
Y12	PRG1_PRU1_GPO3 PADCONFIG: PADCONFIG69 0x000F4114	PRG1_PRU1_GPO3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI3	1	I	0								
		PRG1_RGMII2_RD3	2	I	0								
		RGMII2_RD3	4	I	0								
		GPIO0_68	7	IO	pad								
		GPMC0_A6	8	OZ									
W12	PRG1_PRU1_GPO4 PADCONFIG: PADCONFIG70 0x000F4118	PRG1_PRU1_GPO4	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI4	1	I	0								
		PRG1_RGMII2_RX_CTL	2	I	0								
		PRG1_PWM2_B2	3	IO	1								
		RGMII2_RX_CTL	4	I	0								
		RMII2_RX_ER	5	I	0								
		GPIO0_69	7	IO	pad								
		GPMC0_A7	8	OZ									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AA13	PRG1_PRU1_GPO5 PADCONFIG: PADCONFIG71 0x000F411C	PRG1_PRU1_GPO5	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI5	1	I	0								
		RGMII1_RD0	4	I	0								
		GPIO0_70	7	IO	pad								
		GPMC0_A8	8	OZ									
U11	PRG1_PRU1_GPO6 PADCONFIG: PADCONFIG72 0x000F4120	PRG1_PRU1_GPO6	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI6	1	I	0								
		PRG1_RGMII2_RXC	2	I	0								
		RGMII2_RXC	4	I	0								
		GPIO0_71	7	IO	pad								
		GPMC0_A9	8	OZ									
V15	PRG1_PRU1_GPO7 PADCONFIG: PADCONFIG73 0x000F4124	PRG1_PRU1_GPO7	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI7	1	I	0								
		PRG1_IEP1_EDC_LATCH_IN1	2	I	0								
		RGMII1_TD0	4	O									
		RMII1_RXD0	5	I	0								
		SPI3_CS3	6	IO	1								
		GPIO0_72	7	IO	pad								
		GPMC0_A10	8	OZ									
U12	PRG1_PRU1_GPO8 PADCONFIG: PADCONFIG74 0x000F4128	PRG1_PRU1_GPO8	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI8	1	I	0								
		PRG1_PWM2_TZ_OUT	3	O									
		RGMII1_RD1	4	I	0								
		GPIO0_73	7	IO	pad								
		GPMC0_A11	8	OZ									
V14	PRG1_PRU1_GPO9 PADCONFIG: PADCONFIG75 0x000F412C	PRG1_PRU1_GPO9	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI9	1	I	0								
		PRG1_UART0_RXD	2	I	1								
		RGMII1_TD1	4	O									
		RMII1_RXD1	5	I	0								
		PRG1_IEP0_EDIO_DATA_IN_OUT30	6	IO	0								
		GPIO0_74	7	IO	pad								
		GPMC0_A12	8	OZ									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
W14	PRG1_PRU1_GPO10 PADCONFIG: PADCONFIG76 0x000F4130	PRG1_PRU1_GPO10	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI10	1	I	0								
		PRG1_UART0_TXD	2	O									
		PRG1_PWM2_TZ_IN	3	I	0								
		RGMII1_TD2	4	O									
		RMII1_TXD0	5	O									
		PRG1_IEP0_EDIO_DATA_IN_OUT31	6	IO	0								
		GPIO0_75	7	IO	pad								
		GPMC0_A13	8	OZ									
AA10	PRG1_PRU1_GPO11 PADCONFIG: PADCONFIG77 0x000F4134	PRG1_PRU1_GPO11	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI11	1	I	0								
		PRG1_RGMII2_TD0	2	O									
		RGMII2_TD0	4	O									
		RMII2_TXD0	5	O									
		GPIO0_76	7	IO	pad								
		GPMC0_A14	8	OZ									
V10	PRG1_PRU1_GPO12 PADCONFIG: PADCONFIG78 0x000F4138	PRG1_PRU1_GPO12	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI12	1	I	0								
		PRG1_RGMII2_TD1	2	O									
		PRG1_PWM1_A0	3	IO	0								
		RGMII2_TD1	4	O									
		RMII2_TXD1	5	O									
		GPIO0_77	7	IO	pad								
		GPMC0_A15	8	OZ									
U10	PRG1_PRU1_GPO13 PADCONFIG: PADCONFIG79 0x000F413C	PRG1_PRU1_GPO13	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI13	1	I	0								
		PRG1_RGMII2_TD2	2	O									
		PRG1_PWM1_B0	3	IO	1								
		RGMII2_TD2	4	O									
		RMII2_CRS_DV	5	I	0								
		GPIO0_78	7	IO	pad								
		GPMC0_A16	8	OZ									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AA11	PRG1_PRU1_GPO14 PADCONFIG: PADCONFIG80 0x000F4140	PRG1_PRU1_GPO14	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI14	1	I	0								
		PRG1_RGMII2_TD3	2	O									
		PRG1_PWM1_A1	3	IO	0								
		RGMII2_TD3	4	O									
		GPIO0_79	7	IO	pad								
		GPMC0_A17	8	OZ									
Y11	PRG1_PRU1_GPO15 PADCONFIG: PADCONFIG81 0x000F4144	PRG1_PRU1_GPO15	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI15	1	I	0								
		PRG1_RGMII2_TX_CTL	2	O									
		PRG1_PWM1_B1	3	IO	1								
		RGMII2_TX_CTL	4	O									
		RMII2_TX_EN	5	O									
		GPIO0_80	7	IO	pad								
		GPMC0_A18	8	OZ									
Y10	PRG1_PRU1_GPO16 PADCONFIG: PADCONFIG82 0x000F4148	PRG1_PRU1_GPO16	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI16	1	I	0								
		PRG1_RGMII2_TXC	2	IO	0								
		PRG1_PWM1_A2	3	IO	0								
		RGMII2_TXC	4	IO	0								
		GPIO0_81	7	IO	pad								
		GPMC0_A19	8	OZ									
AA14	PRG1_PRU1_GPO17 PADCONFIG: PADCONFIG83 0x000F414C	PRG1_PRU1_GPO17	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI17	1	I	0								
		PRG1_IEP1_EDC_SYNC_OUT1	2	O									
		PRG1_PWM1_B2	3	IO	1								
		RGMII1_TD3	4	O									
		RMII1_TXD1	5	O									
		GPIO0_19	7	IO	pad								
		GPMC0_BE3n	8	O									
		PRG1_ECAP0_SYNC_OUT	9	O									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
Y13	PRG1_PRU1_GPO18 PADCONFIG: PADCONFIG84 0x000F4150	PRG1_PRU1_GPO18	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI18	1	I	0								
		PRG1_IEP1_EDC_LATCH_IN0	2	I	0								
		PRG1_PWM1_TZ_IN	3	I	0								
		RGMII1_RD2	4	I	0								
		RMII1_TX_EN	5	O									
		GPIO0_20	7	IO	pad								
		UART5_CTSn	8	I	1								
		PRG1_ECAP0_SYNC_IN	9	I	0								
V12	PRG1_PRU1_GPO19 PADCONFIG: PADCONFIG85 0x000F4154	PRG1_PRU1_GPO19	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI19	1	I	0								
		PRG1_IEP1_EDC_SYNC_OUT0	2	O									
		PRG1_PWM1_TZ_OUT	3	O									
		RGMII1_RD3	4	I	0								
		RMII1_CRS_DV	5	I	0								
		SPI3_CS2	6	IO	1								
		GPIO0_84	7	IO	pad								
		UART5_RTSn	8	O									
		PRG1_ECAP0_IN_APWM_OUT	9	IO	0								
F16	RESETSTATz PADCONFIG: PADCONFIG169 0x000F42A4	RESETSTATz	0	O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
E18	RESET_REQz PADCONFIG: PADCONFIG168 0x000F42A0	RESET_REQz	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
H16	RSVD0	RSVD0		N/A									
D21	RSVD1	RSVD1		N/A									
G13	RSVD2	RSVD2		N/A									
F17	RSVD3	RSVD3		N/A									
W15	RSVD4	RSVD4		N/A									
V16	RSVD5	RSVD5		N/A									
K2	RSVD6	RSVD6		N/A									
K1	RSVD7	RSVD7		N/A									
F12	RSVD8	RSVD8		N/A									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
T13	SERDES0_REXT	SERDES0_REXT		A					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES	
W16	SERDES0_REFCLK0N	SERDES0_REFCLK0N		IO					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES	
W17	SERDES0_REFCLK0P	SERDES0_REFCLK0P		IO					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES	
Y15	SERDES0_RX0_N	SERDES0_RX0_N		I					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES	
Y16	SERDES0_RX0_P	SERDES0_RX0_P		I					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES	
AA16	SERDES0_TX0_N	SERDES0_TX0_N		O					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES	
AA17	SERDES0_TX0_P	SERDES0_TX0_P		O					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES	
D13	SPI0_CLK PADCONFIG: PADCONFIG132 0x000F4210	SPI0_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		GPIO1_44	7	IO	pad								
C14	SPI1_CLK PADCONFIG: PADCONFIG137 0x000F4224	SPI1_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		EHRPWM6_SYNCI	3	I	0								
		GPIO1_49	7	IO	pad								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
D12	SPI0_CS0 PADCONFIG: PADCONFIG130 0x000F4208	SPI0_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		GPIO1_42	7	IO	pad								
C13	SPI0_CS1 PADCONFIG: PADCONFIG131 0x000F420C	SPI0_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CPTS0_TS_COMP	1	O									
		I2C2_SCL	2	IOD	1								
		TIMER_IO10	3	IO	0								
		PRG0_IEP0_EDIO_OUTVALID	4	O									
		UART6_RXD	5	I	1								
		ADC_EXT_TRIGGER0	6	I	0								
		GPIO1_43	7	IO	pad								
A13	SPI0_D0 PADCONFIG: PADCONFIG133 0x000F4214	SPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		GPIO1_45	7	IO	pad								
A14	SPI0_D1 PADCONFIG: PADCONFIG134 0x000F4218	SPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		GPIO1_46	7	IO	pad								
B14	SPI1_CS0 PADCONFIG: PADCONFIG135 0x000F421C	SPI1_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		EHRPWM6_A	3	IO	0								
		GPIO1_47	7	IO	pad								
D14	SPI1_CS1 PADCONFIG: PADCONFIG136 0x000F4220	SPI1_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CPTS0_TS_SYNC	1	O									
		I2C2_SDA	2	IOD	1								
		PRG1_IEP0_EDIO_OUTVALID	4	O									
		UART6_TXD	5	O									
		ADC_EXT_TRIGGER1	6	I	0								
		GPIO1_48	7	IO	pad								
		TIMER_IO11	8	IO	0								
B15	SPI1_D0 PADCONFIG: PADCONFIG138 0x000F4228	SPI1_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		EHRPWM6_SYNCO	3	O									
		GPIO1_50	7	IO	pad								
A15	SPI1_D1 PADCONFIG: PADCONFIG139 0x000F422C	SPI1_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		EHRPWM6_B	3	IO	0								
		GPIO1_51	7	IO	pad								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
B11	TCK PADCONFIG: MCU_PADCONFIG26 0x04084068	TCK	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
C11	TDI PADCONFIG: MCU_PADCONFIG28 0x04084070	TDI	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
A12	TDO PADCONFIG: MCU_PADCONFIG29 0x04084074	TDO	0	OZ		Off / Off / Up	Off / SS / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
C12	TMS PADCONFIG: MCU_PADCONFIG30 0x04084078	TMS	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
D11	TRSTn PADCONFIG: MCU_PADCONFIG27 0x0408406C	TRSTn	0	I		On / Off / Down	On / Off / Down	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
B16	UART0_CTSn PADCONFIG: PADCONFIG142 0x000F4238	UART0_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI0_CS2	1	IO	1								
		ADC_EXT_TRIGGER0	2	I	0								
		UART2_RXD	3	I	1								
		TIMER_IO6	4	IO	0								
		SPI4_CLK	6	IO	0								
		GPIO1_54	7	IO	pad								
		EQEP0_S	8	IO	0								
		CP_GEMAC_CPTS0_TS_SYNC	9	O									
A16	UART0_RTSn PADCONFIG: PADCONFIG143 0x000F423C	UART0_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI0_CS3	1	IO	1								
		UART2_TXD	3	O									
		TIMER_IO7	4	IO	0								
		SPI4_D0	6	IO	0								
		GPIO1_55	7	IO	pad								
		EQEP0_I	8	IO	0								
D15	UART0_RXD PADCONFIG: PADCONFIG140 0x000F4230	UART0_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_D0	2	IO	0								
		GPIO1_52	7	IO	pad								
		EQEP0_A	8	I	0								

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
C16	UART0_TXD PADCONFIG: PADCONFIG141 0x000F4234	UART0_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_D1	2	IO	0								
		GPIO1_53	7	IO	pad								
		EQEP0_B	8	I	0								
D16	UART1_CTSn PADCONFIG: PADCONFIG146 0x000F4248	UART1_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI1_CS2	1	IO	1								
		ADC_EXT_TRIGGER1	2	I	0								
		PCIE0_CLKREQn	3	IO	0								
		UART3_RXD	4	I	1								
		CP_GEMAC_CPTS0_TS_SYNC	5	O									
		SPI4_D1	6	IO	0								
		GPIO1_58	7	IO	pad								
		EQEP1_S	8	IO	0								
E16	UART1_RTSn PADCONFIG: PADCONFIG147 0x000F424C	UART1_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI1_CS3	1	IO	1								
		UART3_TXD	4	O									
		CP_GEMAC_CPTS0_HW2TSPUSH	5	I	0								
		SPI4_CS0	6	IO	1								
		GPIO1_59	7	IO	pad								
		EQEP1_I	8	IO	0								
E15	UART1_RXD PADCONFIG: PADCONFIG144 0x000F4240	UART1_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CS0	2	IO	1								
		CP_GEMAC_CPTS0_TS_COMP	5	O									
		GPIO1_56	7	IO	pad								
		EQEP1_A	8	I	0								
E14	UART1_TXD PADCONFIG: PADCONFIG145 0x000F4244	UART1_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CLK	2	IO	0								
		CP_GEMAC_CPTS0_HW1TSPUSH	5	I	0								
		GPIO1_57	7	IO	pad								
		EQEP1_B	8	I	0								
AA20	USB0_DM	USB0_DM		IO					1.8 V/3.3 V	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0		USB2PHY	
AA19	USB0_DP	USB0_DP		IO					1.8 V/3.3 V	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0		USB2PHY	

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
E19	USB0_DRVVBUS	USB0_DRVVBUS	0	O		Off / Off / Down	Off / Off / Down	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
	PADCONFIG: PADCONFIG170 0x000F42A8	GPIO1_79	7	IO	pad								
U16	USB0_ID	USB0_ID		A					1.8 V/3.3 V	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0		USB2PHY	
U17	USB0_RCALIB	USB0_RCALIB		A					1.8 V/3.3 V	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0		USB2PHY	
T14	USB0_VBUS	USB0_VBUS		A					1.8 V/3.3 V	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0		USB2PHY	
P12, P13	VDDA_0P85_SERDES0	VDDA_0P85_SERDES0		PWR									
P11	VDDA_0P85_SERDES0_C	VDDA_0P85_SERDES0_C		PWR									
T12	VDDA_0P85_USB0	VDDA_0P85_USB0		PWR									
R14	VDDA_1P8_SERDES0	VDDA_1P8_SERDES0		PWR									
R15	VDDA_1P8_USB0	VDDA_1P8_USB0		PWR									
H15	VDDA_3P3_SDIO	VDDA_3P3_SDIO		PWR									
R13	VDDA_3P3_USB0	VDDA_3P3_USB0		PWR									
J13	VDDA_ADC	VDDA_ADC		PWR									
K12	VDDA_MCU	VDDA_MCU		PWR									
N12	VDDA_PLL0	VDDA_PLL0		PWR									
H9	VDDA_PLL1	VDDA_PLL1		PWR									
J11	VDDA_PLL2	VDDA_PLL2		PWR									
G11	VDDA_TEMP0	VDDA_TEMP0		PWR									
L11	VDDA_TEMP1	VDDA_TEMP1		PWR									
L10, M13	VDDR_CORE	VDDR_CORE		PWR									
F11, G12, G14	VDDSHV0	VDDSHV0		PWR									
M7, N6, P7	VDDSHV1	VDDSHV1		PWR									
R10, R8, T9	VDDSHV2	VDDSHV2		PWR									
P14, P15	VDDSHV3	VDDSHV3		PWR									
M14, M15	VDDSHV4	VDDSHV4		PWR									
L14, L15	VDDSHV5	VDDSHV5		PWR									
F9, G10, G8	VDDSHV_MCU	VDDSHV_MCU		PWR									
F7, G6, H7, J6, K7, L6	VDDS_DDR	VDDS_DDR		PWR									
J8	VDDS_DDR_C	VDDS_DDR_C		PWR									
K14	VDDS_MMC0	VDDS_MMC0		PWR									
H13	VDDS_OSC	VDDS_OSC		PWR									

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET RX/TX/PULL [7]	BALL STATE AFTER RESET RX/TX/PULL [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
J10, J12, K11, K9, L12, L8, M11, M9, N10, N8, P9	VDD_CORE	VDD_CORE		PWR									
H14	VDD_DLL_MMC0	VDD_DLL_MMC0		PWR									
K13	VDD_MMC0	VDD_MMC0		PWR									
K16	VMON_1P8_MCU	VMON_1P8_MCU		A									
E12	VMON_1P8_SOC	VMON_1P8_SOC		A									
F13	VMON_3P3_MCU	VMON_3P3_MCU		A									
F14	VMON_3P3_SOC	VMON_3P3_SOC		A									
K10	VMON_VSYS	VMON_VSYS		A									
G15	VPP	VPP		PWR									
A1, A21, A5, A6, AA1, AA15, AA18, AA21, C10, C15, C3, D1, E11, E13, F10, F15, F8, G1, G16, G3, G7, G9, H11, H20, H21, H6, H8, J14, J7, J9, K6, K8, L1, L16, L3, L7, L9, M10, M12, M6, M8, N11, N13, N15, N7, N9, P1, P10, P18, P6, P8, R12, R7, R9, T10, T11, T15, T16, T8, U3, V17, W10, W18, Y14, Y17, Y19	VSS	VSS		GND									

6.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

Note

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via PADCONFIG registers. Device subsystems may provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **PIN TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - PWR = Power
   - GND = Ground
   - CAP = LDO Capacitor
3. **DESCRIPTION:** Description of the signal
4. **BALL:** Ball number(s) associated with signal

For more information on the IO cell configurations, see the *Pad Configuration Registers* section in *Device Configuration* chapter of the device TRM.

6.3.1 ADC

Note

The ADC can be configured to operate as eight general-purpose digital inputs. For more information, see Analog-to-Digital Converter (ADC) section in Peripherals chapter in the device TRM.

6.3.1.1 MAIN Domain

Table 6-2. ADC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
ADC0_REFN (4)	A	ADC0 Negative Reference	J16
ADC0_REFP (4)	A	ADC0 Positive Reference	J15
ADC0_AIN0 (1) (2) (3)	A	ADC Analog Input 0 / GPIO1_80 (Input Only)	G20
ADC0_AIN1 (1) (2) (3)	A	ADC Analog Input 1 / GPIO1_81 (Input Only)	F20
ADC0_AIN2 (1) (2) (3)	A	ADC Analog Input 2 / GPIO1_82 (Input Only)	E21
ADC0_AIN3 (1) (2) (3)	A	ADC Analog Input 3 / GPIO1_83 (Input Only)	D20
ADC0_AIN4 (1) (2) (3)	A	ADC Analog Input 4 / GPIO1_84 (Input Only)	G21
ADC0_AIN5 (1) (2) (3)	A	ADC Analog Input 5 / GPIO1_85 (Input Only)	F21
ADC0_AIN6 (1) (2) (3)	A	ADC Analog Input 6 / GPIO1_86 (Input Only)	F19

Table 6-2. ADC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
ADC0_AIN7 (1) (2) (3)	A	ADC Analog Input 7 / GPIO1_87 (Input Only)	E20
ADC_EXT_TRIGGER0	I	ADC Trigger Input	B16, C13
ADC_EXT_TRIGGER1	I	ADC Trigger Input	D14, D16

(1) The General Purpose Input signal associated with this ADC0_AIN input has a debounce function when ADC0 is configured to operate in GPI mode. For more information on configuring ADC0 to operate in GPI mode, see the TRM *Analog-to-Digital Converter (ADC)* section in the *Peripherals* chapter. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

(2) The ADC0_AIN[7:0] inputs only have hysterisis when ADC0 is configured to operate in GPI mode.

(3) Any unused ADC0_AIN inputs must be pulled to VSS through a resistor or connected directly to VSS when VDDA_ADC is connected to a power source.

(4) The ADC0_REFP and ADC0_REFN reference inputs are analog inputs which must be treated like high transient power supply rails, where ADC0_REFN is expected to be connected directly to the PCB ground plane along with all other VSS pins, and ADC0_REFP is connected to a power source capable of providing at least 4mA of current. ADC0_REFP may be connected to the same power source as VDDA_ADC0 if the voltage tolerance of the supply provides an acceptable accuracy for the ADC reference. A high frequency decoupling capacitor must be connected directly between ADC0_REFP and ADC0_REFN. The high frequency decoupling capacitor should be placed in the ball array on the back side of the PCB and connected directly to the ADC0_REFP and ADC0_REFN pins with vias. ADC0_REFP may be connected to VSS if ADC0 is not used and VDDA_ADC0 has been connected to VSS. The high frequency decoupling capacitor described above will not be required if ADC0 is not used and ADC0_REFP is connected to VSS. See the *Pin Connectivity Requirements* section for more information on ADC0 connectivity.

6.3.2 CPSW3G

6.3.2.1 MAIN Domain

Table 6-3. CPSW3G0 RGMII1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
RGMII1_RXC	I	RGMII Receive Clock	AA5, W13
RGMII1_RX_CTL	I	RGMII Receive Control	V13, W6
RGMII1_TXC	IO	RGMII Transmit Clock	U14
RGMII1_TX_CTL	O	RGMII Transmit Control	U15
RGMII1_RD0	I	RGMII Receive Data 0	AA13, W5
RGMII1_RD1	I	RGMII Receive Data 1	U12, Y5
RGMII1_RD2	I	RGMII Receive Data 2	V6, Y13
RGMII1_RD3	I	RGMII Receive Data 3	V12, V5
RGMII1_TD0	O	RGMII Transmit Data 0	V15
RGMII1_TD1	O	RGMII Transmit Data 1	V14
RGMII1_TD2	O	RGMII Transmit Data 2	W14
RGMII1_TD3	O	RGMII Transmit Data 3	AA14

Table 6-4. CPSW3G0 RGMII2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
RGMII2_RXC	I	RGMII Receive Clock	U11
RGMII2_RX_CTL	I	RGMII Receive Control	W12
RGMII2_TXC	IO	RGMII Transmit Clock	Y10
RGMII2_TX_CTL	O	RGMII Transmit Control	Y11
RGMII2_RD0	I	RGMII Receive Data 0	W11
RGMII2_RD1	I	RGMII Receive Data 1	V11
RGMII2_RD2	I	RGMII Receive Data 2	AA12
RGMII2_RD3	I	RGMII Receive Data 3	Y12
RGMII2_TD0	O	RGMII Transmit Data 0	AA10
RGMII2_TD1	O	RGMII Transmit Data 1	V10
RGMII2_TD2	O	RGMII Transmit Data 2	U10

Table 6-4. CPSW3G0 RGMII2 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
RGMII2_TD3	O	RGMII Transmit Data 3	AA11

Table 6-5. CPSW3G0 RMII1 and RMII2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
RMII1_CRS_DV	I	RMII Carrier Sense / Data Valid	R2, V12
RMII1_RX_ER	I	RMII Receive Data Error	U15, W6
RMII1_TX_EN	O	RMII Transmit Enable	P5, Y13
RMII2_CRS_DV	I	RMII Carrier Sense / Data Valid	U10
RMII2_RX_ER	I	RMII Receive Data Error	W12
RMII2_TX_EN	O	RMII Transmit Enable	Y11
RMII1_RXD0	I	RMII Receive Data 0	V15, W5
RMII1_RXD1	I	RMII Receive Data 1	V14, Y5
RMII1_TXD0	O	RMII Transmit Data 0	V6, W14
RMII1_TXD1	O	RMII Transmit Data 1	AA14, V5
RMII2_RXD0	I	RMII Receive Data 0	W11
RMII2_RXD1	I	RMII Receive Data 1	V11
RMII2_TXD0	O	RMII Transmit Data 0	AA10
RMII2_TXD1	O	RMII Transmit Data 1	V10
RMII_REF_CLK (1)	I	RMII Reference Clock	AA5, U14

(1) RMII_REF_CLK is common to both RMII1 and RMII2.

6.3.3 CPTS

6.3.3.1 MAIN Domain

Table 6-6. CP GEMAC CPTS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
CP_GEMAC_CPTS0_RFT_CLK	I	CPTS Reference Clock Input to CPSW3G0 CPTS	D18
CP_GEMAC_CPTS0_TS_COMP	O	CPTS Time Stamp Counter Compare Output from CPSW3G0 CPTS	E15, K18, W1
CP_GEMAC_CPTS0_TS_SYNC	O	CPTS Time Stamp Counter Bit Output from CPSW3G0 CPTS	B16, D16, K19, U1
CP_GEMAC_CPTS0_HW1TSPUSH	I	CPTS Hardware Time Stamp Push Input to CPSW3G0 CPTS	E14, L21, V1
CP_GEMAC_CPTS0_HW2TSPUSH	I	CPTS Hardware Time Stamp Push Input to CPSW3G0 CPTS	E16, K21, T1

Table 6-7. CPTS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
CPTS0_RFT_CLK	I	CPTS Reference Clock Input	D18
CPTS0_TS_COMP	O	CPTS Time Stamp Counter Compare Output	C13, W1, W7
CPTS0_TS_SYNC	O	CPTS Time Stamp Counter Bit Output	D14, U1, U7
CPTS0_HW1TSPUSH	I	CPTS Hardware Time Stamp Push Input to Time Sync Router	C18, V1, V7
CPTS0_HW2TSPUSH	I	CPTS Hardware Time Stamp Push Input to Time Sync Router	B19, T1, U13
SYNC0_OUT	O	CPTS Time Stamp Generator Bit 0 Output from Time Sync Router	D18
SYNC1_OUT	O	CPTS Time Stamp Generator Bit 1 Output from Time Sync Router	A19

Table 6-7. CPTS0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
SYNC2_OUT	O	CPTS Time Stamp Generator Bit 2 Output from Time Sync Router	A17
SYNC3_OUT	O	CPTS Time Stamp Generator Bit 3 Output from Time Sync Router	B17

6.3.4 DDRSS

6.3.4.1 MAIN Domain

Table 6-8. DDRSS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
DDR0_ACT_n	O	DDRSS Activation Command	H2
DDR0_ALERT_n	IO	DDRSS Alert	H1
DDR0_CAS_n	O	DDRSS Column Address Strobe	J5
DDR0_PAR	O	DDRSS Command and Address Parity	K5
DDR0_RAS_n	O	DDRSS Row Address Strobe	F6
DDR0_WE_n	O	DDRSS Write Enable	H4
DDR0_A0	O	DDRSS Address Bus	D2
DDR0_A1	O	DDRSS Address Bus	C5
DDR0_A2	O	DDRSS Address Bus	E2
DDR0_A3	O	DDRSS Address Bus	D4
DDR0_A4	O	DDRSS Address Bus	D3
DDR0_A5	O	DDRSS Address Bus	F2
DDR0_A6	O	DDRSS Address Bus	J2
DDR0_A7	O	DDRSS Address Bus	L5
DDR0_A8	O	DDRSS Address Bus	J3
DDR0_A9	O	DDRSS Address Bus	J4
DDR0_A10	O	DDRSS Address Bus	K3
DDR0_A11	O	DDRSS Address Bus	J1
DDR0_A12	O	DDRSS Address Bus	M5
DDR0_A13	O	DDRSS Address Bus	K4
DDR0_BA0	O	DDRSS Bank Address	G4
DDR0_BA1	O	DDRSS Bank Address	G5
DDR0_BG0	O	DDRSS Bank Group	G2
DDR0_BG1	O	DDRSS Bank Group	H3
DDR0_CAL0 (1)	A	IO Pad Calibration Resistor	H5
DDR0_CK0	O	DDRSS Clock	F1
DDR0_CK0_n	O	DDRSS Negative Clock	E1
DDR0_CKE0	O	DDRSS Clock Enable	F4
DDR0_CKE1	O	DDRSS Clock Enable	F3
DDR0_CS0_n	O	DDRSS Chip Select 0	E3
DDR0_CS1_n	O	DDRSS Chip Select 1	E4
DDR0_DM0	IO	DDRSS Data Mask	B2
DDR0_DM1	IO	DDRSS Data Mask	M2
DDR0_DQ0	IO	DDRSS Data	A3
DDR0_DQ1	IO	DDRSS Data	A2
DDR0_DQ2	IO	DDRSS Data	B5
DDR0_DQ3	IO	DDRSS Data	A4

Table 6-8. DDRSS0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
DDR0_DQ4	IO	DDRSS Data	B3
DDR0_DQ5	IO	DDRSS Data	C4
DDR0_DQ6	IO	DDRSS Data	C2
DDR0_DQ7	IO	DDRSS Data	B4
DDR0_DQ8	IO	DDRSS Data	N5
DDR0_DQ9	IO	DDRSS Data	L4
DDR0_DQ10	IO	DDRSS Data	L2
DDR0_DQ11	IO	DDRSS Data	M3
DDR0_DQ12	IO	DDRSS Data	N4
DDR0_DQ13	IO	DDRSS Data	N3
DDR0_DQ14	IO	DDRSS Data	M4
DDR0_DQ15	IO	DDRSS Data	N2
DDR0_DQS0	IO	DDRSS Data Strobe 0	C1
DDR0_DQS0_n	IO	DDRSS Complimentary Data Strobe 0	B1
DDR0_DQS1	IO	DDRSS Data Strobe 1	N1
DDR0_DQS1_n	IO	DDRSS Complimentary Data Strobe 1	M1
DDR0_ODT0	O	DDRSS On-Die Termination for Chip Select 0	E5
DDR0_ODT1	O	DDRSS On-Die Termination for Chip Select 1	F5
DDR0_RESET0_n	O	DDRSS Reset	D5

(1) An external 240 Ω ±1% resistor must be connected between this pin and VSS. The maximum power dissipation for the resistor is 5.2mW. No external voltage should be applied to this pin.

6.3.5 ECAP

6.3.5.1 MAIN Domain

Table 6-9. ECAP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
ECAP0_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	D18

Table 6-10. ECAP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
ECAP1_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	C17

Table 6-11. ECAP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
ECAP2_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	D17

6.3.6 Emulation and Debug

6.3.6.1 MAIN Domain

Table 6-12. Trace Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
TRC_CLK	O	Trace Clock	T20
TRC_CTL	O	Trace Control	U21
TRC_DATA0	O	Trace Data 0	T18

Table 6-12. Trace Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
TRC_DATA1	O	Trace Data 1	U20
TRC_DATA2	O	Trace Data 2	U18
TRC_DATA3	O	Trace Data 3	U19
TRC_DATA4	O	Trace Data 4	V20
TRC_DATA5	O	Trace Data 5	V21
TRC_DATA6	O	Trace Data 6	V19
TRC_DATA7	O	Trace Data 7	T17
TRC_DATA8	O	Trace Data 8	R16
TRC_DATA9	O	Trace Data 9	W20
TRC_DATA10	O	Trace Data 10	W21
TRC_DATA11	O	Trace Data 11	V18
TRC_DATA12	O	Trace Data 12	Y21
TRC_DATA13	O	Trace Data 13	Y20
TRC_DATA14	O	Trace Data 14	R17
TRC_DATA15	O	Trace Data 15	P16
TRC_DATA16	O	Trace Data 16	R18
TRC_DATA17	O	Trace Data 17	T21
TRC_DATA18	O	Trace Data 18	P17
TRC_DATA19	O	Trace Data 19	T19
TRC_DATA20	O	Trace Data 20	W19
TRC_DATA21	O	Trace Data 21	Y18
TRC_DATA22	O	Trace Data 22	N16
TRC_DATA23	O	Trace Data 23	R19

6.3.6.2 MCU Domain

Table 6-13. JTAG Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EMU0	IO	Emulation Control 0	D10
EMU1	IO	Emulation Control 1	E10
TCK	I	JTAG Test Clock Input	B11
TDI	I	JTAG Test Data Input	C11
TDO	OZ	JTAG Test Data Output	A12
TMS	I	JTAG Test Mode Select Input	C12
TRSTn	I	JTAG Reset	D11

6.3.7 EPWM

6.3.7.1 MAIN Domain

Table 6-14. EPWM Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EHRPWM_SOCA	O	EHRPWM Start of Conversion A	C17
EHRPWM_SOCB	O	EHRPWM Start of Conversion B	D17
EHRPWM_TZn_IN0	I	EHRPWM Trip Zone Input 0 (active low)	T18
EHRPWM_TZn_IN1	I	EHRPWM Trip Zone Input 1 (active low)	V21
EHRPWM_TZn_IN2	I	EHRPWM Trip Zone Input 2 (active low)	R16, R20
EHRPWM_TZn_IN3	I	EHRPWM Trip Zone Input 3 (active low)	P16

Table 6-14. EPWM Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EHRPWM_TZn_IN4	I	EHRPWM Trip Zone Input 4 (active low)	P17, P19
EHRPWM_TZn_IN5	I	EHRPWM Trip Zone Input 5 (active low)	R21, Y18

Table 6-15. EPWM0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EHRPWM0_A	IO	EHRPWM Output A	U20
EHRPWM0_B	IO	EHRPWM Output B	U18
EHRPWM0_SYNCI	I	Sync Input to EHRPWM module from an external pin	T20
EHRPWM0_SYNCO	O	Sync Output to EHRPWM module to an external pin	U21

Table 6-16. EPWM1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EHRPWM1_A	IO	EHRPWM Output A	U19
EHRPWM1_B	IO	EHRPWM Output B	V20

Table 6-17. EPWM2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EHRPWM2_A	IO	EHRPWM Output A	V19
EHRPWM2_B	IO	EHRPWM Output B	T17

Table 6-18. EPWM3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EHRPWM3_A	IO	EHRPWM Output A	V18
EHRPWM3_B	IO	EHRPWM Output B	Y21
EHRPWM3_SYNCI	I	Sync Input to EHRPWM module from an external pin	Y20
EHRPWM3_SYNCO	O	Sync Output to EHRPWM module to an external pin	R17

Table 6-19. EPWM4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EHRPWM4_A	IO	EHRPWM Output A	R18
EHRPWM4_B	IO	EHRPWM Output B	T21

Table 6-20. EPWM5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EHRPWM5_A	IO	EHRPWM Output A	T19
EHRPWM5_B	IO	EHRPWM Output B	W19

Table 6-21. EPWM6 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EHRPWM6_A	IO	EHRPWM Output A	B14, N16
EHRPWM6_B	IO	EHRPWM Output B	A15, N17
EHRPWM6_SYNCI	I	Sync Input to EHRPWM module from an external pin	C14, R19
EHRPWM6_SYNCO	O	Sync Output to EHRPWM module to an external pin	B15, R20

Table 6-22. EPWM7 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EHRPWM7_A	IO	EHRPWM Output A	P17, P5, W20
EHRPWM7_B	IO	EHRPWM Output B	R2, W21, Y18

Table 6-23. EPWM8 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EHRPWM8_A	IO	EHRPWM Output A	V1, V21
EHRPWM8_B	IO	EHRPWM Output B	R16, W1

6.3.8 EQEP

6.3.8.1 MAIN Domain

Table 6-24. EQEP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EQEP0_A (1)	I	EQEP Quadrature Input A	D15, N16, Y2
EQEP0_B (1)	I	EQEP Quadrature Input B	C16, N17, W2
EQEP0_I (1)	IO	EQEP Index	A16, R20, T6, Y5
EQEP0_S (1)	IO	EQEP Strobe	B16, R19, V3

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

Table 6-25. EQEP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EQEP1_A (1)	I	EQEP Quadrature Input A	E15, T4, W20
EQEP1_B (1)	I	EQEP Quadrature Input B	E14, W21, W3
EQEP1_I (1)	IO	EQEP Index	E16, R21, U6, V6
EQEP1_S (1)	IO	EQEP Strobe	D16, P19, P4

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

Table 6-26. EQEP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EQEP2_A (1)	I	EQEP Quadrature Input A	C17, R5
EQEP2_B (1)	I	EQEP Quadrature Input B	D17, W5, Y4
EQEP2_I (1)	IO	EQEP Index	A17, W4
EQEP2_S (1)	IO	EQEP Strobe	B17, R1

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

6.3.9 FSI

6.3.9.1 MAIN Domain

Table 6-27. FSI0 RX Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
FSI_RX0_CLK	I	FSI Clock	V19
FSI_RX0_D0	I	FSI Data	T17
FSI_RX0_D1	I	FSI Data	R16

Table 6-28. FSI0 TX Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
FSI_TX0_CLK	O	FSI Clock	T19
FSI_TX0_D0	O	FSI Data	Y21
FSI_TX0_D1	O	FSI Data	Y20

Table 6-29. FSI1 RX Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
FSI_RX1_CLK	I	FSI Clock	W20
FSI_RX1_D0	I	FSI Data	W21
FSI_RX1_D1	I	FSI Data	V18

Table 6-30. FSI1 TX Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
FSI_TX1_CLK	O	FSI Clock	N16
FSI_TX1_D0	O	FSI Data	P17
FSI_TX1_D1	O	FSI Data	Y18

Table 6-31. FSI2 RX Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
FSI_RX2_CLK	I	FSI Clock	T20
FSI_RX2_D0	I	FSI Data	U21
FSI_RX2_D1	I	FSI Data	T18

Table 6-32. FSI3 RX Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
FSI_RX3_CLK	I	FSI Clock	U20
FSI_RX3_D0	I	FSI Data	U18
FSI_RX3_D1	I	FSI Data	U19

Table 6-33. FSI4 RX Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
FSI_RX4_CLK	I	FSI Clock	R17
FSI_RX4_D0	I	FSI Data	V20
FSI_RX4_D1	I	FSI Data	V21

Table 6-34. FSI5 RX Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
FSI_RX5_CLK	I	FSI Clock	P16
FSI_RX5_D0	I	FSI Data	R18
FSI_RX5_D1	I	FSI Data	T21

6.3.10 GPIO

6.3.10.1 MAIN Domain

Table 6-35. GPIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
GPIO0_0	IO	General Purpose Input/Output	N20

Table 6-35. GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
GPIO0_1	IO	General Purpose Input/Output	N21
GPIO0_2	IO	General Purpose Input/Output	N19
GPIO0_3	IO	General Purpose Input/Output	M19
GPIO0_4	IO	General Purpose Input/Output	M18
GPIO0_5	IO	General Purpose Input/Output	M20
GPIO0_6	IO	General Purpose Input/Output	M21
GPIO0_7	IO	General Purpose Input/Output	P21
GPIO0_8	IO	General Purpose Input/Output	P20
GPIO0_9	IO	General Purpose Input/Output	N18
GPIO0_10	IO	General Purpose Input/Output	M17
GPIO0_11	IO	General Purpose Input/Output	L19
GPIO0_12	IO	General Purpose Input/Output	L18
GPIO0_13	IO	General Purpose Input/Output	K17
GPIO0_14	IO	General Purpose Input/Output	L17
GPIO0_15	IO	General Purpose Input/Output	T20
GPIO0_16	IO	General Purpose Input/Output	U21
GPIO0_17	IO	General Purpose Input/Output	T18
GPIO0_18	IO	General Purpose Input/Output	U20
GPIO0_19	IO	General Purpose Input/Output	AA14
GPIO0_20	IO	General Purpose Input/Output	Y13
GPIO0_21	IO	General Purpose Input/Output	V20
GPIO0_22	IO	General Purpose Input/Output	V21
GPIO0_23	IO	General Purpose Input/Output	V19
GPIO0_24	IO	General Purpose Input/Output	T17
GPIO0_25	IO	General Purpose Input/Output	R16
GPIO0_26	IO	General Purpose Input/Output	W20
GPIO0_27	IO	General Purpose Input/Output	W21
GPIO0_28	IO	General Purpose Input/Output	V18
GPIO0_29	IO	General Purpose Input/Output	Y21
GPIO0_30	IO	General Purpose Input/Output	Y20
GPIO0_31	IO	General Purpose Input/Output	R17
GPIO0_32	IO	General Purpose Input/Output	P16
GPIO0_33	IO	General Purpose Input/Output	R18
GPIO0_34	IO	General Purpose Input/Output	T21
GPIO0_35	IO	General Purpose Input/Output	P17
GPIO0_36	IO	General Purpose Input/Output	T19
GPIO0_37	IO	General Purpose Input/Output	W19
GPIO0_38	IO	General Purpose Input/Output	Y18
GPIO0_39	IO	General Purpose Input/Output	N16
GPIO0_40	IO	General Purpose Input/Output	N17
GPIO0_41	IO	General Purpose Input/Output	R19
GPIO0_42	IO	General Purpose Input/Output	R20
GPIO0_43 (1)	IO	General Purpose Input/Output	P19
GPIO0_44 (1)	IO	General Purpose Input/Output	R21
GPIO0_45	IO	General Purpose Input/Output	Y7

Table 6-35. GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
GPIO0_46	IO	General Purpose Input/Output	U8
GPIO0_47	IO	General Purpose Input/Output	W8
GPIO0_48	IO	General Purpose Input/Output	V8
GPIO0_49	IO	General Purpose Input/Output	Y8
GPIO0_50	IO	General Purpose Input/Output	V13
GPIO0_51	IO	General Purpose Input/Output	AA7
GPIO0_52	IO	General Purpose Input/Output	U13
GPIO0_53	IO	General Purpose Input/Output	W13
GPIO0_54	IO	General Purpose Input/Output	U15
GPIO0_55	IO	General Purpose Input/Output	U14
GPIO0_56	IO	General Purpose Input/Output	AA8
GPIO0_57	IO	General Purpose Input/Output	U9
GPIO0_58	IO	General Purpose Input/Output	W9
GPIO0_59	IO	General Purpose Input/Output	AA9
GPIO0_60	IO	General Purpose Input/Output	Y9
GPIO0_61	IO	General Purpose Input/Output	V9
GPIO0_62	IO	General Purpose Input/Output	U7
GPIO0_63	IO	General Purpose Input/Output	V7
GPIO0_64	IO	General Purpose Input/Output	W7
GPIO0_65	IO	General Purpose Input/Output	W11
GPIO0_66	IO	General Purpose Input/Output	V11
GPIO0_67	IO	General Purpose Input/Output	AA12
GPIO0_68	IO	General Purpose Input/Output	Y12
GPIO0_69	IO	General Purpose Input/Output	W12
GPIO0_70	IO	General Purpose Input/Output	AA13
GPIO0_71	IO	General Purpose Input/Output	U11
GPIO0_72	IO	General Purpose Input/Output	V15
GPIO0_73	IO	General Purpose Input/Output	U12
GPIO0_74	IO	General Purpose Input/Output	V14
GPIO0_75	IO	General Purpose Input/Output	W14
GPIO0_76	IO	General Purpose Input/Output	AA10
GPIO0_77	IO	General Purpose Input/Output	V10
GPIO0_78	IO	General Purpose Input/Output	U10
GPIO0_79	IO	General Purpose Input/Output	AA11
GPIO0_80	IO	General Purpose Input/Output	Y11
GPIO0_81	IO	General Purpose Input/Output	Y10
GPIO0_82	IO	General Purpose Input/Output	U18
GPIO0_83	IO	General Purpose Input/Output	U19
GPIO0_84	IO	General Purpose Input/Output	V12
GPIO0_85	IO	General Purpose Input/Output	AA6
GPIO0_86	IO	General Purpose Input/Output	Y6

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

Table 6-36. GPIO1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
GPIO1_0	IO	General Purpose Input/Output	Y1
GPIO1_1	IO	General Purpose Input/Output	R4
GPIO1_2	IO	General Purpose Input/Output	U2
GPIO1_3	IO	General Purpose Input/Output	V2
GPIO1_4	IO	General Purpose Input/Output	AA2
GPIO1_5	IO	General Purpose Input/Output	R3
GPIO1_6	IO	General Purpose Input/Output	T3
GPIO1_7	IO	General Purpose Input/Output	T1
GPIO1_8	IO	General Purpose Input/Output	T2
GPIO1_9	IO	General Purpose Input/Output	W6
GPIO1_10	IO	General Purpose Input/Output	AA5
GPIO1_11	IO	General Purpose Input/Output	Y3
GPIO1_12	IO	General Purpose Input/Output	AA3
GPIO1_13	IO	General Purpose Input/Output	R6
GPIO1_14	IO	General Purpose Input/Output	V4
GPIO1_15	IO	General Purpose Input/Output	T5
GPIO1_16	IO	General Purpose Input/Output	U4
GPIO1_17	IO	General Purpose Input/Output	U1
GPIO1_18	IO	General Purpose Input/Output	V1
GPIO1_19	IO	General Purpose Input/Output	W1
GPIO1_20	IO	General Purpose Input/Output	Y2
GPIO1_21	IO	General Purpose Input/Output	W2
GPIO1_22	IO	General Purpose Input/Output	V3
GPIO1_23	IO	General Purpose Input/Output	T4
GPIO1_24	IO	General Purpose Input/Output	W3
GPIO1_25	IO	General Purpose Input/Output	P4
GPIO1_26	IO	General Purpose Input/Output	R5
GPIO1_27	IO	General Purpose Input/Output	W5
GPIO1_28	IO	General Purpose Input/Output	R1
GPIO1_29	IO	General Purpose Input/Output	Y5
GPIO1_30	IO	General Purpose Input/Output	V6
GPIO1_31	IO	General Purpose Input/Output	W4
GPIO1_32	IO	General Purpose Input/Output	Y4
GPIO1_33	IO	General Purpose Input/Output	T6
GPIO1_34	IO	General Purpose Input/Output	U6
GPIO1_35	IO	General Purpose Input/Output	U5
GPIO1_36	IO	General Purpose Input/Output	AA4
GPIO1_37	IO	General Purpose Input/Output	V5
GPIO1_38	IO	General Purpose Input/Output	P5
GPIO1_39	IO	General Purpose Input/Output	R2
GPIO1_40	IO	General Purpose Input/Output	P2
GPIO1_41	IO	General Purpose Input/Output	P3
GPIO1_42	IO	General Purpose Input/Output	D12
GPIO1_43	IO	General Purpose Input/Output	C13
GPIO1_44	IO	General Purpose Input/Output	D13

Table 6-36. GPIO1 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
GPIO1_45	IO	General Purpose Input/Output	A13
GPIO1_46	IO	General Purpose Input/Output	A14
GPIO1_47	IO	General Purpose Input/Output	B14
GPIO1_48	IO	General Purpose Input/Output	D14
GPIO1_49	IO	General Purpose Input/Output	C14
GPIO1_50	IO	General Purpose Input/Output	B15
GPIO1_51	IO	General Purpose Input/Output	A15
GPIO1_52	IO	General Purpose Input/Output	D15
GPIO1_53	IO	General Purpose Input/Output	C16
GPIO1_54	IO	General Purpose Input/Output	B16
GPIO1_55	IO	General Purpose Input/Output	A16
GPIO1_56	IO	General Purpose Input/Output	E15
GPIO1_57	IO	General Purpose Input/Output	E14
GPIO1_58	IO	General Purpose Input/Output	D16
GPIO1_59	IO	General Purpose Input/Output	E16
GPIO1_60	IO	General Purpose Input/Output	A17
GPIO1_61	IO	General Purpose Input/Output	B17
GPIO1_62	IO	General Purpose Input/Output	C17
GPIO1_63	IO	General Purpose Input/Output	D17
GPIO1_64	IOD	General Purpose Input/Output	A18
GPIO1_65	IOD	General Purpose Input/Output	B18
GPIO1_66	IO	General Purpose Input/Output	C18
GPIO1_67	IO	General Purpose Input/Output	B19
GPIO1_68 (1)	IO	General Purpose Input/Output	D18
GPIO1_69	IO	General Purpose Input/Output	A19
GPIO1_70 (1)	IOD	General Purpose Input/Output	C19
GPIO1_71 (1)	IO	General Purpose Input/Output	K18
GPIO1_72 (1)	IO	General Purpose Input/Output	K19
GPIO1_73 (1)	IO	General Purpose Input/Output	L21
GPIO1_74 (1)	IO	General Purpose Input/Output	K21
GPIO1_75 (1)	IO	General Purpose Input/Output	L20
GPIO1_76 (1)	IO	General Purpose Input/Output	J19
GPIO1_77 (1)	IO	General Purpose Input/Output	D19
GPIO1_78 (1)	IO	General Purpose Input/Output	C20
GPIO1_79	IO	General Purpose Input/Output	E19

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

6.3.10.2 MCU Domain

Table 6-37. MCU_GPIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCU_GPIO0_0 (1)	IO	General Purpose Input/Output	E8
MCU_GPIO0_1 (1)	IO	General Purpose Input/Output	D8
MCU_GPIO0_2	IO	General Purpose Input/Output	A8
MCU_GPIO0_3	IO	General Purpose Input/Output	A9
MCU_GPIO0_4	IO	General Purpose Input/Output	B6

Table 6-37. MCU_GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCU_GPIO0_5 (1)	IO	General Purpose Input/Output	A7
MCU_GPIO0_6 (1)	IO	General Purpose Input/Output	B7
MCU_GPIO0_7	IO	General Purpose Input/Output	D7
MCU_GPIO0_8	IO	General Purpose Input/Output	C7
MCU_GPIO0_9	IO	General Purpose Input/Output	C8
MCU_GPIO0_10	IO	General Purpose Input/Output	E7
MCU_GPIO0_11	IO	General Purpose Input/Output	E6
MCU_GPIO0_12 (1)	IO	General Purpose Input/Output	C6
MCU_GPIO0_13 (1)	IO	General Purpose Input/Output	D6
MCU_GPIO0_14	IO	General Purpose Input/Output	C9
MCU_GPIO0_15	IO	General Purpose Input/Output	D9
MCU_GPIO0_16 (1)	IO	General Purpose Input/Output	B8
MCU_GPIO0_17 (1)	IO	General Purpose Input/Output	B9
MCU_GPIO0_18	IOD	General Purpose Input/Output	E9
MCU_GPIO0_19	IOD	General Purpose Input/Output	A10
MCU_GPIO0_20 (1)	IO	General Purpose Input/Output	A11
MCU_GPIO0_21 (1)	IO	General Purpose Input/Output	B10
MCU_GPIO0_22	IO	General Purpose Input/Output	B13

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

6.3.11 GPMC

6.3.11.1 MAIN Domain

Table 6-38. GPMC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
GPMC0_ADVn_ALE	O	GPMC Address Valid (active low) or Address Latch Enable	P16
GPMC0_CLK (1)	O	GPMC clock	R17
GPMC0_DIR	O	GPMC Data Bus Signal Direction Control	N17
GPMC0_FCLK_MUX	O	GPMC functional clock output selected through a mux logic	R17
GPMC0_OEn_REn	O	GPMC Output Enable (active low) or Read Enable (active low)	R18
GPMC0_WEn	O	GPMC Write Enable (active low)	T21
GPMC0_WPn	O	GPMC Flash Write Protect (active low)	N16
GPMC0_A0	OZ	GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories	U2, U7
GPMC0_A1	OZ	GPMC address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode	AA2, V7
GPMC0_A2	OZ	GPMC address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode	T2, W7
GPMC0_A3	OZ	GPMC address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode	V4, W11
GPMC0_A4	OZ	GPMC address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode	U4, V11
GPMC0_A5	OZ	GPMC address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode	AA12, V1
GPMC0_A6	OZ	GPMC address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode	W1, Y12

Table 6-38. GPMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
GPMC0_A7	OZ	GPMC address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode	W12, Y4
GPMC0_A8	OZ	GPMC address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode	AA13, T6
GPMC0_A9	OZ	GPMC address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode	U11, U6
GPMC0_A10	OZ	GPMC address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode	U5, V15
GPMC0_A11	OZ	GPMC address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AA4, U12
GPMC0_A12	OZ	GPMC address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	P2, V14
GPMC0_A13	OZ	GPMC address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	P3, W14
GPMC0_A14	OZ	GPMC address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AA10, AA3
GPMC0_A15	OZ	GPMC address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	R6, V10
GPMC0_A16	OZ	GPMC address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	T5, U10
GPMC0_A17	OZ	GPMC address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AA11, U1
GPMC0_A18	OZ	GPMC address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	T4, Y11
GPMC0_A19	OZ	GPMC address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	R5, Y10
GPMC0_A20	OZ	GPMC address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	R21
GPMC0_A21	OZ	GPMC address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	Y18
GPMC0_A22	OZ	GPMC address 22 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	N16
GPMC0_AD0	IO	GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode	T20
GPMC0_AD1	IO	GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode	U21
GPMC0_AD2	IO	GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	T18
GPMC0_AD3	IO	GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode	U20
GPMC0_AD4	IO	GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode	U18
GPMC0_AD5	IO	GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode	U19
GPMC0_AD6	IO	GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode	V20

Table 6-38. GPMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
GPMC0_AD7	IO	GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode	V21
GPMC0_AD8	IO	GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode	V19
GPMC0_AD9	IO	GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode	T17
GPMC0_AD10	IO	GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode	R16
GPMC0_AD11	IO	GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode	W20
GPMC0_AD12	IO	GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode	W21
GPMC0_AD13	IO	GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode	V18
GPMC0_AD14	IO	GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode	Y21
GPMC0_AD15	IO	GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode	Y20
GPMC0_AD16	IO	GPMC Data 16 Input/Output in A/D non-multiplexed mode and additionally Address 17 Output in A/D multiplexed mode	Y7
GPMC0_AD17	IO	GPMC Data 17 Input/Output in A/D non-multiplexed mode and additionally Address 18 Output in A/D multiplexed mode	U8
GPMC0_AD18	IO	GPMC Data 18 Input/Output in A/D non-multiplexed mode and additionally Address 19 Output in A/D multiplexed mode	W8
GPMC0_AD19	IO	GPMC Data 19 Input/Output in A/D non-multiplexed mode and additionally Address 20 Output in A/D multiplexed mode	V8
GPMC0_AD20	IO	GPMC Data 20 Input/Output in A/D non-multiplexed mode and additionally Address 21 Output in A/D multiplexed mode	Y8
GPMC0_AD21	IO	GPMC Data 21 Input/Output in A/D non-multiplexed mode and additionally Address 22 Output in A/D multiplexed mode	V13
GPMC0_AD22	IO	GPMC Data 22 Input/Output in A/D non-multiplexed mode and additionally Address 23 Output in A/D multiplexed mode	AA7
GPMC0_AD23	IO	GPMC Data 23 Input/Output in A/D non-multiplexed mode and additionally Address 24 Output in A/D multiplexed mode	U13
GPMC0_AD24	IO	GPMC Data 24 Input/Output in A/D non-multiplexed mode and additionally Address 25 Output in A/D multiplexed mode	W13
GPMC0_AD25	IO	GPMC Data 25 Input/Output in A/D non-multiplexed mode and additionally Address 26 Output in A/D multiplexed mode	U15

Table 6-38. GPMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
GPMC0_AD26	IO	GPMC Data 26 Input/Output in A/D non-multiplexed mode and additionally Address 27 Output in A/D multiplexed mode	U14
GPMC0_AD27	IO	GPMC Data 27 Input/Output in A/D non-multiplexed mode and additionally Address 28 Output in A/D multiplexed mode	AA8
GPMC0_AD28	IO	GPMC Data 28 Input/Output in A/D non-multiplexed mode and additionally Address 29 Output in A/D multiplexed mode	U9
GPMC0_AD29	IO	GPMC Data 29 Input/Output in A/D non-multiplexed mode and additionally Address 30 Output in A/D multiplexed mode	W9
GPMC0_AD30	IO	GPMC Data 30 Input/Output in A/D non-multiplexed mode and additionally Address 31 Output in A/D multiplexed mode	AA9
GPMC0_AD31	IO	GPMC Data 31 Input/Output in A/D non-multiplexed mode and additionally Address 0 Output in A/D multiplexed mode	Y9
GPMC0_BE0n_CLE	O	GPMC Lower-Byte Enable (active low) or Command Latch Enable	P17
GPMC0_BE1n	O	GPMC Upper-Byte Enable (active low)	T19
GPMC0_BE2n	O	GPMC Upper-Byte Enable (active low)	V9
GPMC0_BE3n	O	GPMC Upper-Byte Enable (active low)	AA14
GPMC0_CSn0	O	GPMC Chip Select 0 (active low)	R19
GPMC0_CSn1	O	GPMC Chip Select 1 (active low)	R20
GPMC0_CSn2	O	GPMC Chip Select 2 (active low)	P19
GPMC0_CSn3	O	GPMC Chip Select 3 (active low)	R21
GPMC0_WAIT0	I	GPMC External Indication of Wait	W19
GPMC0_WAIT1	I	GPMC External Indication of Wait	Y18

(1) The RXACTIVE bit of the CTRLMMR_PADCONFIG32 register must be set to 0x1 and the TX_DIS bit of the CTRLMMR_PADCONFIG32 register must be reset to 0x0 when GPMC0 is operating in synchronous mode.

6.3.12 I2C

6.3.12.1 MAIN Domain

Table 6-39. I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
I2C0_SCL	IOD	I2C Clock	A18
I2C0_SDA	IOD	I2C Data	B18

Table 6-40. I2C1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
I2C1_SCL	IOD	I2C Clock	C18
I2C1_SDA	IOD	I2C Data	B19

Table 6-41. I2C2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
I2C2_SCL	IOD	I2C Clock	C13, P19
I2C2_SDA	IOD	I2C Data	D14, R21

Table 6-42. I2C3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
I2C3_SCL	IOD	I2C Clock	C17
I2C3_SDA	IOD	I2C Data	D17

6.3.12.2 MCU Domain

Table 6-43. MCU_I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCU_I2C0_SCL	IOD	I2C Clock	E9
MCU_I2C0_SDA	IOD	I2C Data	A10

Table 6-44. MCU_I2C1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCU_I2C1_SCL	IOD	I2C Clock	A11
MCU_I2C1_SDA	IOD	I2C Data	B10

6.3.13 MCAN

6.3.13.1 MAIN Domain

Table 6-45. MCAN0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCAN0_RX	I	MCAN Receive Data	B17
MCAN0_TX	O	MCAN Transmit Data	A17

Table 6-46. MCAN1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCAN1_RX	I	MCAN Receive Data	D17
MCAN1_TX	O	MCAN Transmit Data	C17

6.3.14 MCSPI

6.3.14.1 MAIN Domain

Table 6-47. MCSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
SPI0_CLK	IO	SPI Clock	D13
SPI0_CS0	IO	SPI Chip Select 0	D12
SPI0_CS1	IO	SPI Chip Select 1	C13
SPI0_CS2	IO	SPI Chip Select 2	B16
SPI0_CS3	IO	SPI Chip Select 3	A16
SPI0_D0	IO	SPI Data 0	A13
SPI0_D1	IO	SPI Data 1	A14

Table 6-48. MCSPI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
SPI1_CLK	IO	SPI Clock	C14
SPI1_CS0	IO	SPI Chip Select 0	B14
SPI1_CS1	IO	SPI Chip Select 1	D14
SPI1_CS2	IO	SPI Chip Select 2	D16
SPI1_CS3	IO	SPI Chip Select 3	E16

Table 6-48. MCSPI1 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
SPI1_D0	IO	SPI Data 0	B15
SPI1_D1	IO	SPI Data 1	A15

Table 6-49. MCSPI2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
SPI2_CLK	IO	SPI Clock	E14
SPI2_CS0	IO	SPI Chip Select 0	E15
SPI2_CS1	IO	SPI Chip Select 1	C18
SPI2_CS2	IO	SPI Chip Select 2	B19
SPI2_CS3	IO	SPI Chip Select 3	A19
SPI2_D0	IO	SPI Data 0	D15
SPI2_D1	IO	SPI Data 1	C16

Table 6-50. MCSPI3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
SPI3_CLK	IO	SPI Clock	U4
SPI3_CS0	IO	SPI Chip Select 0	U1
SPI3_CS1	IO	SPI Chip Select 1	T5
SPI3_CS2	IO	SPI Chip Select 2	V12
SPI3_CS3	IO	SPI Chip Select 3	V15
SPI3_D0	IO	SPI Data 0	R6
SPI3_D1	IO	SPI Data 1	V4

Table 6-51. MCSPI4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
SPI4_CLK	IO	SPI Clock	B16
SPI4_CS0	IO	SPI Chip Select 0	E16
SPI4_CS1	IO	SPI Chip Select 1	A17
SPI4_CS2	IO	SPI Chip Select 0	B17
SPI4_CS3	IO	SPI Chip Select 2	D18
SPI4_D0	IO	SPI Data 0	A16
SPI4_D1	IO	SPI Data 1	D16

6.3.14.2 MCU Domain

Table 6-52. MCU_MCSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCU_SPI0_CLK	IO	SPI Clock	E6
MCU_SPI0_CS0	IO	SPI Chip Select 0	D6
MCU_SPI0_CS1	IO	SPI Chip Select 1	C6
MCU_SPI0_CS2	IO	SPI Chip Select 2	D8
MCU_SPI0_CS3	IO	SPI Chip Select 3	B8
MCU_SPI0_D0	IO	SPI Data 0	E7
MCU_SPI0_D1	IO	SPI Data 1	B6

Table 6-53. MCU_MCSPI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCU_SPI1_CLK	IO	SPI Clock	D7
MCU_SPI1_CS0	IO	SPI Chip Select 0	A7
MCU_SPI1_CS1	IO	SPI Chip Select 1	B7
MCU_SPI1_CS2	IO	SPI Chip Select 2	E8
MCU_SPI1_CS3	IO	SPI Chip Select 3	B9
MCU_SPI1_D0	IO	SPI Data 0	C7
MCU_SPI1_D1	IO	SPI Data 1	C8

6.3.15 MDIO

6.3.15.1 MAIN Domain

Table 6-54. MDIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MDIO0_MDC	O	MDIO Clock	R2, Y6
MDIO0_MDIO	IO	MDIO Data	AA6, P5

6.3.16 MMC

6.3.16.1 MAIN Domain

Table 6-55. MMC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MMC0_CALPAD (1)	A	MMC/SD/SDIO Calibration Resistor	F18
MMC0_CLK	IO	MMC/SD/SDIO Clock	G18
MMC0_CMD	IO	MMC/SD/SDIO Command	J21
MMC0_DS	IO	MMC Data Strobe	G19
MMC0_DAT0	IO	MMC/SD/SDIO Data	K20
MMC0_DAT1	IO	MMC/SD/SDIO Data	J20
MMC0_DAT2	IO	MMC/SD/SDIO Data	J18
MMC0_DAT3	IO	MMC/SD/SDIO Data	J17
MMC0_DAT4	IO	MMC/SD/SDIO Data	H17
MMC0_DAT5	IO	MMC/SD/SDIO Data	H19
MMC0_DAT6	IO	MMC/SD/SDIO Data	H18
MMC0_DAT7	IO	MMC/SD/SDIO Data	G17

(1) An external 10 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

Table 6-56. MMC1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MMC1_CLK (1)	IO	MMC/SD/SDIO Clock	L20
MMC1_CMD	IO	MMC/SD/SDIO Command	J19
MMC1_SDCD	I	SD Card Detect	D19
MMC1_SDWP	I	SD Write Protect	C20
MMC1_DAT0	IO	MMC/SD/SDIO Data	K21
MMC1_DAT1	IO	MMC/SD/SDIO Data	L21
MMC1_DAT2	IO	MMC/SD/SDIO Data	K19
MMC1_DAT3	IO	MMC/SD/SDIO Data	K18

(1) For MMC1_CLK signal to work properly, the RXACTIVE bit of the CTRLMMR_PADCONFIG164 register must remain in its default state of 0x1 because of retiming purposes.

6.3.17 OSPI

6.3.17.1 MAIN Domain

Table 6-57. OSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
OSPI0_CLK	O	OSPI Clock	N20
OSPI0_DQS	I	OSPI Data Strobe (DQS) or Loopback Clock Input	N19
OSPI0_ECC_FAIL	I	OSPI ECC Status	L17
OSPI0_LBCLKO	IO	OSPI Loopback Clock Output	N21
OSPI0_CSn0	O	OSPI Chip Select 0 (active low)	L19
OSPI0_CSn1	O	OSPI Chip Select 1 (active low)	L18
OSPI0_CSn2	O	OSPI Chip Select 2 (active low)	K17
OSPI0_CSn3	O	OSPI Chip Select 3 (active low)	L17
OSPI0_D0	IO	OSPI Data 0	M19
OSPI0_D1	IO	OSPI Data 1	M18
OSPI0_D2	IO	OSPI Data 2	M20
OSPI0_D3	IO	OSPI Data 3	M21
OSPI0_D4	IO	OSPI Data 4	P21
OSPI0_D5	IO	OSPI Data 5	P20
OSPI0_D6	IO	OSPI Data 6	N18
OSPI0_D7	IO	OSPI Data 7	M17
OSPI0_RESET_OUT0	O	OSPI Reset	L17
OSPI0_RESET_OUT1	O	OSPI Reset	K17

6.3.18 Power Supply

Table 6-58. Power Supply Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
CAP_VDDS0 (1)	CAP	External capacitor connection for IO group 0	H12
CAP_VDDS1 (1)	CAP	External capacitor connection for IO group 1	T7
CAP_VDDS2 (1)	CAP	External capacitor connection for IO group 2	R11
CAP_VDDS3 (1)	CAP	External capacitor connection for IO group 3	N14
CAP_VDDS4 (1)	CAP	External capacitor connection for IO group 4	M16
CAP_VDDS5 (1)	CAP	External capacitor connection for IO group 5	L13
CAP_VDDSHV_MMC1 (2)	CAP	External capacitor connection for MMC1	K15
CAP_VDDS_MCU (1)	CAP	External capacitor connection for IO MCU	H10
VDDA_0P85_SERDES0	PWR	SERDES0 0.85 V analog supply	P12, P13
VDDA_0P85_SERDES0_C	PWR	SERDES0 clock 0.85 V analog supply	P11
VDDA_0P85_USB0	PWR	USB0 0.85 V analog supply	T12
VDDA_1P8_SERDES0	PWR	SERDES0 1.8 V analog supply	R14
VDDA_1P8_USB0	PWR	USB0 1.8 V analog supply	R15
VDDA_3P3_SDIO	PWR	SDIO 3.3 V analog supply	H15
VDDA_3P3_USB0	PWR	USB0 3.3 V analog supply	R13
VDDA_ADC	PWR	ADC0 analog supply	J13
VDDA_MCU	PWR	POR and MCU PLL analog supply	K12
VDDA_PLL0	PWR	Main, PER1, and R5F PLL analog supply	N12
VDDA_PLL1	PWR	ARM and DDR PLL analog supply	H9
VDDA_PLL2	PWR	PER0 PLL analog supply	J11
VDDA_TEMP0	PWR	TEMP0 analog supply	G11

Table 6-58. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
VDDA_TEMP1	PWR	TEMP1 analog supply	L11
VDDR_CORE	PWR	RAM supply	L10, M13
VDDSHV0	PWR	IO supply for IO group 0	F11, G12, G14
VDDSHV1	PWR	IO supply for IO group 1	M7, N6, P7
VDDSHV2	PWR	IO supply for IO group 2	R10, R8, T9
VDDSHV3	PWR	IO supply for IO group 3	P14, P15
VDDSHV4	PWR	IO supply for IO group 4	M14, M15
VDDSHV5	PWR	IO supply for IO group 5	L14, L15
VDDSHV_MCU	PWR	IO supply for IO MCU	F9, G10, G8
VDDS_DDR	PWR	DDR PHY IO supply	F7, G6, H7, J6, K7, L6
VDDS_DDR_C	PWR	DDR clock IO supply	J8
VDDS_MMC0	PWR	MMC0 PHY IO supply	K14
VDDS_OSC	PWR	MCU_OSC0 supply	H13
VDD_CORE	PWR	Core supply	J10, J12, K11, K9, L12, L8, M11, M9, N10, N8, P9
VDD_DLL_MMC0	PWR	MMC0 PLL analog supply	H14
VDD_MMC0	PWR	MMC0 PHY core supply	K13
VPP	PWR	eFuse ROM programming supply	G15
VSS	GND	Ground	A1, A21, A5, A6, AA1, AA15, AA18, AA21, C10, C15, C3, D1, E11, E13, F10, F15, F8, G1, G16, G3, G7, G9, H11, H20, H21, H6, H8, J14, J7, J9, K6, K8, L1, L16, L3, L7, L9, M10, M12, M6, M8, N11, N13, N15, N7, N9, P1, P10, P18, P6, P8, R12, R7, R9, T10, T11, T15, T16, T8, U3, V17, W10, W18, Y14, Y17, Y19

(1) This pin must always be connected via a 1-μF capacitor to VSS.
(2) This pin must always be connected via a 3.3-μF ±20% capacitor to VSS when the SDIO_LDO is being used to source VDDSHV5. Otherwise, this pin may be connected directly to VSS when the VDDA_3P3_SDIO pin is also connected directly to VSS.

6.3.19 PRU_ICSSG

Note

The PRU_ICSSG contains a second layer of multiplexing to enable additional functionality on the PRU GPO and GPI signals. This internal wrapper multiplexing is described in the PRU_ICSSG chapter in the device TRM.

6.3.19.1 MAIN Domain

Table 6-59. PRU_ICSSG0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
PRG0_ECAP0_IN_APWM_OUT	IO	PRU-ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	R2, U5
PRG0_ECAP0_SYNC_IN	I	PRU-ICSSG ECAP Sync Input	P5, V5
PRG0_ECAP0_SYNC_OUT	O	PRU-ICSSG ECAP Sync Output	AA4, V5
PRG0_IEP0_EDIO_OUTVALID	O	PRU_ICSSG Industrial Ethernet Digital I/O Outvalid	C13
PRG0_IEP0_EDC_LATCH_IN0	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	V1
PRG0_IEP0_EDC_LATCH_IN1	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	T1
PRG0_IEP0_EDC_SYNC_OUT0	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	W1
PRG0_IEP0_EDC_SYNC_OUT1	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	U1
PRG0_IEP0_EDIO_DATA_IN_OUT28	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	W6
PRG0_IEP0_EDIO_DATA_IN_OUT29	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	AA5
PRG0_IEP0_EDIO_DATA_IN_OUT30	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	Y5
PRG0_IEP0_EDIO_DATA_IN_OUT31	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	V6
PRG0_IEP1_EDC_LATCH_IN0	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	P5
PRG0_IEP1_EDC_LATCH_IN1	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	W5
PRG0_IEP1_EDC_SYNC_OUT0	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	R2
PRG0_IEP1_EDC_SYNC_OUT1	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	V5
PRG0_MDIO0_MDC	O	PRU-ICSSG MDIO Clock	P3
PRG0_MDIO0_MDIO	IO	PRU-ICSSG MDIO Data	P2
PRG0_PRU0_GPI0	I	PRU-ICSSG PRU Data Input	Y1
PRG0_PRU0_GPI1	I	PRU-ICSSG PRU Data Input	R4
PRG0_PRU0_GPI2	I	PRU-ICSSG PRU Data Input	U2
PRG0_PRU0_GPI3	I	PRU-ICSSG PRU Data Input	V2
PRG0_PRU0_GPI4	I	PRU-ICSSG PRU Data Input	AA2
PRG0_PRU0_GPI5	I	PRU-ICSSG PRU Data Input	R3
PRG0_PRU0_GPI6	I	PRU-ICSSG PRU Data Input	T3
PRG0_PRU0_GPI7	I	PRU-ICSSG PRU Data Input	T1
PRG0_PRU0_GPI8	I	PRU-ICSSG PRU Data Input	T2
PRG0_PRU0_GPI9	I	PRU-ICSSG PRU Data Input	W6
PRG0_PRU0_GPI10	I	PRU-ICSSG PRU Data Input	AA5
PRG0_PRU0_GPI11	I	PRU-ICSSG PRU Data Input	Y3
PRG0_PRU0_GPI12	I	PRU-ICSSG PRU Data Input	AA3
PRG0_PRU0_GPI13	I	PRU-ICSSG PRU Data Input	R6
PRG0_PRU0_GPI14	I	PRU-ICSSG PRU Data Input	V4
PRG0_PRU0_GPI15	I	PRU-ICSSG PRU Data Input	T5
PRG0_PRU0_GPI16	I	PRU-ICSSG PRU Data Input	U4

Table 6-59. PRU_ICSSG0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
PRG0_PRU0_GPI17	I	PRU-ICSSG PRU Data Input	U1
PRG0_PRU0_GPI18	I	PRU-ICSSG PRU Data Input	V1
PRG0_PRU0_GPI19	I	PRU-ICSSG PRU Data Input	W1
PRG0_PRU0_GPO0	IO	PRU-ICSSG PRU Data Output	Y1
PRG0_PRU0_GPO1	IO	PRU-ICSSG PRU Data Output	R4
PRG0_PRU0_GPO2	IO	PRU-ICSSG PRU Data Output	U2
PRG0_PRU0_GPO3	IO	PRU-ICSSG PRU Data Output	V2
PRG0_PRU0_GPO4	IO	PRU-ICSSG PRU Data Output	AA2
PRG0_PRU0_GPO5	IO	PRU-ICSSG PRU Data Output	R3
PRG0_PRU0_GPO6	IO	PRU-ICSSG PRU Data Output	T3
PRG0_PRU0_GPO7	IO	PRU-ICSSG PRU Data Output	T1
PRG0_PRU0_GPO8	IO	PRU-ICSSG PRU Data Output	T2
PRG0_PRU0_GPO9	IO	PRU-ICSSG PRU Data Output	W6
PRG0_PRU0_GPO10	IO	PRU-ICSSG PRU Data Output	AA5
PRG0_PRU0_GPO11	IO	PRU-ICSSG PRU Data Output	Y3
PRG0_PRU0_GPO12	IO	PRU-ICSSG PRU Data Output	AA3
PRG0_PRU0_GPO13	IO	PRU-ICSSG PRU Data Output	R6
PRG0_PRU0_GPO14	IO	PRU-ICSSG PRU Data Output	V4
PRG0_PRU0_GPO15	IO	PRU-ICSSG PRU Data Output	T5
PRG0_PRU0_GPO16	IO	PRU-ICSSG PRU Data Output	U4
PRG0_PRU0_GPO17	IO	PRU-ICSSG PRU Data Output	U1
PRG0_PRU0_GPO18	IO	PRU-ICSSG PRU Data Output	V1
PRG0_PRU0_GPO19	IO	PRU-ICSSG PRU Data Output	W1
PRG0_PRU1_GPI0	I	PRU-ICSSG PRU Data Input	Y2
PRG0_PRU1_GPI1	I	PRU-ICSSG PRU Data Input	W2
PRG0_PRU1_GPI2	I	PRU-ICSSG PRU Data Input	V3
PRG0_PRU1_GPI3	I	PRU-ICSSG PRU Data Input	T4
PRG0_PRU1_GPI4	I	PRU-ICSSG PRU Data Input	W3
PRG0_PRU1_GPI5	I	PRU-ICSSG PRU Data Input	P4
PRG0_PRU1_GPI6	I	PRU-ICSSG PRU Data Input	R5
PRG0_PRU1_GPI7	I	PRU-ICSSG PRU Data Input	W5
PRG0_PRU1_GPI8	I	PRU-ICSSG PRU Data Input	R1
PRG0_PRU1_GPI9	I	PRU-ICSSG PRU Data Input	Y5
PRG0_PRU1_GPI10	I	PRU-ICSSG PRU Data Input	V6
PRG0_PRU1_GPI11	I	PRU-ICSSG PRU Data Input	W4
PRG0_PRU1_GPI12	I	PRU-ICSSG PRU Data Input	Y4
PRG0_PRU1_GPI13	I	PRU-ICSSG PRU Data Input	T6
PRG0_PRU1_GPI14	I	PRU-ICSSG PRU Data Input	U6
PRG0_PRU1_GPI15	I	PRU-ICSSG PRU Data Input	U5
PRG0_PRU1_GPI16	I	PRU-ICSSG PRU Data Input	AA4
PRG0_PRU1_GPI17	I	PRU-ICSSG PRU Data Input	V5
PRG0_PRU1_GPI18	I	PRU-ICSSG PRU Data Input	P5
PRG0_PRU1_GPI19	I	PRU-ICSSG PRU Data Input	R2
PRG0_PRU1_GPO0	IO	PRU-ICSSG PRU Data Output	Y2
PRG0_PRU1_GPO1	IO	PRU-ICSSG PRU Data Output	W2

Table 6-59. PRU_ICSSG0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
PRG0_PRU1_GPO2	IO	PRU-ICSSG PRU Data Output	V3
PRG0_PRU1_GPO3	IO	PRU-ICSSG PRU Data Output	T4
PRG0_PRU1_GPO4	IO	PRU-ICSSG PRU Data Output	W3
PRG0_PRU1_GPO5	IO	PRU-ICSSG PRU Data Output	P4
PRG0_PRU1_GPO6	IO	PRU-ICSSG PRU Data Output	R5
PRG0_PRU1_GPO7	IO	PRU-ICSSG PRU Data Output	W5
PRG0_PRU1_GPO8	IO	PRU-ICSSG PRU Data Output	R1
PRG0_PRU1_GPO9	IO	PRU-ICSSG PRU Data Output	Y5
PRG0_PRU1_GPO10	IO	PRU-ICSSG PRU Data Output	V6
PRG0_PRU1_GPO11	IO	PRU-ICSSG PRU Data Output	W4
PRG0_PRU1_GPO12	IO	PRU-ICSSG PRU Data Output	Y4
PRG0_PRU1_GPO13	IO	PRU-ICSSG PRU Data Output	T6
PRG0_PRU1_GPO14	IO	PRU-ICSSG PRU Data Output	U6
PRG0_PRU1_GPO15	IO	PRU-ICSSG PRU Data Output	U5
PRG0_PRU1_GPO16	IO	PRU-ICSSG PRU Data Output	AA4
PRG0_PRU1_GPO17	IO	PRU-ICSSG PRU Data Output	V5
PRG0_PRU1_GPO18	IO	PRU-ICSSG PRU Data Output	P5
PRG0_PRU1_GPO19	IO	PRU-ICSSG PRU Data Output	R2
PRG0_PWM0_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	V1
PRG0_PWM0_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	W1
PRG0_PWM1_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	P5
PRG0_PWM1_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	R2
PRG0_PWM2_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	T18, V6
PRG0_PWM2_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	R1, U21
PRG0_PWM3_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	P16, W6
PRG0_PWM3_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	R17, Y3
PRG0_PWM0_A0	IO	PRU_ICSSG PWM Output A	AA3
PRG0_PWM0_A1	IO	PRU_ICSSG PWM Output A	V4
PRG0_PWM0_A2	IO	PRU_ICSSG PWM Output A	U4
PRG0_PWM0_B0	IO	PRU_ICSSG PWM Output B	R6
PRG0_PWM0_B1	IO	PRU_ICSSG PWM Output B	T5
PRG0_PWM0_B2	IO	PRU_ICSSG PWM Output B	U1
PRG0_PWM1_A0	IO	PRU_ICSSG PWM Output A	Y4
PRG0_PWM1_A1	IO	PRU_ICSSG PWM Output A	U6
PRG0_PWM1_A2	IO	PRU_ICSSG PWM Output A	AA4
PRG0_PWM1_B0	IO	PRU_ICSSG PWM Output B	T6
PRG0_PWM1_B1	IO	PRU_ICSSG PWM Output B	U5
PRG0_PWM1_B2	IO	PRU_ICSSG PWM Output B	V5
PRG0_PWM2_A0	IO	PRU_ICSSG PWM Output A	U2, U20
PRG0_PWM2_A1	IO	PRU_ICSSG PWM Output A	T2, U19
PRG0_PWM2_A2	IO	PRU_ICSSG PWM Output A	V19, V3
PRG0_PWM2_B0	IO	PRU_ICSSG PWM Output B	AA2, U18
PRG0_PWM2_B1	IO	PRU_ICSSG PWM Output B	AA5, V20
PRG0_PWM2_B2	IO	PRU_ICSSG PWM Output B	T17, W3
PRG0_PWM3_A0	IO	PRU_ICSSG PWM Output A	V18, Y1

Table 6-59. PRU_ICSSG0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
PRG0_PWM3_A1	IO	PRU_ICSSG PWM Output A	R18, T3
PRG0_PWM3_A2	IO	PRU_ICSSG PWM Output A	T19, V2
PRG0_PWM3_B0	IO	PRU_ICSSG PWM Output B	R4, Y21
PRG0_PWM3_B1	IO	PRU_ICSSG PWM Output B	T1, T21
PRG0_PWM3_B2	IO	PRU_ICSSG PWM Output B	R3, W19
PRG0_RGMII1_RXC	I	PRU_ICSSG RGMII Receive Clock	T3
PRG0_RGMII1_RX_CTL	I	PRU_ICSSG RGMII Receive Control	AA2
PRG0_RGMII1_TXC	IO	PRU_ICSSG RGMII Transmit Clock	U4
PRG0_RGMII1_TX_CTL	O	PRU_ICSSG RGMII Transmit Control	T5
PRG0_RGMII2_RXC	I	PRU_ICSSG RGMII Receive Clock	R5
PRG0_RGMII2_RX_CTL	I	PRU_ICSSG RGMII Receive Control	W3
PRG0_RGMII2_TXC	IO	PRU_ICSSG RGMII Transmit Clock	AA4
PRG0_RGMII2_TX_CTL	O	PRU_ICSSG RGMII Transmit Control	U5
PRG0_RGMII1_RD0	I	PRU_ICSSG RGMII Receive Data	Y1
PRG0_RGMII1_RD1	I	PRU_ICSSG RGMII Receive Data	R4
PRG0_RGMII1_RD2	I	PRU_ICSSG RGMII Receive Data	U2
PRG0_RGMII1_RD3	I	PRU_ICSSG RGMII Receive Data	V2
PRG0_RGMII1_TD0	O	PRU_ICSSG RGMII Transmit Data	Y3
PRG0_RGMII1_TD1	O	PRU_ICSSG RGMII Transmit Data	AA3
PRG0_RGMII1_TD2	O	PRU_ICSSG RGMII Transmit Data	R6
PRG0_RGMII1_TD3	O	PRU_ICSSG RGMII Transmit Data	V4
PRG0_RGMII2_RD0	I	PRU_ICSSG RGMII Receive Data	Y2
PRG0_RGMII2_RD1	I	PRU_ICSSG RGMII Receive Data	W2
PRG0_RGMII2_RD2	I	PRU_ICSSG RGMII Receive Data	V3
PRG0_RGMII2_RD3	I	PRU_ICSSG RGMII Receive Data	T4
PRG0_RGMII2_TD0	O	PRU_ICSSG RGMII Transmit Data	W4
PRG0_RGMII2_TD1	O	PRU_ICSSG RGMII Transmit Data	Y4
PRG0_RGMII2_TD2	O	PRU_ICSSG RGMII Transmit Data	T6
PRG0_RGMII2_TD3	O	PRU_ICSSG RGMII Transmit Data	U6
PRG0_UART0_CTSn	I	PRU-ICSSG UART Clear to Send (active low)	W6
PRG0_UART0_RTSn	O	PRU-ICSSG UART Request to Send (active low)	AA5
PRG0_UART0_RXD	I	PRU-ICSSG UART Receive Data	Y5
PRG0_UART0_TXD	O	PRU-ICSSG UART Transmit Data	V6

Table 6-60. PRU_ICSSG1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
PRG1_ECAP0_IN_APWM_OUT	IO	PRU-ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	V12
PRG1_ECAP0_SYNC_IN	I	PRU-ICSSG ECAP Sync Input	Y13
PRG1_ECAP0_SYNC_OUT	O	PRU-ICSSG ECAP Sync Output	AA14
PRG1_IEP0_EDIO_OUTVALID	O	PRU_ICSSG Industrial Ethernet Digital I/O Outvalid	D14
PRG1_IEP0_EDC_LATCH_IN0	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	V7
PRG1_IEP0_EDC_LATCH_IN1	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	U13

Table 6-60. PRU_ICSSG1 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
PRG1_IEP0_EDC_SYNC_OUT0	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	W7
PRG1_IEP0_EDC_SYNC_OUT1	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	U7
PRG1_IEP0_EDIO_DATA_IN_OUT28	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/ Output	U15
PRG1_IEP0_EDIO_DATA_IN_OUT29	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/ Output	U14
PRG1_IEP0_EDIO_DATA_IN_OUT30	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/ Output	V14
PRG1_IEP0_EDIO_DATA_IN_OUT31	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/ Output	W14
PRG1_IEP1_EDC_LATCH_IN0	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	Y13
PRG1_IEP1_EDC_LATCH_IN1	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	V15
PRG1_IEP1_EDC_SYNC_OUT0	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	V12
PRG1_IEP1_EDC_SYNC_OUT1	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	AA14
PRG1_MDIO0_MDC	O	PRU-ICSSG MDIO Clock	Y6
PRG1_MDIO0_MDIO	IO	PRU-ICSSG MDIO Data	AA6
PRG1_PRU0_GPI0	I	PRU-ICSSG PRU Data Input	Y7
PRG1_PRU0_GPI1	I	PRU-ICSSG PRU Data Input	U8
PRG1_PRU0_GPI2	I	PRU-ICSSG PRU Data Input	W8
PRG1_PRU0_GPI3	I	PRU-ICSSG PRU Data Input	V8
PRG1_PRU0_GPI4	I	PRU-ICSSG PRU Data Input	Y8
PRG1_PRU0_GPI5	I	PRU-ICSSG PRU Data Input	V13
PRG1_PRU0_GPI6	I	PRU-ICSSG PRU Data Input	AA7
PRG1_PRU0_GPI7	I	PRU-ICSSG PRU Data Input	U13
PRG1_PRU0_GPI8	I	PRU-ICSSG PRU Data Input	W13
PRG1_PRU0_GPI9	I	PRU-ICSSG PRU Data Input	U15
PRG1_PRU0_GPI10	I	PRU-ICSSG PRU Data Input	U14
PRG1_PRU0_GPI11	I	PRU-ICSSG PRU Data Input	AA8
PRG1_PRU0_GPI12	I	PRU-ICSSG PRU Data Input	U9
PRG1_PRU0_GPI13	I	PRU-ICSSG PRU Data Input	W9
PRG1_PRU0_GPI14	I	PRU-ICSSG PRU Data Input	AA9
PRG1_PRU0_GPI15	I	PRU-ICSSG PRU Data Input	Y9
PRG1_PRU0_GPI16	I	PRU-ICSSG PRU Data Input	V9
PRG1_PRU0_GPI17	I	PRU-ICSSG PRU Data Input	U7
PRG1_PRU0_GPI18	I	PRU-ICSSG PRU Data Input	V7
PRG1_PRU0_GPI19	I	PRU-ICSSG PRU Data Input	W7
PRG1_PRU0_GPO0	IO	PRU-ICSSG PRU Data Output	Y7
PRG1_PRU0_GPO1	IO	PRU-ICSSG PRU Data Output	U8
PRG1_PRU0_GPO2	IO	PRU-ICSSG PRU Data Output	W8
PRG1_PRU0_GPO3	IO	PRU-ICSSG PRU Data Output	V8
PRG1_PRU0_GPO4	IO	PRU-ICSSG PRU Data Output	Y8
PRG1_PRU0_GPO5	IO	PRU-ICSSG PRU Data Output	V13

Table 6-60. PRU_ICSSG1 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
PRG1_PRU0_GPO6	IO	PRU-ICSSG PRU Data Output	AA7
PRG1_PRU0_GPO7	IO	PRU-ICSSG PRU Data Output	U13
PRG1_PRU0_GPO8	IO	PRU-ICSSG PRU Data Output	W13
PRG1_PRU0_GPO9	IO	PRU-ICSSG PRU Data Output	U15
PRG1_PRU0_GPO10	IO	PRU-ICSSG PRU Data Output	U14
PRG1_PRU0_GPO11	IO	PRU-ICSSG PRU Data Output	AA8
PRG1_PRU0_GPO12	IO	PRU-ICSSG PRU Data Output	U9
PRG1_PRU0_GPO13	IO	PRU-ICSSG PRU Data Output	W9
PRG1_PRU0_GPO14	IO	PRU-ICSSG PRU Data Output	AA9
PRG1_PRU0_GPO15	IO	PRU-ICSSG PRU Data Output	Y9
PRG1_PRU0_GPO16	IO	PRU-ICSSG PRU Data Output	V9
PRG1_PRU0_GPO17	IO	PRU-ICSSG PRU Data Output	U7
PRG1_PRU0_GPO18	IO	PRU-ICSSG PRU Data Output	V7
PRG1_PRU0_GPO19	IO	PRU-ICSSG PRU Data Output	W7
PRG1_PRU1_GPI0	I	PRU-ICSSG PRU Data Input	W11
PRG1_PRU1_GPI1	I	PRU-ICSSG PRU Data Input	V11
PRG1_PRU1_GPI2	I	PRU-ICSSG PRU Data Input	AA12
PRG1_PRU1_GPI3	I	PRU-ICSSG PRU Data Input	Y12
PRG1_PRU1_GPI4	I	PRU-ICSSG PRU Data Input	W12
PRG1_PRU1_GPI5	I	PRU-ICSSG PRU Data Input	AA13
PRG1_PRU1_GPI6	I	PRU-ICSSG PRU Data Input	U11
PRG1_PRU1_GPI7	I	PRU-ICSSG PRU Data Input	V15
PRG1_PRU1_GPI8	I	PRU-ICSSG PRU Data Input	U12
PRG1_PRU1_GPI9	I	PRU-ICSSG PRU Data Input	V14
PRG1_PRU1_GPI10	I	PRU-ICSSG PRU Data Input	W14
PRG1_PRU1_GPI11	I	PRU-ICSSG PRU Data Input	AA10
PRG1_PRU1_GPI12	I	PRU-ICSSG PRU Data Input	V10
PRG1_PRU1_GPI13	I	PRU-ICSSG PRU Data Input	U10
PRG1_PRU1_GPI14	I	PRU-ICSSG PRU Data Input	AA11
PRG1_PRU1_GPI15	I	PRU-ICSSG PRU Data Input	Y11
PRG1_PRU1_GPI16	I	PRU-ICSSG PRU Data Input	Y10
PRG1_PRU1_GPI17	I	PRU-ICSSG PRU Data Input	AA14
PRG1_PRU1_GPI18	I	PRU-ICSSG PRU Data Input	Y13
PRG1_PRU1_GPI19	I	PRU-ICSSG PRU Data Input	V12
PRG1_PRU1_GPO0	IO	PRU-ICSSG PRU Data Output	W11
PRG1_PRU1_GPO1	IO	PRU-ICSSG PRU Data Output	V11
PRG1_PRU1_GPO2	IO	PRU-ICSSG PRU Data Output	AA12
PRG1_PRU1_GPO3	IO	PRU-ICSSG PRU Data Output	Y12
PRG1_PRU1_GPO4	IO	PRU-ICSSG PRU Data Output	W12
PRG1_PRU1_GPO5	IO	PRU-ICSSG PRU Data Output	AA13
PRG1_PRU1_GPO6	IO	PRU-ICSSG PRU Data Output	U11
PRG1_PRU1_GPO7	IO	PRU-ICSSG PRU Data Output	V15
PRG1_PRU1_GPO8	IO	PRU-ICSSG PRU Data Output	U12
PRG1_PRU1_GPO9	IO	PRU-ICSSG PRU Data Output	V14
PRG1_PRU1_GPO10	IO	PRU-ICSSG PRU Data Output	W14

Table 6-60. PRU_ICSSG1 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
PRG1_PRU1_GPO11	IO	PRU-ICSSG PRU Data Output	AA10
PRG1_PRU1_GPO12	IO	PRU-ICSSG PRU Data Output	V10
PRG1_PRU1_GPO13	IO	PRU-ICSSG PRU Data Output	U10
PRG1_PRU1_GPO14	IO	PRU-ICSSG PRU Data Output	AA11
PRG1_PRU1_GPO15	IO	PRU-ICSSG PRU Data Output	Y11
PRG1_PRU1_GPO16	IO	PRU-ICSSG PRU Data Output	Y10
PRG1_PRU1_GPO17	IO	PRU-ICSSG PRU Data Output	AA14
PRG1_PRU1_GPO18	IO	PRU-ICSSG PRU Data Output	Y13
PRG1_PRU1_GPO19	IO	PRU-ICSSG PRU Data Output	V12
PRG1_PWM0_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	V7
PRG1_PWM0_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	W7
PRG1_PWM1_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	Y13
PRG1_PWM1_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	V12
PRG1_PWM2_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	P19, W14
PRG1_PWM2_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	R20, U12
PRG1_PWM3_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	U15
PRG1_PWM3_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	AA8
PRG1_PWM0_A0	IO	PRU_ICSSG PWM Output A	U9
PRG1_PWM0_A1	IO	PRU_ICSSG PWM Output A	AA9
PRG1_PWM0_A2	IO	PRU_ICSSG PWM Output A	V9
PRG1_PWM0_B0	IO	PRU_ICSSG PWM Output B	W9
PRG1_PWM0_B1	IO	PRU_ICSSG PWM Output B	Y9
PRG1_PWM0_B2	IO	PRU_ICSSG PWM Output B	U7
PRG1_PWM1_A0	IO	PRU_ICSSG PWM Output A	V10
PRG1_PWM1_A1	IO	PRU_ICSSG PWM Output A	AA11
PRG1_PWM1_A2	IO	PRU_ICSSG PWM Output A	Y10
PRG1_PWM1_B0	IO	PRU_ICSSG PWM Output B	U10
PRG1_PWM1_B1	IO	PRU_ICSSG PWM Output B	Y11
PRG1_PWM1_B2	IO	PRU_ICSSG PWM Output B	AA14
PRG1_PWM2_A0	IO	PRU_ICSSG PWM Output A	N16, W8
PRG1_PWM2_A1	IO	PRU_ICSSG PWM Output A	P17, W13
PRG1_PWM2_A2	IO	PRU_ICSSG PWM Output A	AA12, V21
PRG1_PWM2_B0	IO	PRU_ICSSG PWM Output B	N17, Y8
PRG1_PWM2_B1	IO	PRU_ICSSG PWM Output B	U14, Y18
PRG1_PWM2_B2	IO	PRU_ICSSG PWM Output B	R16, W12
PRG1_PWM3_A0	IO	PRU_ICSSG PWM Output A	Y7
PRG1_PWM3_A1	IO	PRU_ICSSG PWM Output A	AA7
PRG1_PWM3_A2	IO	PRU_ICSSG PWM Output A	V8
PRG1_PWM3_B0	IO	PRU_ICSSG PWM Output B	U8
PRG1_PWM3_B1	IO	PRU_ICSSG PWM Output B	U13
PRG1_PWM3_B2	IO	PRU_ICSSG PWM Output B	V13
PRG1_RGMII1_RXC	I	PRU_ICSSG RGMII Receive Clock	AA7
PRG1_RGMII1_RX_CTL	I	PRU_ICSSG RGMII Receive Control	Y8
PRG1_RGMII1_TXC	IO	PRU_ICSSG RGMII Transmit Clock	V9
PRG1_RGMII1_TX_CTL	O	PRU_ICSSG RGMII Transmit Control	Y9

Table 6-60. PRU_ICSSG1 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
PRG1_RGMII2_RXC	I	PRU_ICSSG RGMII Receive Clock	U11
PRG1_RGMII2_RX_CTL	I	PRU_ICSSG RGMII Receive Control	W12
PRG1_RGMII2_TXC	IO	PRU_ICSSG RGMII Transmit Clock	Y10
PRG1_RGMII2_TX_CTL	O	PRU_ICSSG RGMII Transmit Control	Y11
PRG1_RGMII1_RD0	I	PRU_ICSSG RGMII Receive Data	Y7
PRG1_RGMII1_RD1	I	PRU_ICSSG RGMII Receive Data	U8
PRG1_RGMII1_RD2	I	PRU_ICSSG RGMII Receive Data	W8
PRG1_RGMII1_RD3	I	PRU_ICSSG RGMII Receive Data	V8
PRG1_RGMII1_TD0	O	PRU_ICSSG RGMII Transmit Data	AA8
PRG1_RGMII1_TD1	O	PRU_ICSSG RGMII Transmit Data	U9
PRG1_RGMII1_TD2	O	PRU_ICSSG RGMII Transmit Data	W9
PRG1_RGMII1_TD3	O	PRU_ICSSG RGMII Transmit Data	AA9
PRG1_RGMII2_RD0	I	PRU_ICSSG RGMII Receive Data	W11
PRG1_RGMII2_RD1	I	PRU_ICSSG RGMII Receive Data	V11
PRG1_RGMII2_RD2	I	PRU_ICSSG RGMII Receive Data	AA12
PRG1_RGMII2_RD3	I	PRU_ICSSG RGMII Receive Data	Y12
PRG1_RGMII2_TD0	O	PRU_ICSSG RGMII Transmit Data	AA10
PRG1_RGMII2_TD1	O	PRU_ICSSG RGMII Transmit Data	V10
PRG1_RGMII2_TD2	O	PRU_ICSSG RGMII Transmit Data	U10
PRG1_RGMII2_TD3	O	PRU_ICSSG RGMII Transmit Data	AA11
PRG1_UART0_CTSn	I	PRU-ICSSG UART Clear to Send (active low)	U15
PRG1_UART0_RTSn	O	PRU-ICSSG UART Request to Send (active low)	U14
PRG1_UART0_RXD	I	PRU-ICSSG UART Receive Data	V14
PRG1_UART0_TXD	O	PRU-ICSSG UART Transmit Data	W14

6.3.20 Reserved

Table 6-61. Reserved Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
RSVD0	N/A	Reserved, must be left unconnected	H16
RSVD1	N/A	Reserved, must be left unconnected	D21
RSVD2	N/A	Reserved, must be left unconnected	G13
RSVD3	N/A	Reserved, must be left unconnected	F17
RSVD4	N/A	Reserved, must be left unconnected	W15
RSVD5	N/A	Reserved, must be left unconnected	V16
RSVD6	N/A	Reserved, must be left unconnected	K2
RSVD7	N/A	Reserved, must be left unconnected	K1
RSVD8	N/A	Reserved, must be left unconnected	F12

6.3.21 SERDES

6.3.21.1 MAIN Domain

Table 6-62. SERDES0 Signal Descriptions

SIGNAL NAME [1] ((2))	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
PCIE0_CLKREQn	IO	PCIE Clock Request Signal	D16
SERDES0_REXT (1)	A	External SerDes PHY Calibration Resistor	T13
SERDES0_REFCLK0N	IO	SerDes PHY Reference Clock Input/Output (negative)	W16

Table 6-62. SERDES0 Signal Descriptions (continued)

SIGNAL NAME [1] ([2])	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
SERDES0_REFCLK0P	IO	SerDes PHY Reference Clock Input/Output (positive)	W17
SERDES0_RX0_N	I	SerDes PHY Differential Receive Data (negative)	Y15
SERDES0_RX0_P	I	SerDes PHY Differential Receive Data (positive)	Y16
SERDES0_TX0_N	O	SerDes PHY Differential Transmit Data (negative)	AA16
SERDES0_TX0_P	O	SerDes PHY Differential Transmit Data (positive)	AA17

(1) An external 3.01 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.
(2) The functionality of these pins is controlled by SERDES0_LN0_CTRL_LANE_FUNC_SEL.

6.3.22 System and Miscellaneous

6.3.22.1 Boot Mode Configuration

6.3.22.1.1 MAIN Domain

Table 6-63. Sysboot Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
BOOTMODE00	I	Bootmode pin 0	T20
BOOTMODE01	I	Bootmode pin 1	U21
BOOTMODE02	I	Bootmode pin 2	T18
BOOTMODE03	I	Bootmode pin 3	U20
BOOTMODE04	I	Bootmode pin 4	U18
BOOTMODE05	I	Bootmode pin 5	U19
BOOTMODE06	I	Bootmode pin 6	V20
BOOTMODE07	I	Bootmode pin 7	V21
BOOTMODE08	I	Bootmode pin 8	V19
BOOTMODE09	I	Bootmode pin 9	T17
BOOTMODE10	I	Bootmode pin 10	R16
BOOTMODE11	I	Bootmode pin 11	W20
BOOTMODE12	I	Bootmode pin 12	W21
BOOTMODE13	I	Bootmode pin 13	V18
BOOTMODE14	I	Bootmode pin 14	Y21
BOOTMODE15	I	Bootmode pin 15	Y20

6.3.22.2 Clock

6.3.22.2.1 MCU Domain

Table 6-64. MCU Clock Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCU_OSC0_XI	I	High frequency oscillator input	C21
MCU_OSC0_XO	O	High frequency oscillator output	B20

6.3.22.3 System

6.3.22.3.1 MAIN Domain

Table 6-65. System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
CLKOUT0	O	RMII Clock Output (50 MHz). This pin is used for clock source to the external PHY and must be routed back to the RMII_REF_CLK pin for proper device operation.	A19, U13
EXTINTn	I	External Interrupt	C19

Table 6-65. System Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
EXT_REFCLK1	I	External clock input to Main Domain, routed to Timer clock muxes as one of the selectable input clock sources for Timer/WDT modules, or as reference clock to MAIN_PLL2 (PER1 PLL)	A19
OBSCLK0	O	Observation clock output for test and debug purposes only	D17
PORz_OUT	O	Main Domain POR status output	E17
RESETSTATz	O	Main Domain warm reset status output	F16
RESET_REQz	I	Main Domain external warm reset request input	E18
SYSCLKOUT0	O	SYSCLK0 output from Main PLL controller (divided by 6) for test and debug purposes only	C17

6.3.22.3.2 MCU Domain

Table 6-66. MCU System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCU_EXT_REFCLK0	I	External system clock input	B7
MCU_OBSCLK0	O	Observation clock output for test and debug purposes only	C6, E10
MCU_PORz	I	MCU Domain cold reset	B21
MCU_RESETSTATz	O	MCU Domain warm reset status output	B13
MCU_RESETz	I	MCU Domain warm reset	B12
MCU_SAFETY_ERRORn	IO	Error signal output from MCU Domain ESM	A20
MCU_SYSCLKOUT0	O	MCU Domain system clock output for test and debug purposes only	C6

6.3.22.4 VMON

Table 6-67. VMON Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
VMON_1P8_MCU	A	Voltage monitor input for 1.8 V MCU power supply	K16
VMON_1P8_SOC	A	Voltage monitor input for 1.8 V SoC power supply	E12
VMON_3P3_MCU	A	Voltage monitor input for 3.3 V MCU power supply	F13
VMON_3P3_SOC	A	Voltage monitor input for 3.3 V SoC power supply	F14
VMON_VSYS	A	Voltage monitor input, fixed 0.45 V (+/-3%) threshold. Use with external precision voltage divider to monitor a higher voltage rail such as the PMIC input supply.	K10

6.3.23 TIMER

6.3.23.1 MAIN Domain

Table 6-68. TIMER Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	C18, K18
TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	B19, K19
TIMER_IO2	IO	Timer Inputs and Outputs (not tied to single timer instance)	A17, L21
TIMER_IO3	IO	Timer Inputs and Outputs (not tied to single timer instance)	B17, K21

Table 6-68. TIMER Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
TIMER_IO4	IO	Timer Inputs and Outputs (not tied to single timer instance)	C17, L20
TIMER_IO5	IO	Timer Inputs and Outputs (not tied to single timer instance)	D17, J19
TIMER_IO6	IO	Timer Inputs and Outputs (not tied to single timer instance)	B16, D19, T1
TIMER_IO7	IO	Timer Inputs and Outputs (not tied to single timer instance)	A16, C20, U7
TIMER_IO8	IO	Timer Inputs and Outputs (not tied to single timer instance)	P19, V7
TIMER_IO9	IO	Timer Inputs and Outputs (not tied to single timer instance)	R21, W7
TIMER_IO10	IO	Timer Inputs and Outputs (not tied to single timer instance)	C13, U13
TIMER_IO11	IO	Timer Inputs and Outputs (not tied to single timer instance)	D14, U1

6.3.23.2 MCU Domain

Table 6-69. MCU_TIMER Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCU_TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	D8
MCU_TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	E8
MCU_TIMER_IO2	IO	Timer Inputs and Outputs (not tied to single timer instance)	B8
MCU_TIMER_IO3	IO	Timer Inputs and Outputs (not tied to single timer instance)	B9

6.3.24 UART

6.3.24.1 MAIN Domain

Table 6-70. UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
UART0_CTSn	I	UART Clear to Send (active low)	B16
UART0_DCDn	I	UART Data Carrier Detect (active low)	C17
UART0_DSRn	I	UART Data Set Ready (active low)	D17
UART0_DTRn	O	UART Data Terminal Ready (active low)	A17
UART0_RIn	I	UART Ring Indicator	B17
UART0_RTSn	O	UART Request to Send (active low)	A16
UART0_RXD	I	UART Receive Data	D15
UART0_TXD	O	UART Transmit Data	C16

Table 6-71. UART1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
UART1_CTSn	I	UART Clear to Send (active low)	D16
UART1_RTSn	O	UART Request to Send (active low)	E16
UART1_RXD	I	UART Receive Data	E15
UART1_TXD	O	UART Transmit Data	E14

Table 6-72. UART2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
UART2_CTSn	I	UART Clear to Send (active low)	L20, V19, Y1
UART2_RTSn	O	UART Request to Send (active low)	J19, T18, U2
UART2_RXD	I	UART Receive Data	B16, K18, T20, V1, W6
UART2_TXD	O	UART Transmit Data	A16, K19, R4, U21

Table 6-73. UART3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
UART3_CTSn	I	UART Clear to Send (active low)	D19, T17, V2
UART3_RTSn	O	UART Request to Send (active low)	C20, R3, U19
UART3_RXD	I	UART Receive Data	AA5, D16, L21, U20, W1
UART3_TXD	O	UART Transmit Data	AA2, E16, K21, U18

Table 6-74. UART4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
UART4_CTSn	I	UART Clear to Send (active low)	R16, R5, T3, V1
UART4_RTSn	O	UART Request to Send (active low)	R1, R17, T2, W1
UART4_RXD	I	UART Receive Data	A17, L20, V20, W4, Y3
UART4_TXD	O	UART Transmit Data	B17, J19, T1, V21, W5, Y4

Table 6-75. UART5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
UART5_CTSn	I	UART Clear to Send (active low)	W20, Y13, Y2
UART5_RTSn	O	UART Request to Send (active low)	T21, V12, V3
UART5_RXD	I	UART Receive Data	C17, D19, P16, T6, Y5
UART5_TXD	O	UART Transmit Data	C20, D17, R18, W2

Table 6-76. UART6 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
UART6_CTSn	I	UART Clear to Send (active low)	T4, W21
UART6_RTSn	O	UART Request to Send (active low)	P17, P4
UART6_RXD	I	UART Receive Data	C13, U6, V6, Y21
UART6_TXD	O	UART Transmit Data	D14, W3, Y20

6.3.24.2 MCU Domain

Table 6-77. MCU_UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCU_UART0_CTSn	I	UART Clear to Send (active low)	D8
MCU_UART0_RTSn	O	UART Request to Send (active low)	E8
MCU_UART0_RXD	I	UART Receive Data	A9

Table 6-77. MCU_UART0 Signal Descriptions (continued)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCU_UART0_TXD	O	UART Transmit Data	A8

Table 6-78. MCU_UART1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
MCU_UART1_CTSn	I	UART Clear to Send (active low)	B8
MCU_UART1_RTSn	O	UART Request to Send (active low)	B9
MCU_UART1_RXD	I	UART Receive Data	C9
MCU_UART1_TXD	O	UART Transmit Data	D9

6.3.25 USB

6.3.25.1 MAIN Domain

Table 6-79. USB0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	ALV PIN [4]
USB0_DM	IO	USB 2.0 Differential Data (negative)	AA20
USB0_DP	IO	USB 2.0 Differential Data (positive)	AA19
USB0_DRVVBUS	O	USB VBUS control output (active high)	E19
USB0_ID	A	USB 2.0 Dual-Role Device Role Select	U16
USB0_RCALIB (1)	A	Pin to connect to calibration resistor	U17
USB0_VBUS (2)	A	USB Level-shifted VBUS Input	T14

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS. The maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.

(2) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see Section 9.2.3, *USB VBUS Design Guidelines*.

6.4 Pin Connectivity Requirements

This section describes connectivity requirements for package balls that have specific connectivity requirements and unused package balls.

Note

All power balls must be supplied with the voltages specified in the *Recommended Operating Conditions* section, unless otherwise specified.

Note

For additional clarification, "leave unconnected" or "no connect" (NC) means **no** signal traces can be connected to these device ball numbers.

Table 6-80. Connectivity Requirements

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
A20 D11	MCU_SAFETY_ERRORn TRSTn	Each of these balls must be connected to VSS through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic low level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-down can be used to hold a valid logic low level if no PCB signal trace is connected to the ball.
D10 E10 B12 E18 B11 C11 C12	EMU0 EMU1 MCU_RESETz RESET_REQz TCK TDI TMS	Each of these balls must be connected to the corresponding power supply(1) through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-up can be used to hold a valid logic high level if no PCB signal trace is connected to the ball.
A18 B18 E9 A10	I2C0_SCL I2C0_SDA MCU_I2C0_SCL MCU_I2C0_SDA	Each of these balls must be connected to the corresponding power supply(1) through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high level.
T20 U21 T18 U20 U18 U19 V20 V21 V19 T17 R16 W20 W21 V18 Y21 Y20	GPMC0_AD0 GPMC0_AD1 GPMC0_AD2 GPMC0_AD3 GPMC0_AD4 GPMC0_AD5 GPMC0_AD6 GPMC0_AD7 GPMC0_AD8 GPMC0_AD9 GPMC0_AD10 GPMC0_AD11 GPMC0_AD12 GPMC0_AD13 GPMC0_AD14 GPMC0_AD15	Each of these balls must be connected to the corresponding power supply(1) or VSS through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high or low level as appropriate to select the desired device boot mode.
J13 G20 F20 E21, D20 G21 F21 F19 E20 J15 J16	VDDA_ADC ADC0_AIN0 ADC0_AIN1 ADC0_AIN2 ADC0_AIN3 ADC0_AIN4 ADC0_AIN5 ADC0_AIN6 ADC0_AIN7 ADC0_REFP ADC0_REFN	If the entire ADC0 is not used, each of these balls must be connected directly to VSS.

Table 6-80. Connectivity Requirements (continued)

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
G20 F20 E21, D20 G21 F21 F19 E20	ADC0_AIN0 ADC0_AIN1 ADC0_AIN2 ADC0_AIN3 ADC0_AIN4 ADC0_AIN5 ADC0_AIN6 ADC0_AIN7	Any unused ADC0_AIN[7:0] ball must be pulled to VSS through a resistor or connected directly to VSS when VDDA_ADC is connected to a power source.
F7 G6 H7 J6, K7 L6 J8	VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR_C	If DDRSS0 is not used, each of these balls must be connected directly to VSS.

Table 6-80. Connectivity Requirements (continued)

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
H2 H1 J5 K5 F6 H4 D2 C5 E2 D4 D3 F2 J2 L5 J3 J4 K3 J1 M5 K4 G4 G5 G2 H3 H5 F1 E1 F4 F3 E3 E4 B2 M2 A3 A2 B5 A4 B3 C4 C2 B4 N5 L4 L2 M3 N4 N3 M4 N2 C1 B1 N1 M1 E5 F5 D5	DDR0_ACT_n DDR0_ALERT_n DDR0_CAS_n DDR0_PAR DDR0_RAS_n DDR0_WE_n DDR0_A0 DDR0_A1 DDR0_A2 DDR0_A3 DDR0_A4 DDR0_A5 DDR0_A6 DDR0_A7 DDR0_A8 DDR0_A9 DDR0_A10 DDR0_A11 DDR0_A12 DDR0_A13 DDR0_BA0 DDR0_BA1 DDR0_BG0 DDR0_BG1 DDR0_CAL0 DDR0_CK0 DDR0_CK0_n DDR0_CKE0 DDR0_CKE1 DDR0_CS0_n DDR0_CS1_n DDR0_DM0 DDR0_DM1 DDR0_DQ0 DDR0_DQ1 DDR0_DQ2 DDR0_DQ3 DDR0_DQ4 DDR0_DQ5 DDR0_DQ6 DDR0_DQ7 DDR0_DQ8 DDR0_DQ9 DDR0_DQ10 DDR0_DQ11 DDR0_DQ12 DDR0_DQ13 DDR0_DQ14 DDR0_DQ15 DDR0_DQS0 DDR0_DQS0_n DDR0_DQS1 DDR0_DQS1_n DDR0_ODT0 DDR0_ODT1 DDR0_RESET0_n	If DDRSS0 is not used, leave unconnected. Note: The DDR0 pins in this list can only be left unconnected when VDDS_DDR and VDDS_DDR_C are connected to VSS. The DDR0 pins must be connected as defined in the AM64x\AM243x DDR Board Design and Layout Guidelines, when VDDS_DDR and VDDS_DDR_C are connected to a power source.
K13 H14	VDD_MMC0 VDD_DLL_MMC0	If MMC0 is not used, each of these balls must be connected to the same power source as VDD_CORE.
K14	VDDS_MMC0	If MMC0 is not used, each of these balls must be connected to any 1.8-V power source that does not violate device power supply sequencing requirements.

Table 6-80. Connectivity Requirements (continued)

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
F18 G18 J21 G19 K20 J20 J18 J17 H17 H19 H18 G17	MMC0_CALPAD MMC0_CLK MMC0_CMD MMC0_DS MMC0_DAT0 MMC0_DAT1 MMC0_DAT2 MMC0_DAT3 MMC0_DAT4 MMC0_DAT5 MMC0_DAT6 MMC0_DAT7	If MMC0 is not used, each of these balls must be left unconnected.
H15 K15	VDDA_3P3_SDIO CAP_VDDSHV_MMC1	If SDIO_LDO is not used to power VDDSHV5, each of these balls must be connected directly to VSS.
P12 P13 P11 R14	VDDA_0P85_SERDES0 VDDA_0P85_SERDES0 VDDA_0P85_SERDES0_C VDDA_1P8_SERDES0	If SERDES0 is not used and the device boundary scan function is required, each of these balls must be connected to valid power sources. If SERDES0 is not used and the device boundary scan function is not required, each of these balls can alternatively be connected directly to VSS.
T13 W16 W17 Y15 Y16 AA16 AA17	SERDES0_REXT SERDES0_REFCLK0N SERDES0_REFCLK0P SERDES0_RX0_N SERDES0_RX0_P SERDES0_TX0_N SERDES0_TX0_P	If SERDES0 is not used, leave unconnected. Note: The SERDES0_REXT pin can only be left unconnected when VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C, and VDDA_1P8_SERDES0 are connected to VSS. The SERDES0_REXT pin must be connected to VSS through the appropriate external resistor when VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C, and VDDA_1P8_SERDES0 are connected to power sources.
T12 R15 R13	VDDA_0P85_USB0 VDDA_1P8_USB0 VDDA_3P3_USB0	If USB0 is not used, each of these balls must be connected directly to VSS.
AA20 AA19 U16 U17 T14	USB0_DM USB0_DP USB0_ID USB0_RCALIB USB0_VBUS	If USB0 is not used, leave unconnected. Note: The USB0_RCALIB pin can only be left unconnected when VDDA_0P85_USB0, VDDA_1P8_USB0, and VDDA_3P3_USB0 are connected to VSS. The USB0_RCALIB pin must be connected to VSS through the appropriate external resistor when VDDA_0P85_USB0, VDDA_1P8_USB0, and VDDA_3P3_USB0 are connected to power sources.
K10	VMON_VSYS	If VMON_VSYS is not used, this ball must be connected directly to VSS.
K16 E12 F13 F14	VMON_1P8_MCU VMON_1P8_SOC VMON_3P3_MCU VMON_3P3_SOC	If VMON_1P8_MCU, VMON_1P8_SOC, VMON_3P3_MCU, and VMON_3P3_SOC are not used to monitor the MCU and SOC power rails, these balls must still be connected to their respective 1.8-V and 3.3-V power rails.

(1) To determine which power supply is associated with any IO, see the POWER column of the *Pin Attributes* table.

Note

Internal pull resistors are weak and may not source enough current to maintain a valid logic level for some operating conditions. This can be the case when connected to components with leakage to the opposite logic level, or when external noise sources couple to signal traces attached to balls which are only pulled to a valid logic level by the internal resistor. Therefore, external pull resistors are recommended to hold a valid logic level on balls with external connections.

Many of the device IOs are turned off by default and external pull resistors may be required to hold inputs of any attached device in a valid logic state until software initializes the respective IOs. The state of configurable device IOs are defined in the BALL STATE DURING RESET RX/TX/PULL and BALL STATE AFTER RESET RX/TX/PULL columns of the *Pin Attributes* table. Any IO with its input buffer (RX) turned off is allowed to float without damaging the device. However, any IO with its input buffer (RX) turned on shall never be allowed to float to any potential between V_{ILSS} and V_{IHSS}. The input buffer can enter a high-current state which could damage the IO cell if allowed to float between these levels.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)(2)

PARAMETER		MIN	MAX	UNIT
VDD_CORE	Core supply	-0.3	1.05	V
VDDR_CORE	RAM supply	-0.3	1.05	V
VDD_MMC0	MMC0 PHY core supply	-0.3	1.05	V
VDD_DLL_MMC0	MMC0 PLL analog supply	-0.3	1.05	V
VDDA_0P85_SERDES0	SERDES0 0.85-V analog supply	-0.3	1.05	V
VDDA_0P85_SERDES0_C	SERDES0 clock 0.85-V analog supply	-0.3	1.05	V
VDDA_0P85_USB0	USB0 0.85-V analog supply	-0.3	1.05	V
VDDS_DDR	DDR PHY IO supply	-0.3	1.57	V
VDDS_DDR_C	DDR clock IO supply	-0.3	1.57	V
VDDS_MMC0	MMC0 PHY IO supply	-0.3	1.98	V
VDDS_OSC	MCU_OSC0 supply	-0.3	1.98	V
VDDA_MCU	POR and MCU PLL analog supply	-0.3	1.98	V
VDDA_ADC0	ADC0 analog supply	-0.3	1.98	V
VDDA_PLL0	Main, PER1, and R5F PLL analog supply	-0.3	1.98	V
VDDA_PLL1	ARM and DDR PLL analog supply	-0.3	1.98	V
VDDA_PLL2	PER0 PLL analog supply	-0.3	1.98	V
VDDA_1P8_SERDES0	SERDES0 1.8-V analog supply	-0.3	1.98	V
VDDA_1P8_USB0	USB0 1.8-V analog supply	-0.3	1.98	V
VDDA_TEMP0	TEMP0 analog supply	-0.3	1.98	V
VDDA_TEMP1	TEMP1 analog supply	-0.3	1.98	V
VPP	eFuse ROM programming supply	-0.3	1.98	V
VDDSHV_MCU	IO supply for IO MCU	-0.3	3.63	V
VDDSHV0	IO supply for IO group 0	-0.3	3.63	V
VDDSHV1	IO supply for IO group 1	-0.3	3.63	V
VDDSHV2	IO supply for IO group 2	-0.3	3.63	V
VDDSHV3	IO supply for IO group 3	-0.3	3.63	V
VDDSHV4	IO supply for IO group 4	-0.3	3.63	V
VDDSHV5	IO supply for IO group 5	-0.3	3.63	V
VDDA_3P3_USB0	USB0 3.3-V analog supply	-0.3	3.63	V
VDDA_3P3_SDIO	SDIO 3.3-V analog supply	-0.3	3.63	V
Steady-state max voltage at all fail-safe IO pins	MCU_PORz	-0.3	3.63	V
	MCU_I2C0_SCL, MCU_I2C0_SDA, I2C0_SCL, I2C0_SDA, and EXTINTn When operating at 1.8V	-0.3	1.98(3)	V
	MCU_I2C0_SCL, MCU_I2C0_SDA, I2C0_SCL, I2C0_SDA, and EXTINTn When operating at 3.3V	-0.3	3.63(3)	
	VMON_1P8_MCU, and VMON_1P8_SOC	-0.3	1.98	V
	VMON_3P3_MCU, and VMON_3P3_SOC	-0.3	3.63	V
	VMON_VSYS(4)	-0.3	1.98	V

over operating junction temperature range (unless otherwise noted)[1][2]

PARAMETER			MIN	MAX	UNIT
Steady-state max voltage at all other IO pins[5]		USB0_VBUS[6]	-0.3	3.6	V
		USB0_ID[7]	-0.3	3.6	
		All other IO pins	-0.3	IO supply voltage + 0.3	V
Transient overshoot and undershoot at IO pin		20% of IO supply voltage for up to 20% of the signal period (see Figure 7-1, *IO Transient Voltage Ranges*)		0.2 × VDD[8]	V
Latch-up performance[9]		I-Test	-100	+100	mA
		Over-Voltage (OV) Test		1.5 x VDD[8]	V
T_{STG}	Storage temperature		-55	+150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Section 7.4, *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltage values are with respect to VSS, unless otherwise noted.

(3) The absolute maximum ratings for these fail-safe pins depends on their IO supply operating voltage. Therefore, this value is also defined by the maximum V_{IH} value found in the *I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics* section, where the electrical characteristics table has separate parameter values for 1.8-V mode and 3.3-V mode.

(4) The VMON_VSYS pin provides a way to monitor the system power supply. For more information, see Section 9.2.4, *System Power Supply Monitor Design Guidelines*.

(5) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.

(6) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see Section 9.2.3, *USB Design Guidelines*.

(7) The USB0_ID pin is connected to analog circuits in the USB0 PHY. The analog circuits source a known current while measuring voltage, to determine the resistance value (RID), if connected to VSS through a resistor. This pin should be connected to VSS for USB host operation, or left unconnected for USB device operation, and should never be connected to any external voltage source.

(8) VDD is the voltage on the corresponding power-supply pin(s) for the IO.

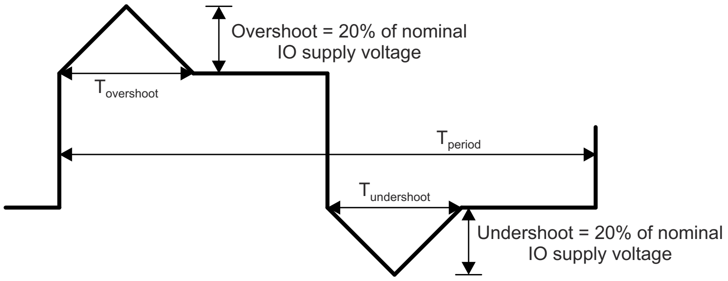
(9) For current pulse injection (I-Test):

- Pins stressed per JEDEC JESD78 (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

For over-voltage performance (Over-Voltage (OV) Test):

- Supplies stressed per JEDEC JESD78 (Class II) and passed specified voltage injection.

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The MCU_I2C0_SCL, MCU_I2C0_SDA, I2C0_SCL, I2C0_SDA, EXTINTn, VMON_1P8_MCU, VMON_1P8_SOC, VMON_3P3_MCU, VMON_3P3_SOC, VMON_VSYS, and MCU_PORz are the only fail-safe IO terminals. All other IO terminals are not fail-safe and the voltage applied to them should be limited to the value defined by the Steady State Max. Voltage at all IO pins parameter in Section 7.1.



A. $T_{overshoot} + T_{undershoot} < 20\%$ of T_{period}

Figure 7-1. IO Transient Voltage Ranges

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Power-On Hours (POH)

POWER ON HOURS (POH)[1] [2] [3]		
JUNCTION TEMPERATURE RANGE (T_J)		**LIFETIME (POH)**
Extended Industrial	–40°C to 105°C	100000

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.
(3) POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH.

7.4 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN[1]	NOM	MAX[1]	UNIT
VDD_CORE	Core supply	0.75-V operation	0.715	0.75	0.79	V
		0.85-V operation	0.81	0.85	0.895	V
VDDR_CORE	RAM supply		0.81	0.85	0.895	V
VDD_MMC0[2]	MMC0 PHY core supply		0.81	0.85	0.895	V
VDD_DLL_MMC0[2]	MMC0 PLL analog supply		0.81	0.85	0.895	V
VDDA_0P85_SERDES0	SERDES0 0.85 V analog supply		0.81	0.85	0.895	V
VDDA_0P85_SERDES0_C	SERDES0 clock 0.85 V analog supply		0.81	0.85	0.895	V
VDDA_0P85_USB0	USB0 0.85 V analog supply		0.81	0.85	0.895	V
VDDS_DDR[3] VDDS_DDR_C[3]	DDR PHY IO supply DDR clock IO supply	1.1-V operation	1.06	1.1	1.17	V
		1.2-V operation	1.14	1.2	1.26	V
VDDS_MMC0	MMC0 PHY IO supply		1.71	1.8	1.89	V
VDDS_OSC	MCU_OSC0 supply		1.71	1.8	1.89	V
VDDA_MCU	POR and MCU PLL analog supply		1.71	1.8	1.89	V
VDDA_ADC0	ADC0 analog supply		1.71	1.8	1.89	V
VDDA_PLL0	Main, PER and R5F PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL1	ARM and DDR PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL2	PER0 PLL analog supply		1.71	1.8	1.89	V
VDDA_1P8_SERDES0	SERDES0 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_1P8_USB0	USB0 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_TEMP0	TEMP0 analog supply		1.71	1.8	1.89	V
VDDA_TEMP1	TEMP1 analog supply		1.71	1.8	1.89	V
VPP	eFuse ROM programming supply		1.71	1.8	1.89	V
VMON_1P8_MCU	Voltage monitor for 1.8 V MCU power supply		1.71	1.8	1.89	V
VMON_1P8_SOC	Voltage monitor for 1.8 V SoC power supply		1.71	1.8	1.89	V
VDDA_3P3_USB0	USB0 3.3 V analog supply		3.135	3.3	3.465	V
VDDA_3P3_SDIO	SDIO 3.3 V analog supply		3.135	3.3	3.465	V
VMON_3P3_MCU	Voltage monitor for 3.3 V MCU power supply		3.135	3.3	3.465	V
VMON_3P3_SOC	Voltage monitor for 3.3 V SoC power supply		3.135	3.3	3.465	V
VMON_VSYS	Voltage monitor pin		0	see[4]	1	V
USB0_VBUS	USB Level-shifted VBUS Input		0	see[5]	3.465	V
USB0_ID	USB0 analog I/O for RID detection			see[6]		V
VDDSHV_MCU	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV0	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV1	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV2	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV3	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV4	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V

over operating junction temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN(1)	NOM	MAX(1)	UNIT
VDDSHV5	Dual-voltage IO supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
T_J	Operating junction temperature range	Automotive	–40		125	°C
		Extended Industrial	–40		105	

(1) The voltage at the device ball must never drop below the MIN voltage or rise above the MAX voltage for any amount of time during normal device operation.
(2) VDD_MMC0 and VDD_DLL_MMC0 must be connected to the same power source as VDD_CORE when MMC0 is not used. In this case, VDD_MMC0 and VDD_DLL_MMC0 may be operated at a nominal voltage of 0.75 or 0.85.
(3) VDDS_DDR and VDDS_DDR_C shall be sourced from the same power source.
(4) The VMON_VSYS pin provides a way to monitor the system power supply. For more information, see Section 9.2.4, *System Power Supply Monitor Design Guidelines*.
(5) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see Section 9.2.3, *USB Design Guidelines*.
(6) The USB0_ID pin is connected to analog circuits in the USB0 PHY. The analog circuits source a known current while measuring voltage, to determine the resistance value (RID), if connected to VSS through a resistor. This pin should be connected to VSS for USB host operation, or left unconnected for USB device operation, and should never be connected to any external voltage source.

7.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each Operating Performance Point (OPP) for processor clocks and device core clocks.

Table 7-1 describes the maximum supported frequency per speed grade for the device.

Table 7-1. Speed Grade Maximum Frequency

DEVICE	MAXIMUM FREQUENCY (MHz)								
	SPEED GRADE	A53SS	R5FSS	M4FSS	CBASS0	ICSSG	DMSC-L	DDR4(1)	LPDDR4(1)
AM64x	S	1000	800	400	250	333	250	800 (DDR-1600)	800 (LPDDR-1600)
AM64x	K	800	400	400	250	250	250	800 (DDR-1600)	800 (LPDDR-1600)

(1) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. Refer to AM64x\AM243x DDR Board Design and Layout Guidelines for the proper PCB implementation to achieve maximum DDR frequency.

7.6 Power Consumption Summary

For information on the device power consumption, see the AM64x/AM243x Power Estimation Tool application note.

7.7 Electrical Characteristics

Note

The interfaces or signals described in Section 7.7.1 through Section 7.7.10 correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

7.7.1 I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8 V MODE						
V_{IL}	Input Low Voltage				0.3 × VDD(1)	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDD(1)	V
V_{IH}	Input High Voltage		0.7 × VDD(1)		1.98(2)	V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDD(1)			V
V_{HYS}	Input Hysteresis Voltage		0.1 × VDD(1)			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0 V			±10	µA
V_{OL}	Output Low Voltage				0.2 × VDD(1)	V
I_{OL} (3)	Low Level Output Current	$V_{OL(MAX)}$	10			mA
SR_I (5)	Input Slew Rate		18f(4) or 1.8E+6			V/s
3.3 V MODE (6)						
V_{IL}	Input Low Voltage				0.3 × VDD(1)	V
V_{ILSS}	Input Low Voltage Steady State				0.25 × VDD(1)	V
V_{IH}	Input High Voltage		0.7 × VDD(1)		3.63(2)	V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDD(1)			V
V_{HYS}	Input Hysteresis Voltage		0.05 × VDD(1)			mV
I_{IN}	Input Leakage Current.	V_I = 3.3 V or V_I = 0 V			±10	µA
V_{OL}	Output Low Voltage				0.4	V
I_{OL} (3)	Low Level Output Current	$V_{OL(MAX)}$	10			mA
SR_I (5)	Input Slew Rate		33f(4) or 3.3E+6		8E+7	V/s

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.
(2) This value also defines the Absolute Maximum Ratings value the IO.
(3) The I_{OL} parameter defines the minimum Low Level Output Current for which the device is able to maintain the specified V_{OL} value. The value defined by this parameter should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} value for attached components.
(4) f = toggle frequency of the input signal in Hz.
(5) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.
(6) I2C Hs-mode is not supported when operating the IO in 3.3 V mode.

7.7.2 Fail-Safe Reset (FS RESET) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.3 × VDDS_OSC	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDDS_OSC	V
V_{IH}	Input High Voltage		0.7 × VDDS_OSC			V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDDS_OSC			V
V_{HYS}	Input Hysteresis Voltage		200			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0 V			±10	μA
SR_I (2)	Input Slew Rate		18f(1) or 1.8E+6			V/s

(1) f = toggle frequency of the input signal in Hz.

(2) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

7.7.3 High-Frequency Oscillator (HFOSC) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.35 × VDDS_OSC	V
V_{IH}	Input High Voltage		0.65 × VDDS_OSC			V
V_{HYS}	Input Hysteresis Voltage			49		mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0.0 V			±10	μA

7.7.4 eMMCPHY Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.35 × VDDS_MMC0	V
V_{ILSS}	Input Low Voltage Steady State				0.20	V
V_{IH}	Input High Voltage		0.65 × VDDS_MMC0			V
V_{IHSS}	Input High Voltage Steady State		1.4			V
I_{IN}	Input Leakage Current.	V_I = 1.8 V or 0 V			±10	μA
R_{PU}	Pull-up Resistor		15	20	25	kΩ
R_{PD}	Pull-down Resistor		15	20	25	kΩ
V_{OL}	Output Low Voltage	I_{OL} = 2 mA			0.30	V
V_{OH}	Output High Voltage	I_{OH} = -2 mA	VDDS_MMC0 - 0.30			V
SR_I	Input Slew Rate		5E+8			V/s

7.7.5 SDIO Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8 V MODE						
V_{IL}	Input Low Voltage				0.58	V
V_{ILSS}	Input Low Voltage Steady State				0.58	V
V_{IH}	Input High Voltage		1.27			V
V_{IHSS}	Input High Voltage Steady State		1.7			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0 V			±10	μA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output Low Voltage				0.45	V
V_{OH}	Output High Voltage		VDDSHV5 - 0.45			V
I_{OL} (1)	Low Level Output Current	$V_{OL(MAX)}$	4			mA
I_{OH} (1)	High Level Output Current	$V_{OH(MIN)}$	4			mA
SR_I (3)	Input Slew Rate		18f(2) or 1.8E+6			V/s
3.3 V MODE						
V_{IL}	Input Low Voltage				0.25 × VDDSHV5	V
V_{ILSS}	Input Low Voltage Steady State				0.15 × VDDSHV5	V
V_{IH}	Input High Voltage		0.625 × VDDSHV5			V
V_{IHSS}	Input High Voltage Steady State		0.625 × VDDSHV5			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 3.3 V or V_I = 0 V			±10	μA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output Low Voltage				0.125 × VDDSHV5	V
V_{OH}	Output High Voltage		0.75 × VDDSHV5			V
I_{OL} (1)	Low Level Output Current	$V_{OL(MAX)}$	6			mA
I_{OH} (1)	High Level Output Current	$V_{OH(MIN)}$	10			mA
SR_I (3)	Input Slew Rate		33f(2) or 3.3E+6			V/s

(1) The I_{OL} and I_{OH} parameters define the minimum Low Level Output Current and High Level Output Current for which the device is able to maintain the specified V_{OL} and V_{OH} values. Values defined by these parameters should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} and V_{OH} values for attached components.

(2) f = toggle frequency of the input signal in Hz.

(3) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

7.7.6 LVCMOS Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8-V MODE						
V_{IL}	Input Low Voltage				0.35 × VDD(1)	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDD(1)	V
V_{IH}	Input High Voltage		0.65 × VDD(1)			V
V_{IHSS}	Input High Voltage Steady State		0.85 × VDD(1)			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0.0 V			±10	μA
R_{PU}	Pull-up Resistor		15	22	30	kΩ
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.45	V
V_{OH}	Output High Voltage		VDD(1) - 0.45			V
I_{OL} (2)	Low Level Output Current	$V_{OL(MAX)}$	3			mA
I_{OH} (2)	High Level Output Current	$V_{OH(MIN)}$	3			mA
SR_I (4)	Input Slew Rate		18f(3) or 1.8E+6			V/s
3.3-V MODE						
V_{IL}	Input Low Voltage				0.8	V
V_{ILSS}	Input Low Voltage Steady State				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{IHSS}	Input High Voltage Steady State		2.0			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 3.3 V or V_I = 0.0 V			±10	μA
R_{PU}	Pull-up Resistor		15	22	30	kΩ
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{OL} (2)	Low Level Output Current	$V_{OL(MAX)}$	5			mA
I_{OH} (2)	High Level Output Current	$V_{OH(MIN)}$	9			mA
SR_I (4)	Input Slew Rate		33f(3) or 3.3E+6			V/s

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.
(2) The I_{OL} and I_{OH} parameters define the minimum Low Level Output Current and High Level Output Current for which the device is able to maintain the specified V_{OL} and V_{OH} values. Values defined by these parameters should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} and V_{OH} values for attached components.
(3) f = toggle frequency of the input signal in Hz.
(4) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

7.7.7 ADC12B Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ADC0_VREFP} (1)	Positive Reference Voltage, ADC0_VREFP		1.71		1.89	V
V_{ADC0_VREFN} (1)	Negative Reference Voltage, ADC0_VREFN			VSS		V
$V_{ADC\_AIN[7:0]}$	Analog Input Voltage, ADC_AIN[7:0], Full-scale		VSS		VDDA_ADC0	V
DNL	Differential Non-Linearity		> -1		+1	LSB
INL	Integral Non-Linearity		-2		+2	LSB
$LSB_{GAIN\text{-}ERROR}$	Gain Error			±10		LSB
$LSB_{OFFSET\text{-}ERROR}$	Offset Error			±5		LSB
SNR	Signal-to-Noise Ratio	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		70		dB
THD	Total Harmonic Distortion	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		-75		dB
$Z_{ADC\_AIN[0:7]}$	Analog Input Impedance, ADC0_AIN[7:0]			(2)		Ω
I_{IN}	Input Leakage			±10		μA
C_{SMPL}	Sampling Capacitance			5.5		pF
Sampling Dynamics						
F_{SMPL_CLK}	ADC0 SMPL_CLK Frequency			60		MHz
t_C	Conversion Time			13		ADC0 SMPL_CLK Cycles
t_{ACQ}	Acquisition Time		2		257	ADC0 SMPL_CLK Cycles
T_R	Sampling Rate	ADC0 SMPL_CLK = 60 MHz			4	MSPS
General Purpose Input Mode (3)						
V_{IL}	Input Low Voltage				0.35 × VDDA_ADC0	V
V_{ILSS}	Input Low Voltage Steady State				0.35 × VDDA_ADC0	V
V_{IH}	Input High Voltage		0.65 × VDDA_ADC0			V
V_{IHSS}	Input High Voltage Steady State		0.65 × VDDA_ADC0			V
V_{HYS}	Input Hysteresis Voltage		200			mV
I_I	Input Leakage Current	ADC0_AIN[7:0] = VDDA_ADC0 or ADC0_AIN[7:0] = VSS			10	μA

(1) The ADC0_REFP and ADC0_REFN reference inputs are analog inputs which must be treated like high transient power supply rails. ADC0_REFN is expected to be connected directly to the PCB ground plane along with all other VSS pins, and ADC0_REFP is connected to a power source capable of providing at least 4 mA of current. ADC0_REFP can be connected to the same power source as VDDA_ADC0 if the voltage tolerance of the supply provides an acceptable accuracy for the ADC reference. A high frequency decoupling capacitor must be connected directly to the ADC0_REFP and ADC0_REFN pins with vias and be placed in the ball array on the back side of the PCB.

(2) The ADC0_AIN pins are connected to an internal sampling capacitor for a user configurable acquisition time and acquisition frequency. The input impedance of the ADC0_AIN pins is a function of the sampling capacitance along with user configurable acquisition time and

acquisition frequency. The designer must understand the time required for the source impedance of each ADC0_AIN pin to charge the internal sampling capacitor. The acquisition time must be set long enough for the internal sampling capacitor to settle to greater than 14 bits of accuracy.

(3) ADC0 can be configured to operate in General Purpose Input mode, where all ADC0_AIN[7:0] inputs are globally enabled to operate as digital inputs via the ADC0_CTRL register (gpi_mode_en = 1).

7.7.8 USB2PHY Electrical Characteristics

Note

USB0 interface is compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

7.7.9 SerDes PHY Electrical Characteristics

Note

The PCIe interface is compliant with the electrical parameters specified in PCI Express® Base Specification Revision 4.0, February 19, 2014.

Note

USB0 instance is compliant with the USB3.1 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the Universal Serial Bus 3.1 Specification, Revision 1.0 , July 26, 2013.

7.7.10 DDR Electrical Characteristics

Note

The DDR interface is compatible with DDR4 devices that are **JESD79-4B standard-compliant**, and LPDDR4 devices that are **JESD209-4B standard-compliant**

7.8 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses..

7.8.1 Recommended Operating Conditions for OTP eFuse Programming

over operating junction temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VDD_CORE	Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)		See *Recommended Operating Conditions*		V
VPP	Supply voltage range for the eFuse ROM domain during normal operation without hardware support to program eFuse ROM		NC[1]		V
	Supply voltage range for the eFuse ROM domain during normal operation with hardware support to program eFuse ROM		0		V
	Supply voltage range for the eFuse ROM domain during OTP programming[2]	1.71	1.8	1.89	V
$I_{(VPP)}$	VPP current			400	mA
$SR_{(VPP)}$	VPP Slew Rate			6E+4	V/s
T_J	Operating junction temperature range while programming eFuse ROM.	0	25	85	°C

(1) NC stands for No Connect.
(2) Supply voltage range includes DC errors and peak-to-peak noise.

7.8.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.
- The VPP power supply must be ramped up after the proper device power-up sequence (for more details, see Section 7.10.2, *Power Supply Sequencing*).

7.8.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP terminal during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP terminal according to the specification in Section 7.8.1.
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP terminal.

7.8.4 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse. CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

7.9 Thermal Resistance Characteristics

For operation and reliability concerns, the maximum junction temperature of the device must be equal to or less than the T_J value identified in *Recommended Operating Conditions*.

7.9.1 Thermal Resistance Characteristics

Table 7-2. Thermal Resistance Characteristics

TI recommends performing system level thermal simulations with worst case device power consumption.

NO.	PARAMETER[1]	DESCRIPTION	°C/W[2]	AIR FLOW (m/s)[3]
ALV Package				
T1	$R\Theta_{JC}$	Junction-to-case	0.98	N/A
T2	$R\Theta_{JB}$	Junction-to-board	3.87	N/A
T3	$R\Theta_{JA}$	Junction-to-free air	12.8	0
T4	$R\Theta_{JA}$	Junction-to-moving air	9.2	1
T5			8.2	2
T6			7.6	3
T7	Ψ_{JT}	Junction-to-package top	0.53	0
T8			0.55	1
T9			0.57	2
T10			0.58	3
T11	Ψ_{JB}	Junction-to-board	3.74	0
T12			3.5	1
T13			3.4	2
T14			3.3	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [RΘJC] value, which is based on a JEDEC defined 1S0P system) and is subject to change based on environment as well as application. For more information, see the EIA/JEDEC standards.
  - JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
  - JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
  - JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
  - JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
  - JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) °C/W = degrees Celsius per watt.

(3) m/s = meters per second.

7.10 Timing and Switching Characteristics

Note

The Timing Requirements and Switching Characteristics values may change following the silicon characterization result.

Note

The default SLEWRATE settings in each pad configuration register must be used to ensure timings, unless specific instructions are given otherwise.

7.10.1 Timing Parameters and Information

The timing parameter symbols used in *Timing and Switching Characteristics* sections are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in Table 7-3:

Table 7-3. Timing Parameters Subscripts

SYMBOL	PARAMETER
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

7.10.2 Power Supply Requirements

This section describes the power supply requirements to ensure proper device operation.

Note

All power balls must be supplied with the voltages specified in the *Recommended Operating Conditions* section, unless otherwise specified in *Signal Descriptions* and *Pin Connectivity Requirements*.

7.10.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 18 mV/µs. For instance, as shown in Figure 7-2, TI recommends having the supply ramp slew for a 1.8-V supply of more than 100 µs.

Figure 7-2 describes the Power Supply Slew Rate Requirement in the device.

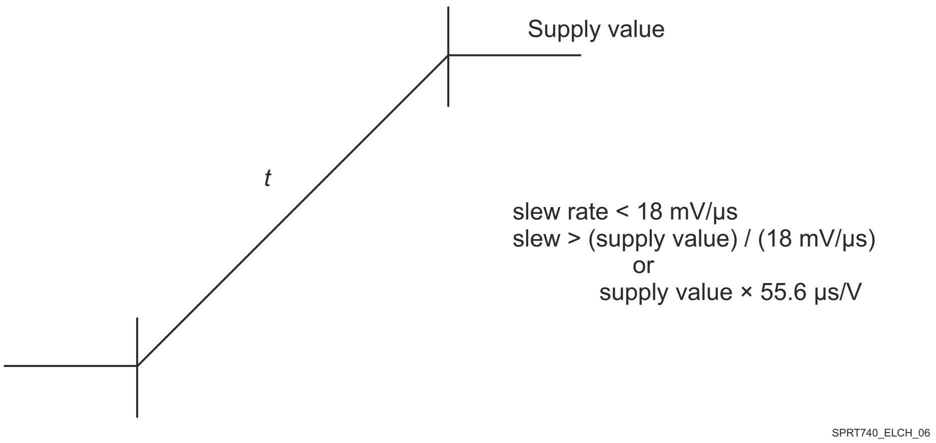


Figure 7-2. Power Supply Slew and Slew Rate

7.10.2.2 Power Supply Sequencing

This section describes power sequence requirements using power sequence diagrams and associated notes. Each power sequence diagram demonstrates the sequential order expected for each device power rail. This is done by assigning each device power rail to one or more waveform. A dual-voltage power rail may be associated with more than one waveform and the associated note will describe which waveform is applicable. Each waveform defines a transition region for the associated power rails and shows its sequential relationship to the transition regions of other power rails. The notes associated with the power sequence diagram provides further detail of these requirements. See the *Power-up Sequence* section for details on power-up requirements, and the *Power-down Sequence* section for details on power-down requirements.

Two types of power supply transition regions are used to simplify the power supply sequencing diagrams. The legends shown in Figure 7-3 and Figure 7-4 along with their descriptions are provided to clarify what each transition regions represents.

Figure 7-3 defines a transition region with multiple power rails which may be sourced from multiple power supplies or a single power supply. Transitions shown within the transition region represent a use case where multiple power supplies are used to source power rails associated with this waveform, and these power supplies are allowed to ramp at different times within the region since they do not have any specific sequence requirement relative to each other.

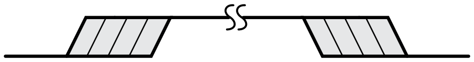


Figure 7-3. Multiple Power Supply Transition Legend

Figure 7-4 defines a transition region with one or more power rails which must be sourced from a single common power supply. No transitions are shown within the region to represent a single ramp within the transition region.

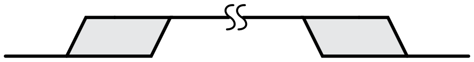


Figure 7-4. Single Common Power Supply Transition Legend

7.10.2.2.1 Power-Up Sequencing

Figure 7-5 describes the device power-up sequencing.

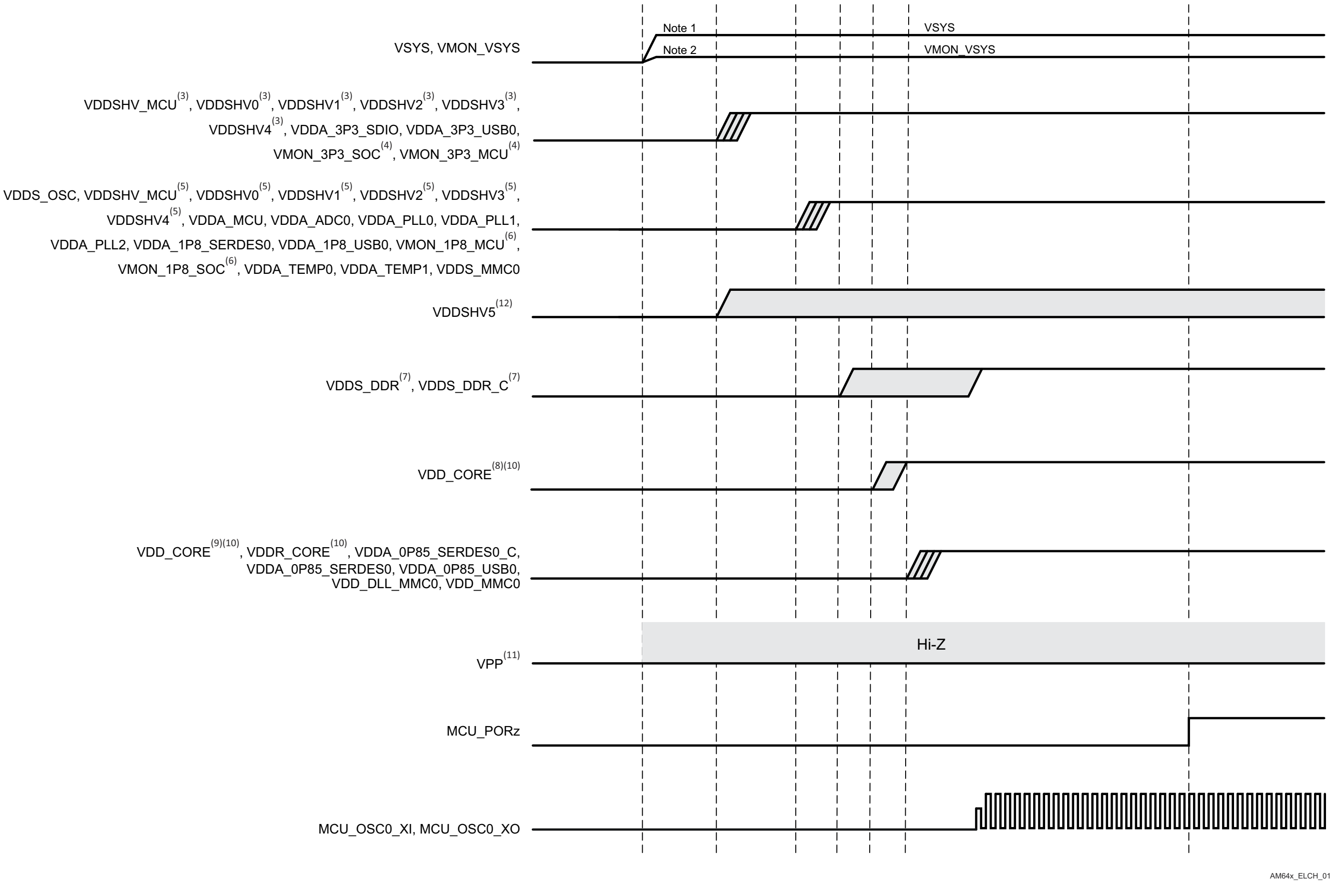


Figure 7-5. Power-Up Sequencing

1. VSYS represents the name of a supply which sources power to the entire system. This supply is expected to be a pre-regulated supply that sources power management devices which source all other supplies.
2. VMON_VSYS input is used to monitor VSYS via an external resistor divider circuit. For more information, see Section 9.2.4, *System Power Supply Monitor Design Guidelines*.
3. VDDSHV_MCU and VDDSHVx [x=0-5] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements. When any of the VDDSHV_MCU or VDDSHVx [x=0-5] IO supplies are operating at 3.3V, they shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.
4. The VMON_3P3_MCU and VMON_3P3_SOC inputs are used to monitor supply voltage and shall be connected to the respective 3.3V supply source.
5. VDDSHV_MCU and VDDSHVx [x=0-5] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements. When any of the VDDSHV_MCU or VDDSHVx [x=0-5] IO supplies are operating at 1.8V, they shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.
6. The VMON_1P8_MCU and VMON_1P8_SOC inputs are used to monitor supply voltage and shall be connected to the respective 1.8V supply source.
7. VDDS_DDR and VDDS_DDR_C are expected to be powered by the same source such that they ramp together.
8. VDD_CORE can be operated at 0.75V or 0.85V. When VDD_CORE is operating at 0.75V, it shall be ramped up prior to all 0.85V supplies as shown in this waveform.
9. VDD_CORE can be operated at 0.75V or 0.85V. When VDD_CORE is operating at 0.85V, it shall be ramped up with other 0.85V supplies during the 0.85V ramp period defined by this waveform.

10. The potential applied to VDDR_CORE must never be greater than the potential applied to VDD_CORE + 0.18V during power-up or power-down. This requires VDD_CORE to ramp up before and ramp down after VDDR_CORE when VDD_CORE is operating at 0.75V. VDD_CORE does not have any ramp requirements beyond the one defined for VDDR_CORE. VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V.
11. VPP is the 1.8V eFuse programming supply, which shall be left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply shall only be sourced while programming eFuse.
12. VDDSHV5 was designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

7.10.2.2.2 Power-Down Sequencing

Figure 7-6 describes the device power-down sequencing.

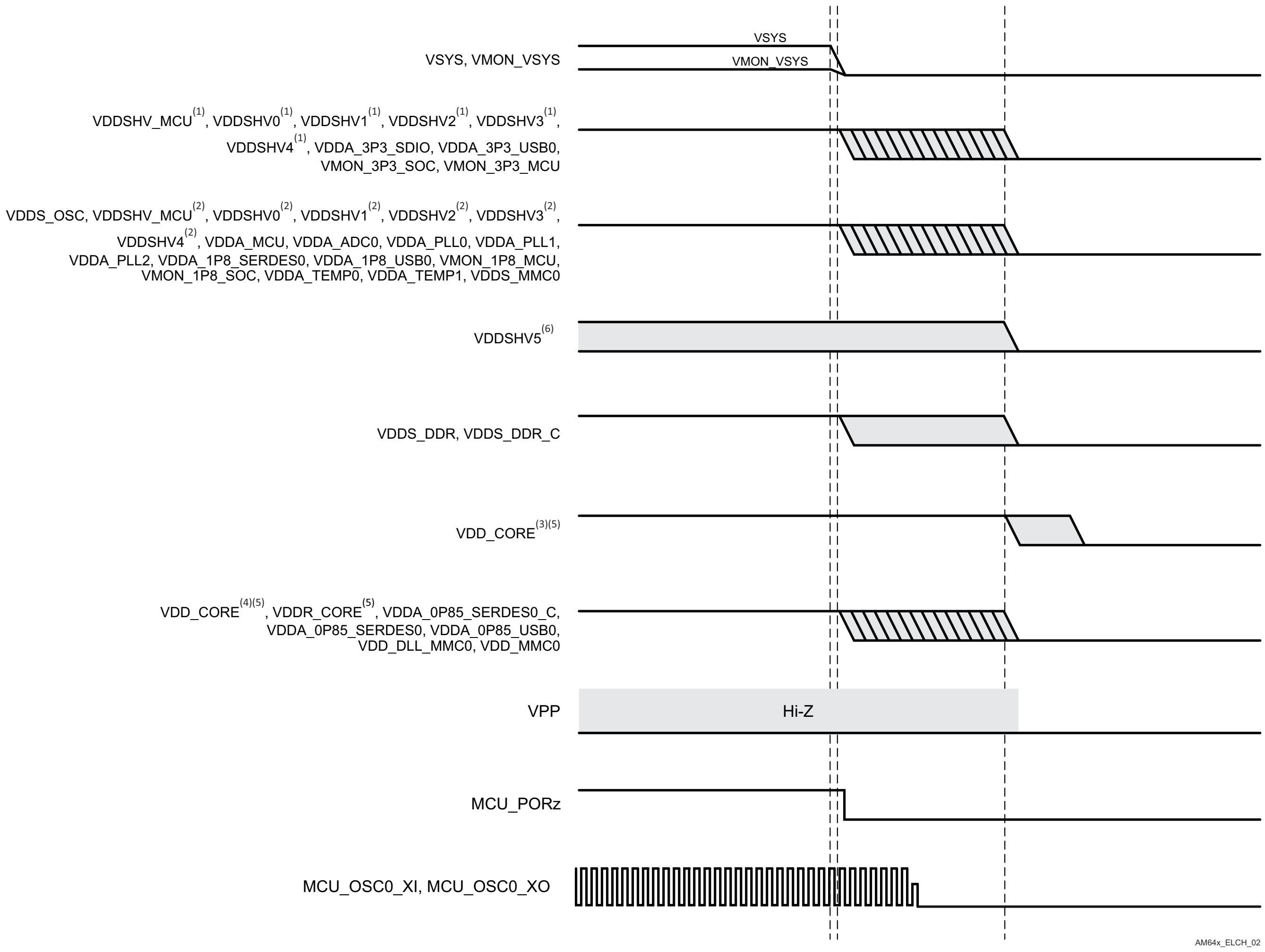


Figure 7-6. Power-Down Sequencing

1. VDDSHV_MCU and VDDSHVx [x=0-5] when operating at 3.3V.
2. VDDSHV_MCU and VDDSHVx [x=0-5] when operating at 1.8V.
3. VDD_CORE when operating at 0.75V.
4. VDD_CORE when operating at 0.85V.
5. The potential applied to VDDR_CORE must never be greater than the potential applied to VDD_CORE + 0.18V during power-up or power-down. This requires VDD_CORE to ramp up before and ramp down after VDDR_CORE when VDD_CORE is operating at 0.75V. VDD_CORE does not have any ramp requirements beyond the one defined for VDDR_CORE. VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V.
6. VDDSHV5 was designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

7.10.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

7.10.3.1 Reset Timing

Tables and figures provided in this section define timing conditions, timing requirements, and switching characteristics for reset related signals.

Table 7-4. Reset Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD(1) = 1.8V	0.0018		V/ns
		VDD(1) = 3.3V	0.0033		V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance			30	pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

Table 7-5. MCU_PORz Timing Requirements

see Figure 7-7

NO.	PARAMETER		MIN	MAX	UNIT
RST1	$t_{h(SUPPLIES\_VALID - MCU\_PORz)}$	Hold time, MCU_PORz active (low) at Power-up after supplies valid (using external crystal circuit)	9500000		ns
RST2		Hold time, MCU_PORz active (low) at Power-up after supplies valid and external clock stable (using external LVCMOS clock source)	1200		ns
RST3	$t_{w(MCU\_PORzL)}$	Pulse Width, MCU_PORz low after Power-up (without removal of Power or system reference clock MCU_OSC0_XI/XO)	1200		ns

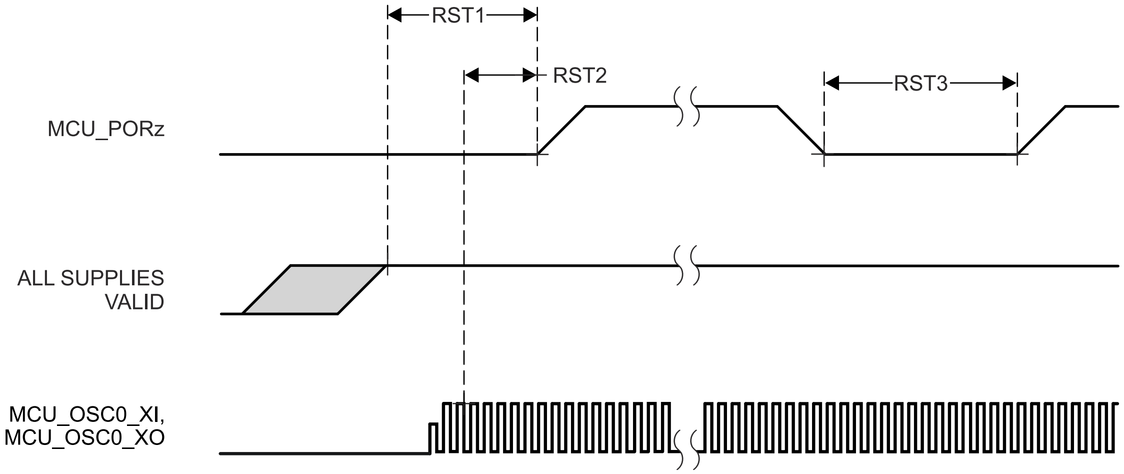


Figure 7-7. MCU_PORz Timing Requirements

Table 7-6. MCU_RESETSTATz, and RESETSTATz Switching Characteristics

see Figure 7-8

NO.	PARAMETER		MIN	MAX	UNIT
RST4	$t_{d(MCU\_PORzL-MCU\_RESETSTATzL)}$	Delay time, MCU_PORz active (low) to MCU_RESETSTATz active (low)	0		ns
RST5	$t_{d(MCU\_PORzH-MCU\_RESETSTATzH)}$	Delay time, MCU_PORz inactive (high) to MCU_RESETSTATz inactive (high)	6120*S(1)		ns
RST6	$t_{d(MCU\_PORzL-RESETSTATzL)}$	Delay time, MCU_PORz active (low) to RESETSTATz active (low)	0		ns
RST7	$t_{d(MCU\_PORzH-RESETSTATzH)}$	Delay time, MCU_PORz inactive (high) to RESETSTATz inactive (high)	9195*S(1)		ns
RST8	$t_{w(MCU\_RESETSTATzL)}$	Pulse Width, MCU_RESETSTATz low (SW_MCU_WARMRST)	966*S(1)		ns
RST9	$t_{w(RESETSTATzL)}$	Pulse Width, RESETSTATz low (SW_MCU_WARMRST, SW_MAIN_PORz, or SW_MAIN_WARMRST)	4040*S		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

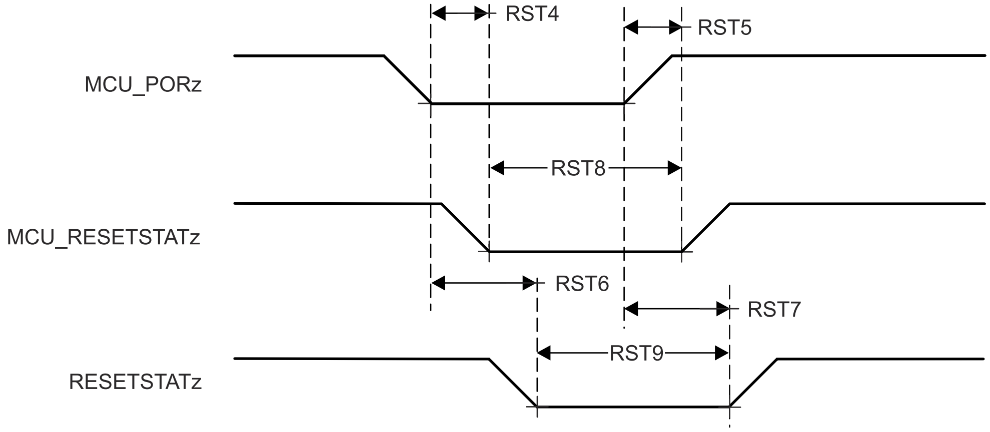


Figure 7-8. MCU_RESETSTATz, and RESETSTATz Switching Characteristics

Table 7-7. MCU_RESETz Timing Requirements

see Figure 7-9

NO.	PARAMETER		MIN	MAX	UNIT
RST10	$t_{w(MCU\_RESETzL)}$ (1)	Pulse Width, MCU_RESETz active (low)	1200		ns

(1) This timing parameter is valid only after all supplies are valid and MCU_PORz has been asserted for the specified time.

Table 7-8. MCU_RESETSTATz, and RESETSTATz Switching Characteristics

see Figure 7-9

NO.	PARAMETER		MIN	MAX	UNIT
RST11	$t_{d(MCU\_RESETzL-MCU\_RESETSTATzL)}$	Delay time, MCU_RESETz active (low) to MCU_RESETSTATz active (low)	0		ns
RST12	$t_{d(MCU\_RESETzH-MCU\_RESETSTATzH)}$	Delay time, MCU_RESETz inactive (high) to MCU_RESETSTATz inactive (high)	966*S(1)		ns
RST13	$t_{d(MCU\_RESETzL-RESETSTATzL)}$	Delay time, MCU_RESETz active (low) to RESETSTATz active (low)	960		ns
RST14	$t_{d(MCU\_RESETzH-RESETSTATzH)}$	Delay time, MCU_RESETz inactive (high) to RESETSTATz inactive (high)	4040*S(1)		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

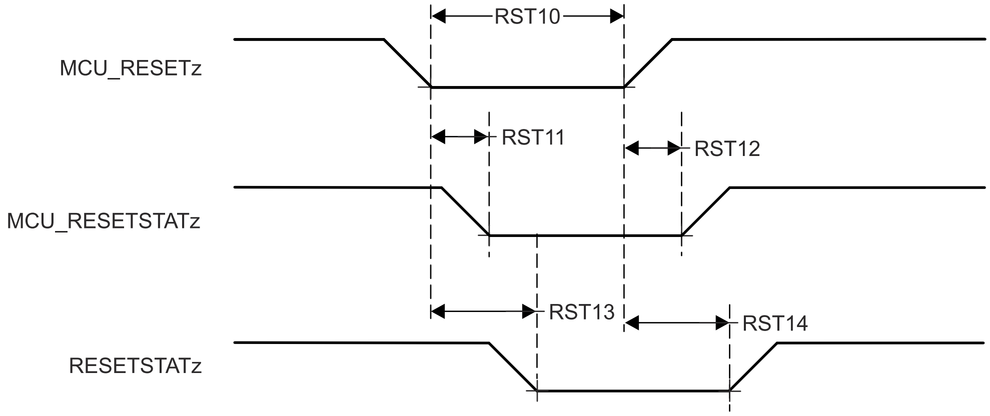


Figure 7-9. MCU_RESETz, MCU_RESETSTATz, and RESETSTATz Timing Requirements and Switching Characteristics

Table 7-9. RESET_REQz Timing Requirements

see Figure 7-10

NO.	PARAMETER		MIN	MAX	UNIT
RST15	$t_{w(RESET\_REQzL)}$ (1)	Pulse Width, RESET_REQz active (low)	1200		ns

(1) This timing parameter is valid only after all supplies are valid and MCU_PORz has been asserted for the specified time.

Table 7-10. RESETSTATz Switching Characteristics

see Figure 7-10

NO.	PARAMETER		MIN	MAX	UNIT
RST16	$t_{d(RESET\_REQzL-RESETSTATzL)}$	Delay time, RESET_REQz active (low) to RESETSTATz active (low)	900*T(1)		ns
RST17	$t_{d(RESET\_REQzH-RESETSTATzH)}$	Delay time, RESET_REQz inactive (high) to RESETSTATz inactive (high)	4040*S(2)		ns

(1) T = Reset Isolation Time (Software Dependent)
(2) S = MCU_OSC0_XI/XO clock period in ns.

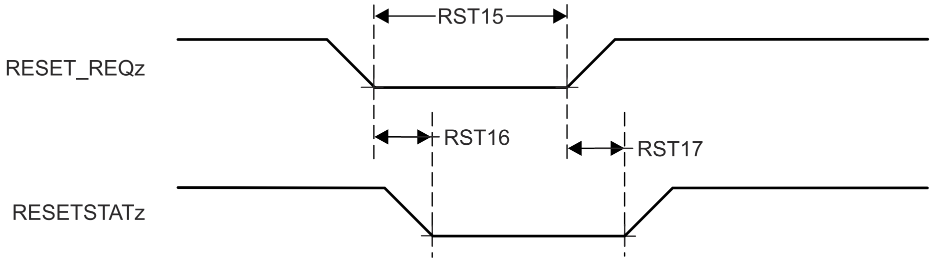


Figure 7-10. RESET_REQz and RESETSTATz Timing Requirements and Switching Characteristics

Table 7-11. EMUx Timing Requirements

see Figure 7-11

NO.	PARAMETER		MIN	MAX	UNIT
RST18	$t_{su(EMUx-MCU\_PORz)}$	Setup time, EMU[1:0] before MCU_PORz inactive (high)	3*S(1)		ns
RST19	$t_{h(MCU\_PORz - EMUx)}$	Hold time, EMU[1:0] after MCU_PORz inactive (high)	10		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

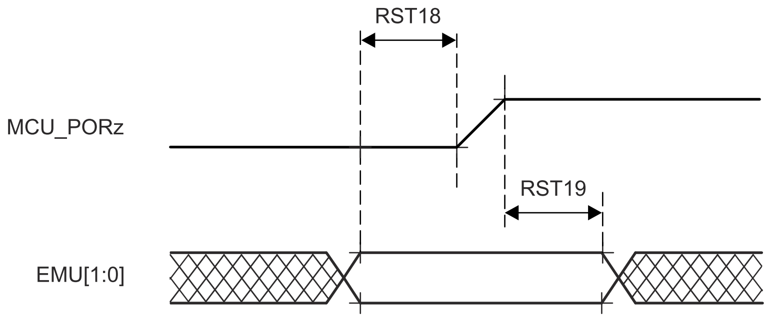


Figure 7-11. EMUx Timing Requirements

Table 7-12. BOOTMODE Timing Requirements

see Figure 7-12

NO.	PARAMETER		MIN	MAX	UNIT
RST23	$t_{su(BOOTMODE-PORz\_OUT)}$	Setup time, BOOTMODE[15:00] before PORz_OUT high (External MCU PORz event or Software SW_MAIN_PORz)	3*S(1)		ns
RST24	$t_{h(PORz\_OUT - BOOTMODE)}$	Hold time, BOOTMODE[15:00] after PORz_OUT high (External MCU PORz event, or Software SW_MAIN_PORz)	0		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

Table 7-13. PORz_OUT Switching Characteristics

see Figure 7-12

NO.	PARAMETER		MIN	MAX	UNIT
RST25	$t_{d(MCU\_PORzL-PORz\_OUT)}$	Delay time, MCU_PORz active (low) to PORz_OUT active (low)	0		ns
RST26	$t_{d(MCU\_PORzH-PORz\_OUT)}$	Delay time, MCU_PORz inactive (high) to PORz_OUT inactive (high)	1840		ns
RST27	$t_{w(PORz\_OUTL)}$	Pulse Width, PORz_OUT low (MCU_PORz or SW_MAIN_PORz)	1200		ns

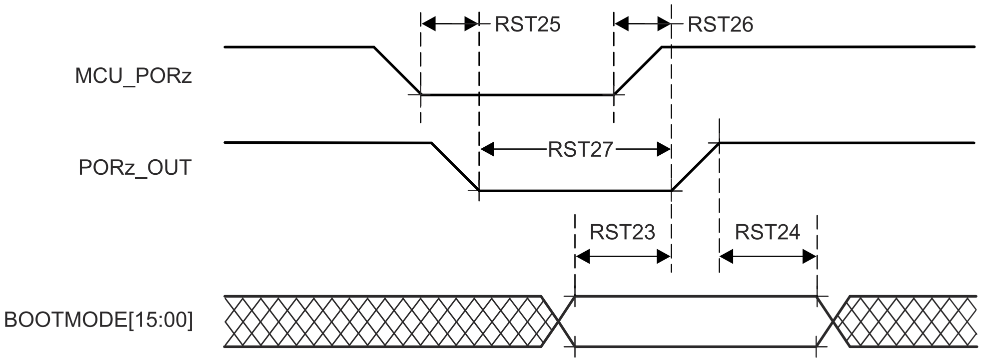


Figure 7-12. BOOTMODE Timing Requirements and PORz_OUT Switching Characteristics

7.10.3.2 Safety Signal Timing

Tables and figures provided in this section define timing conditions and switching characteristics for MCU_SAFETY_ERRORn.

Table 7-14. MCU_SAFETY_ERRORn Timing Conditions

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output load capacitance		30	pF

Table 7-15. MCU_SAFETY_ERRORn Switching Characteristics

see Figure 7-13

NO.	PARAMETER		MIN	MAX	UNIT
SFTY1	$t_{c(MCU\_SAFETY\_ERRORn)}$	Cycle time minimum, MCU_SAFETY_ERRORn (PWM mode enabled)	(P*H)+(P*L)(1) (3) (4)		ns
SFTY2	$t_{w(MCU\_SAFETY\_ERRORn)}$	Pulse width minimum, MCU_SAFETY_ERRORn active (PWM mode disabled)(5)	P*R(1) (2)		ns
SFTY3	$t_{d\ (ERROR\_CONDITION\text{-}MCU\_SAFETY\_ERRORnL)}$	Delay time, ERROR CONDITION to MCU_SAFETY_ERRORn active(5)	50*P(1)		ns

(1) P = ESM functional clock
(2) R = Error Pin Counter Pre-Load Register count value
(3) H = Error Pin PWM High Pre-Load Register count value
(4) L = Error Pin PWM Low Pre-Load Register count value
(5) When PWM mode is enabled, MCU_SAFETY_ERRORn stops toggling after SFTY3 and will maintain its value (either high or low) until the error is cleared. When PWM mode is disabled, MCU_SAFETY_ERRORn is active low.

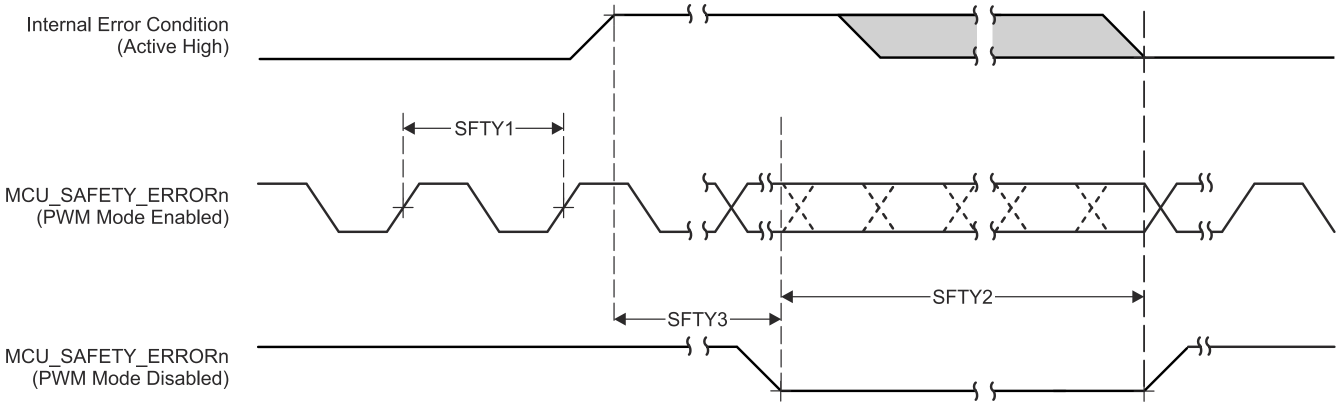


Figure 7-13. MCU_SAFETY_ERRORn Timing Requirements and Switching Characteristics

7.10.3.3 Clock Timing

Tables and figures provided in this section define timing conditions, timing requirements, and switching characteristics for clock signals.

Table 7-16. Clock Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		0.5		V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	10 ns ≤ t_c < 20 ns		10	pF
		20 ns ≤ t_c		30	pF

Table 7-17. Clock Timing Requirements

see Figure 7-14

NO.			MIN	MAX	UNIT
CLK1	$t_{c(EXT\_REFCLK1)}$	Cycle time minimum, EXT_REFCLK1	10		ns
CLK2	$t_{w(EXT\_REFCLK1H)}$	Pulse Duration, EXT_REFCLK1 high	E*0.45(1)	E*0.55(1)	ns
CLK3	$t_{w(EXT\_REFCLK1L)}$	Pulse Duration, EXT_REFCLK1 low	E*0.45(1)	E*0.55(1)	ns
CLK1	$t_{c(MCU\_EXT\_REFCLK0)}$	Cycle time minimum, MCU_EXT_REFCLK0	10		ns
CLK2	$t_{w(MCU\_EXT\_REFCLK0H)}$	Pulse Duration, MCU_EXT_REFCLK0 high	F*0.45(2)	F*0.55(2)	ns
CLK3	$t_{w(MCU\_EXT\_REFCLK0L)}$	Pulse Duration, MCU_EXT_REFCLK0 low	F*0.45(2)	F*0.55(2)	ns

(1) E = EXT_REFCLK1 cycle time
(2) F = MCU_EXT_REFCLK0 cycle time

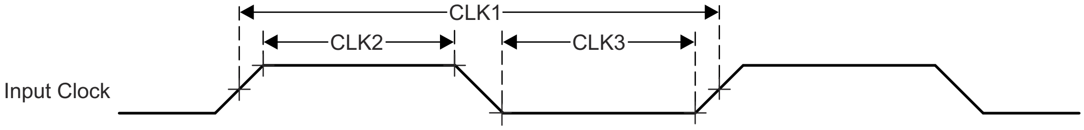


Figure 7-14. Clock Timing Requirements

Table 7-18. Clock Switching Characteristics

see Figure 7-15

NO.	PARAMETER		MIN	MAX	UNIT
CLK4	$t_{c(SYSCLKOUT0)}$	Cycle time minimum,SYSCLKOUT0	8		ns
CLK5	$t_{w(SYSCLKOUT0H)}$	Pulse Duration, SYSCLKOUT0 high	A*0.4(1)	A*0.6(1)	ns
CLK6	$t_{w(SYSCLKOUT0L)}$	Pulse Duration, SYSCLKOUT0 low	A*0.4(1)	A*0.6(1)	ns
CLK4	$t_{c(OBSCLK0)}$	Cycle time minimum, OBSCLK0	5		ns
CLK5	$t_{w(OBSCLK0H)}$	Pulse Duration, OBSCLK0 high	B*0.45(2)	B*0.55(2)	ns
CLK6	$t_{w(OBSCLK0L)}$	Pulse Duration,OBSCLK0 low	B*0.45(2)	B*0.55(2)	ns
CLK4	$t_{c(CLKOUT0)}$	Cycle time minimum, CLKOUT0	20		ns
CLK5	$t_{w(CLKOUT0H)}$	Pulse Duration, CLKOUT0 high	C*0.4(3)	C*0.6(3)	ns
CLK6	$t_{w(CLKOUT0L)}$	Pulse Duration,CLKOUT0 low	C*0.4(3)	C*0.6(3)	ns
CLK4	$t_{c(MCU\_SYSCLKOUT0)}$	Cycle time minimum, MCU_SYSCLKOUT0	10		ns
CLK5	$t_{w(MCU\_SYSCLKOUT0H)}$	Pulse Duration, MCU_SYSCLKOUT0 high	G*0.4(4)	G*0.6(4)	ns
CLK6	$t_{w(MCU\_SYSCLKOUT0L)}$	Pulse Duration,MCU_SYSCLKOUT0 low	G*0.4(4)	G*0.6(4)	ns
CLK4	$t_{c(MCU\_OBSCLK0)}$	Cycle time minimum, MCU_OBSCLK0	5		ns
CLK5	$t_{w(MCU\_OBSCLK0H)}$	Pulse Duration, MCU_OBSCLK0 high	H*0.45(5)	H*0.55(5)	ns
CLK6	$t_{w(MCU\_OBSCLK0L)}$	Pulse Duration,MCU_OBSCLK0 low	H*0.45(5)	H*0.55(5)	ns

(1) A = SYSCLKOUT0 cycle time
(2) B = OBSCLK0 cycle time
(3) C = CLKOUT0 cycle time
(4) G = MCU_SYSCLKOUT0 cycle time
(5) H = MCU_OBSCLK0 cycle time

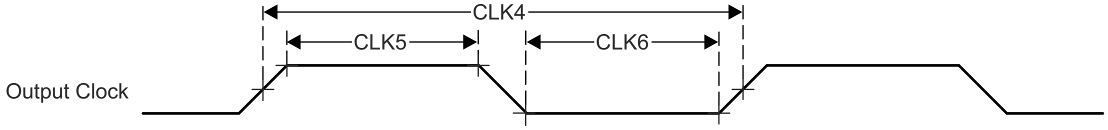


Figure 7-15. Clock Switching Characteristics

7.10.4 Clock Specifications

7.10.4.1 Input Clocks / Oscillators

Various external clock inputs/outputs are needed to drive the device. Summary of these input clock signals is as follows:

- MCU_OSC0_XI/MCU_OSC0_XO — External main crystal interface pins connected to the internal high-frequency oscillator (MCU_HFOSC0), which is the default clock source for internal reference clock MCU_HFOSC0_CLKOUT.
- General purpose clock inputs
  - MCU_EXT_REFCLK0 — Optional external system clock input for MCU domain.
  - EXT_REFCLK1 — Optional external system clock input for MAIN domain.
  - SERDES0_REFCLK0P/N — Optional SERDES0 reference clock input for PCIe.
- External CPTS reference clock inputs
  - CP_GEMAC_CPTS0_RFT_CLK — CPTS reference clock input.
  - CPTS_RFT_CLK — CPTS reference clock input.

Figure 7-16 shows the external input clock sources and the output clocks to peripherals.

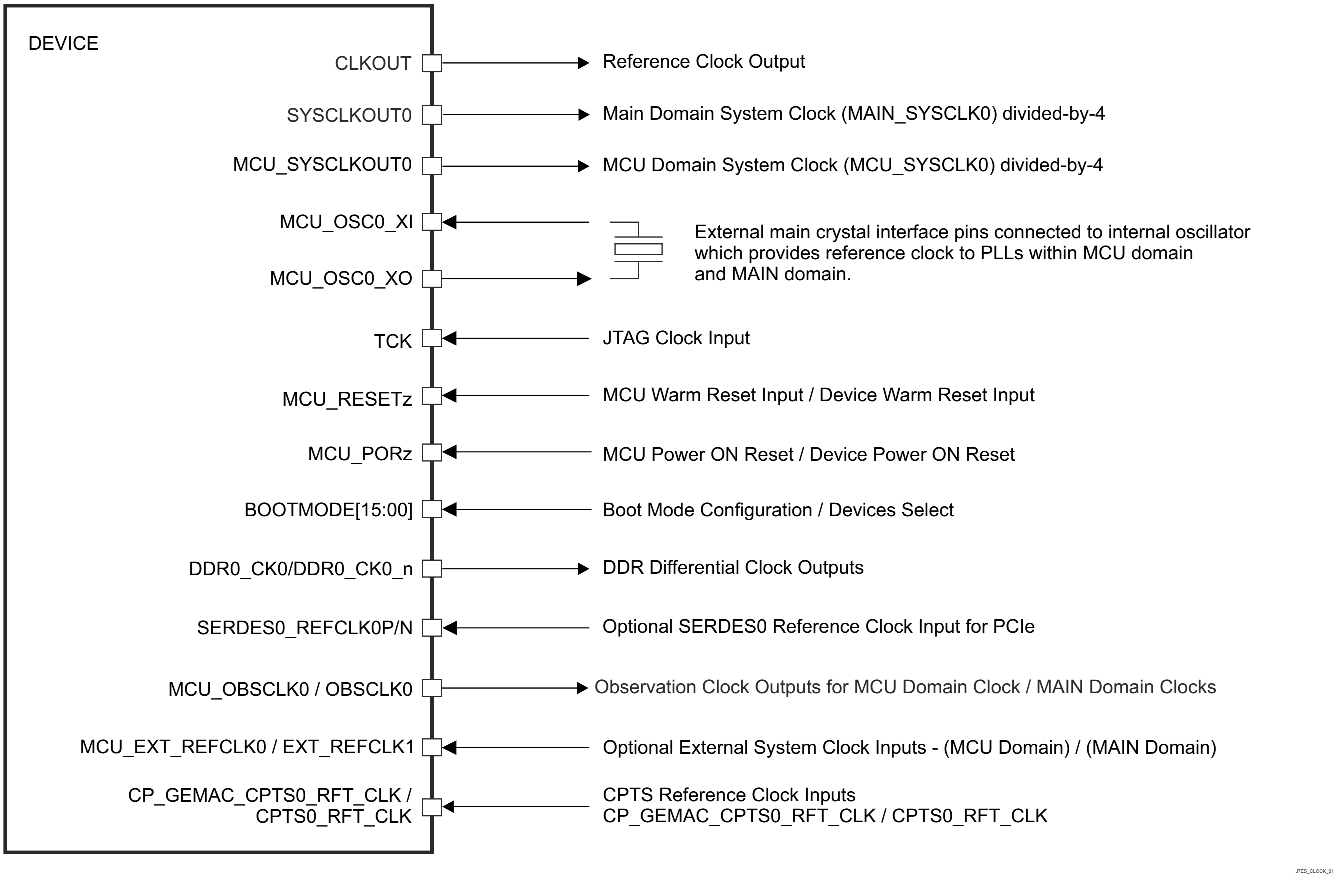


Figure 7-16. Input Clocks Interface

For more information about Input clock interfaces, see *Clocking* section in *Device Configuration* chapter in the device TRM.

7.10.4.1.1 MCU_OSC0 Internal Oscillator Clock Source

Figure 7-17 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit must be placed as close as possible to the MCU_OSC0_XI and MCU_OSC0_XO pins.

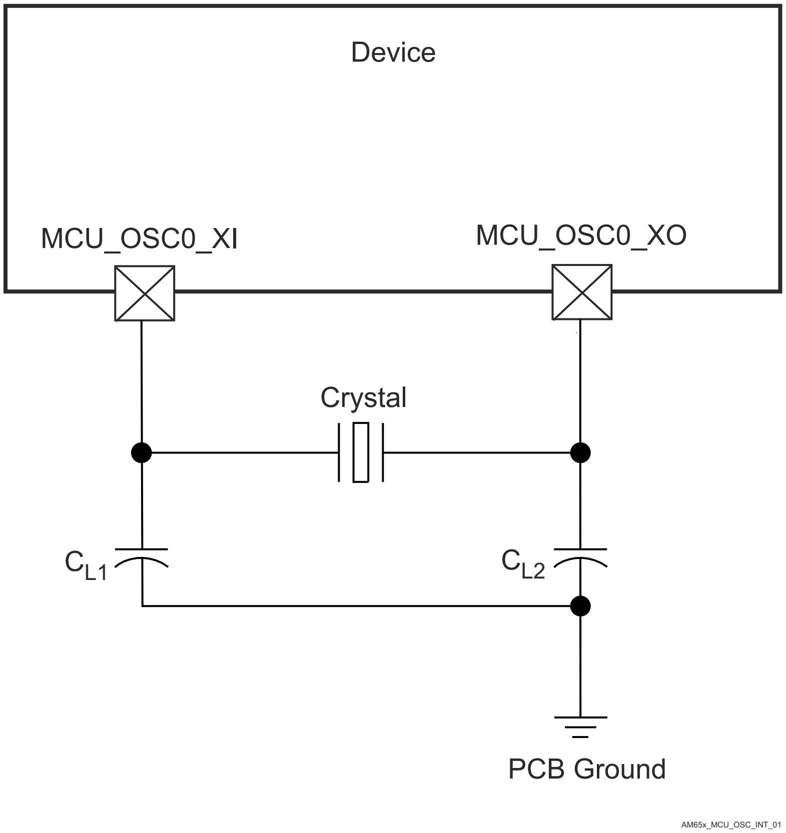


Figure 7-17. MCU_OSC0 Crystal Implementation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 7-19 summarizes the required electrical constraints.

Table 7-19. MCU_OSC0 Crystal Circuit Requirements

PARAMETER				MIN	TYP	MAX	UNIT
F_{xtal}	Crystal Parallel Resonance Frequency				25		MHz
F_{xtal}	Crystal Frequency Stability and Tolerance		Ethernet RGMII and RMII not used			±100	ppm
			Ethernet RGMII and RMII using derived clock			±50	
$C_{L1+PCBXI}$	Capacitance of C_{L1} + C_{PCBXI}			12		24	pF
$C_{L2+PCBXO}$	Capacitance of C_{L2} + C_{PCBXO}			12		24	pF
C_L	Crystal Load Capacitance			6		12	pF
C_{shunt}	Crystal Circuit Shunt Capacitance	ESR_{xtal} = 30 Ω	25 MHz			7	pF
		ESR_{xtal} = 40 Ω	25 MHz			5	pF
		ESR_{xtal} = 50 Ω	25 MHz			5	pF
ESR_{xtal}	Crystal Effective Series Resistance					(1)	Ω

(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C_{shunt} parameter.

When selecting a crystal, the system design must consider temperature and aging characteristics of the crystal based on worst case environment and expected life expectancy of the system.

Table 7-20 details the switching characteristics of the oscillator.

Table 7-20. MCU_OSC0 Switching Characteristics - Crystal Mode

PARAMETER		MIN	TYP	MAX	UNIT
C_{XI}	XI Capacitance			1.44	pF
C_{XO}	XO Capacitance			1.52	pF
C_{XIXO}	XI to XO Mutual Capacitance			0.01	pF
t_s	Start-up Time		4		ms

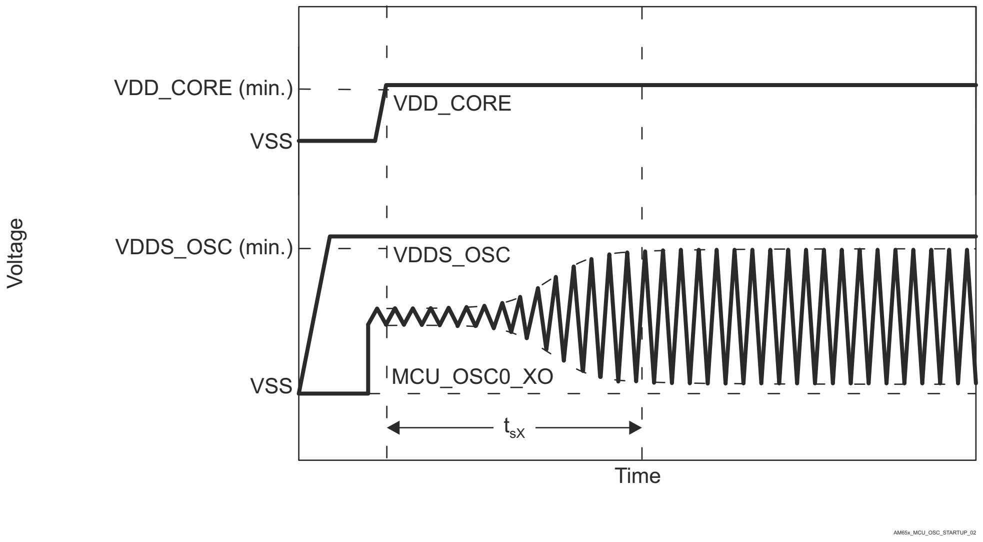


Figure 7-18. MCU_OSC0 Start-up Time

7.10.4.1.1.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load, C_L, of this circuit is a combination of discrete capacitors C_{L1}, C_{L2}, and several parasitic contributions. PCB signal traces which connect crystal circuit components to MCU_OSC0_XI and MCU_OSC0_XO have parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where the PCB designer should be able to extract parasitic capacitance for each signal trace. The MCU_OSC0 circuits and device package have combined parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where these parasitic capacitance values are defined in Table 7-20.

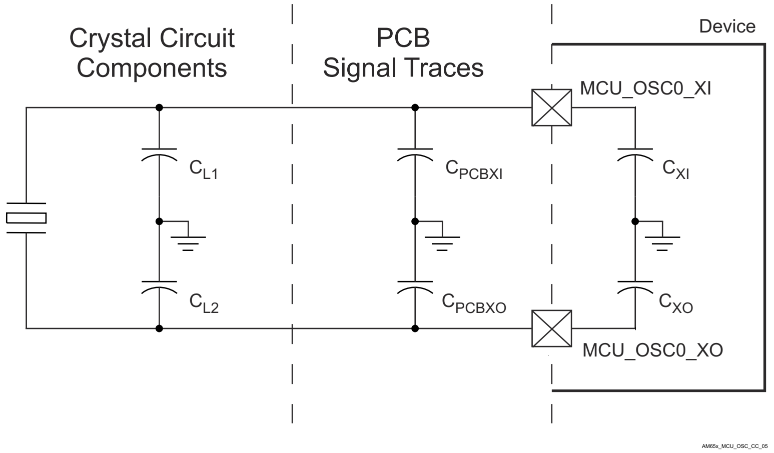


Figure 7-19. Load Capacitance

Load capacitors, C_{L1} and C_{L2} in Figure 7-17, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer.

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of C_{L1} and C_{L2}, multiply the capacitive load value C_L by 2. Using this result, subtract the combined values of C_{PCBXI} + C_{XI} to determine the value of C_{L1} and the combined values of C_{PCBXO} + C_{XO} to determine the value of C_{L2}. For example, if C_L = 10 pF, C_{PCBXI} = 2.9 pF, C_{XI} = 0.5 pF, C_{PCBXO} = 3.7 pF, C_{XO} = 0.5 pF, the value of $C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 \times 10\text{ pF}) - 2.9\text{ pF} - 0.5\text{ pF})] = 16.6$ pF and $C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 \times 10\text{ pF}) - 3.7\text{ pF} - 0.5\text{ pF})] = 15.8$ pF

7.10.4.1.1.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for MCU_OSC0 operating conditions defined in Table 7-19. Shunt capacitance, C_{shunt}, of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to MCU_OSC0 have mutual parasitic capacitance to each other, $C_{PCBXIXO}$, where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance, C_{XIXO}, where this mutual parasitic capacitance value is defined in Table 7-20.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

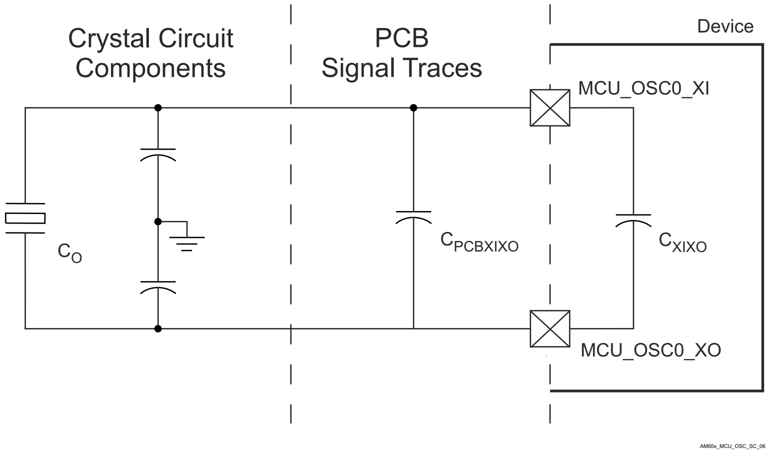


Figure 7-20. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied. C_O in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$$C_{shunt} \geq C_O + C_{PCBXIXO} + C_{XIXO}$$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30 Ω, $C_{PCBXIXO}$ = 0.04 pF, C_{XIXO} = 0.01 pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

7.10.4.1.2 MCU_OSC0 LVCMOS Digital Clock Source

Figure 7-21 shows the recommended oscillator connections when MCU_OSC0_XI is connected to a 1.8-V LVCMOS square-wave digital clock source.

Note

A DC steady-state condition is not allowed on MCU_OSC0_XI when the oscillator is powered up. This is not allowed because MCU_OSC0_XI is internally AC coupled to a comparator that can enter an unknown state when DC is applied to the input. Therefore, application software must power down MCU_OSC0 any time MCU_OSC0_XI is not toggling between logic states.

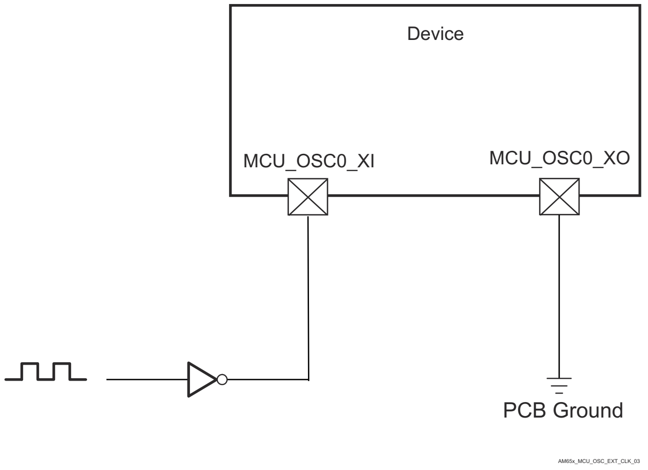


Figure 7-21. 1.8-V LVCMOS-Compatible Clock Input

7.10.4.2 Output Clocks

The device provides several system clock outputs. Summary of these output clocks are as follows:

- **MCU_SYSCLKOUT0**
  - MCU_SYSCLKOUT0 is the MCU domain system clock (MCU_SYSCK0) divided-by-4. This clock output is provided for test and debug purposes only.
- **MCU_OBSCLK0**
  - Observation clock output for test and debug purposes only.
- **SYSCLKOUT0**
  - SYSCLKOUT0 is the MAIN domain system clock (MAIN_SYSCLK0) divided-by-4. This clock output is provided for test and debug purposes only.
- **CLKOUT0**
  - CLKOUT0 is the Ethernet subsystem clock (MAIN_PLL0_HSDIV4_CLKOUT) divided-by-5 or divided-by-10. This clock output was provided to source to the external PHY. When configured to operate as the RMII Clock source (50 MHz) the signal must also be routed back to the RMII_REF_CLK pin for proper device operation.
- **OBSCLK0**
  - Observation clock output for test and debug purposes only.
- **GPMC_FCLK_MUX**
  - GPMC_FCLK_MUX is the GPMC0 functional clock (GPMC_FCLK). This clock is provided as an alternative GPMC interface clock when attached devices require a continuous running clock.

For more information, see *Clock Outputs* section in *Clocking* chapter and *GPMC Clock Configuration* section in *Peripherals* chapter in the device TRM.

7.10.4.3 PLLs

Power is supplied to the Phase-Locked Loop circuits (PLLs) by internal regulators that derive their power from off-chip power-sources.

There is one PLL in the MCU domain:

- MCU0_PLL

There are six PLLs in the MAIN domain:

- ARM0_PLL
- MAIN_PLL
- PER0_PLL
- PER1_PLL
- DDR PLL
- R5F PLL

Note

For more information, see:

- *Device Configuration / Clocking / PLLs* section in the device TRM.
- *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)* section in the device TRM.

Note

The input reference clock (MCU_OSC0_XI / MCU_OSC0_XO) is specified and the lock time is ensured by the PLL controller, as documented in the *Device Configuration* chapter in the device TRM.

7.10.4.4 Recommended System Precautions for Clock and Control Signal Transitions

All clock and strobe signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

Monotonic transitions are more likely to occur with fast signal transitions. It is easy for noise to create non-monotonic events on a signal with slow transitions. Therefore, avoid slow signal transitions on all clock and control signals since they are more likely to generate glitches inside the device.

7.10.5 Peripherals

7.10.5.1 CPSW3G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Note

CPSW3G MDIO0, CPSW3G RMII1, CPSW3G RMII2, and CPSW3G RGMII1 have one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for these interfaces can be found in the tables of the CPSW3G IOSETs section.

7.10.5.1.1 CPSW3G MDIO Timing

Table 7-21, Table 7-22, Table 7-23, and Figure 7-22 present timing conditions, requirements, and switching characteristics for CPSW3G MDIO.

Table 7-21. CPSW3G MDIO Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	10	470	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	0	5	ns
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		1	ns

Table 7-22. CPSW3G MDIO Timing Requirements

see Figure 7-22

NO.	PARAMETER		MIN	MAX	UNIT
MDIO1	$t_{su(MDIO\_MDC)}$	Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high	45		ns
MDIO2	$t_{h(MDC\_MDIO)}$	Hold time, MDIO[x]_MDIO valid after MDIO[x]_MDC high	0		ns

Table 7-23. CPWS3G MDIO Switching Characteristics

see Figure 7-22

NO.	PARAMETER		MIN	MAX	UNIT
MDIO3	$t_{c(MDC)}$	Cycle time, MDIO[x]_MDC	400		ns
MDIO4	$t_{w(MDCH)}$	Pulse Duration, MDIO[x]_MDC high	160		ns
MDIO5	$t_{w(MDCL)}$	Pulse Duration, MDIO[x]_MDC low	160		ns
MDIO7	$t_{d(MDC\_MDIO)}$	Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid	-10	10	ns

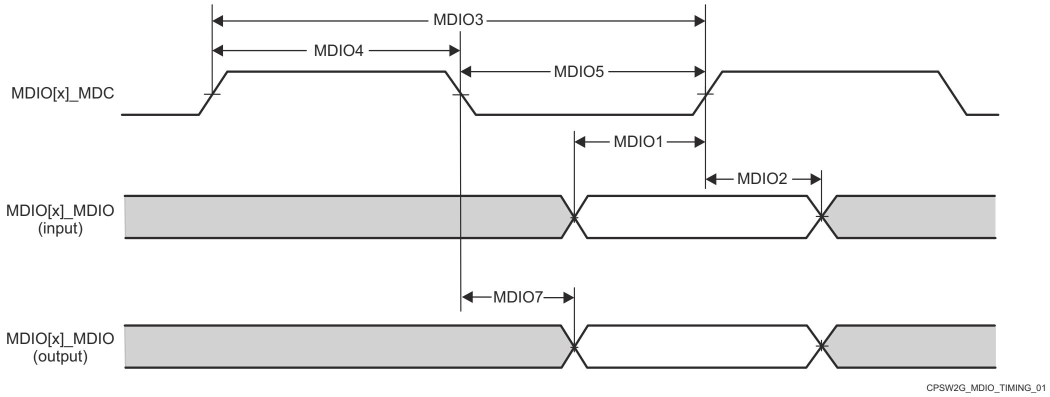


Figure 7-22. CPSW3G MDIO Timing Requirements and Switching Characteristics

7.10.5.1.2 CPSW3G RMII Timing

Table 7-24, Table 7-25, Figure 7-23, Table 7-26, Figure 7-24 Table 7-27, and Figure 7-25 present timing conditions, requirements, and switching characteristics for CPSW3G RMII.

Table 7-24. CPSW3G RMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD(1) = 1.8V	0.18	0.54	V/ns
		VDD(1) = 3.3V	0.4	1.2	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	25	pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

Table 7-25. RMII[x]_REF_CLK Timing Requirements – RMII Mode

see Figure 7-23

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII1	$t_{c(REF\_CLK)}$	Cycle time, RMII[x]_REF_CLK	19.999	20.001	ns
RMII2	$t_{w(REF\_CLKH)}$	Pulse Duration, RMII[x]_REF_CLK High	7	13	ns
RMII3	$t_{w(REF\_CLKL)}$	Pulse Duration, RMII[x]_REF_CLK Low	7	13	ns

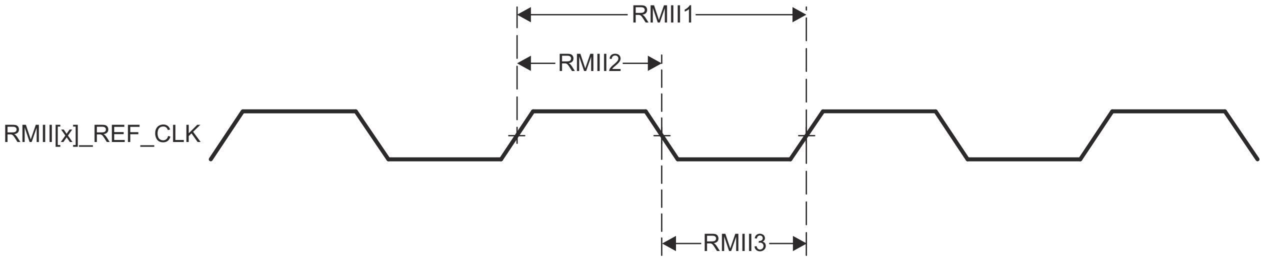


Figure 7-23. CPSW3G RMII[x]_REF_CLK Timing Requirements – RMII Mode

Table 7-26. RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RX_ER Timing Requirements – RMII Mode

see Figure 7-24

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII4	$t_{su(RXD-REF\_CLK)}$	Setup time, RMII[x]_RXD[1:0] valid before RMII[x]_REF_CLK	4		ns
	$t_{su(CRS\_DV-REF\_CLK)}$	Setup time, RMII[x]_CRS_DV valid before RMII[x]_REF_CLK	4		ns
	$t_{su(RX\_ER-REF\_CLK)}$	Setup time, RMII[x]_RX_ER valid before RMII[x]_REF_CLK	4		ns
RMII5	$t_{h(REF\_CLK-RXD)}$	Hold time RMII[x]_RXD[1:0] valid after RMII[x]_REF_CLK	2		ns
	$t_{h(REF\_CLK-CRS\_DV)}$	Hold time, RMII[x]_CRS_DV valid after RMII[x]_REF_CLK	2		ns
	$t_{h(REF\_CLK-RX\_ER)}$	Hold time, RMII[x]_RX_ER valid after RMII[x]_REF_CLK	2		ns

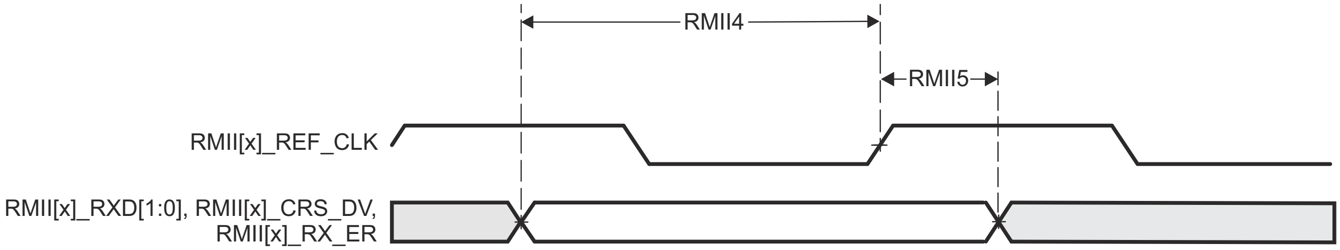


Figure 7-24. CPSW3G RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RX_ER Timing Requirements – RMII Mode

Table 7-27. RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

see Figure 7-25

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII6	$t_{d(REF\_CLK-TXD)}$	Delay time, RMII[x]_REF_CLK High to RMII[x]_TXD[1:0] valid	2	10	ns
	$t_{d(REF\_CLK-TX\_EN)}$	Delay time, RMII[x]_REF_CLK to RMII[x]_TX_EN valid	2	10	ns

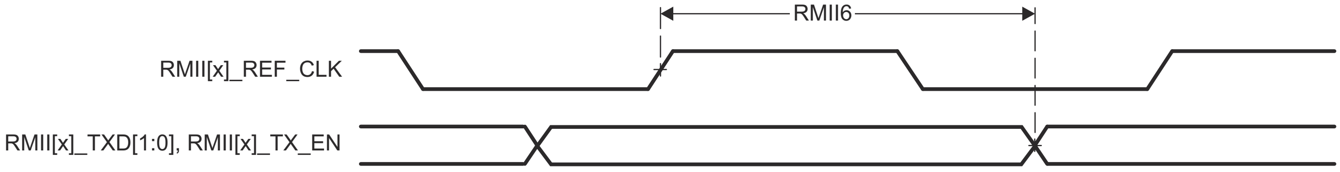


Figure 7-25. RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

7.10.5.1.3 CPSW3G RGMII Timing

Table 7-28, Table 7-29, Table 7-30, Figure 7-26, Table 7-31, Table 7-32, and Figure 7-27 present timing conditions, requirements, and switching characteristics for CPSW3G RGMII.

Table 7-28. CPSW3G RGMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		2.64	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(\text{Trace Mismatch Delay})}$	Propagation delay mismatch across all traces	RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL		50	ps
		RGMII[x]_TXC, RGMII[x]_TD[3:0], RGMII[x]_TX_CTL		50	ps

Table 7-29. RGMII[x]_RXC Timing Requirements – RGMII Mode

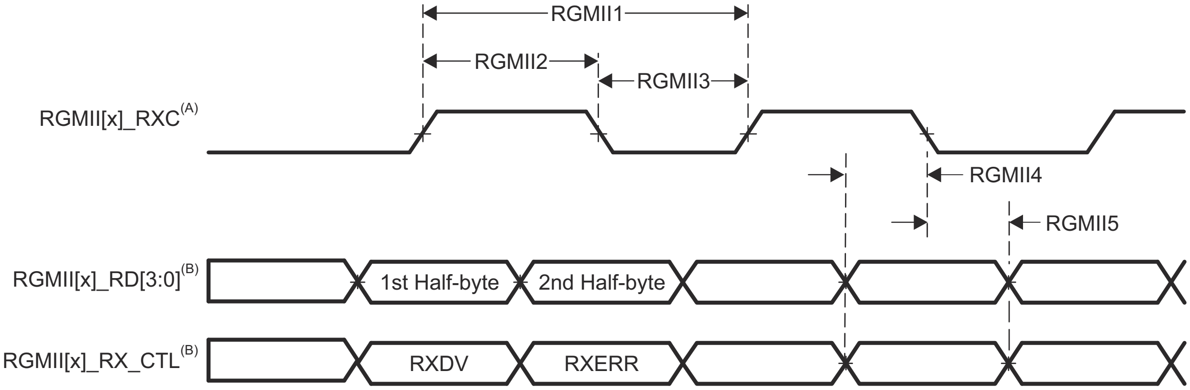
see Figure 7-26

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII1	$t_{c(RXC)}$	Cycle time, RGMII[x]_RXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII2	$t_{w(RXCH)}$	Pulse duration, RGMII[x]_RXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII3	$t_{w(RXCL)}$	Pulse duration, RGMII[x]_RXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

Table 7-30. RGMII[x]_RD[3:0], and RGMII[x]_RX_CTL Timing Requirements – RGMII Mode

see Figure 7-26

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII4	$t_{su(RD-RXC)}$	Setup time, RGMII[x]_RD[3:0] valid before RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{su(RX\_CTL-RXC)}$	Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
RGMII5	$t_{h(RXC-RD)}$	Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{h(RXC-RX\_CTL)}$	Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns



A. RGMII[x]_RXC must be externally delayed relative to the data and control pins.

B. Data and control information is received using both edges of the clocks. RGMII[x]_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_RXC and data bits 7-4 on the falling edge of RGMII[x]_RXC. Similarly, RGMII[x]_RX_CTL carries RXDV on rising edge of RGMII[x]_RXC and RXERR on falling edge of RGMII[x]_RXC.

Figure 7-26. CPSW3G RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL Timing Requirements - RGMII Mode

Table 7-31. RGMII[x]_TXC Switching Characteristics – RGMII Mode

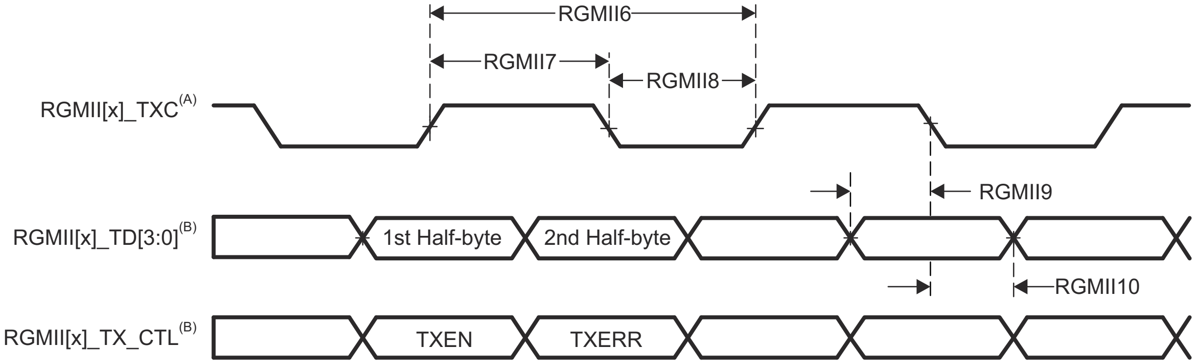
see Figure 7-27

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII6	$t_{c(TXC)}$	Cycle time, RGMII[x]_TXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII7	$t_{w(TXCH)}$	Pulse duration, RGMII[x]_TXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII8	$t_{w(TXCL)}$	Pulse duration, RGMII[x]_TXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

Table 7-32. RGMII[x]_TD[3:0] and RGMII[x]_TX_CTL Switching Characteristics – RGMII Mode

see Figure 7-27

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII9	$t_{osu(TD-TXC)}$	Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{osu(TX\_CTL-TXC)}$	Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
RGMII10	$t_{oh(TXC-TD)}$	Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{oh(TXC-TX\_CTL)}$	Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns



A. TXC is delayed internally before being driven to the RGMII[x]_TXC pin. This internal delay is always enabled.

B. Data and control information is received using both edges of the clocks. RGMII[x]_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_TXC and data bits 7-4 on the falling edge of RGMII[x]_TXC. Similarly, RGMII[x]_TX_CTL carries TXEN on rising edge of RGMII[x]_TXC and TXERR on falling edge of RGMII[x]_TXC.

Figure 7-27. CPSW3G RGMII[x]_TXC, RGMII[x]_TD[3:0], and RGMII[x]_TX_CTL Switching Characteristics - RGMII Mode

7.10.5.1.4 CPSW3G IOSETs

Table 7-33 defines valid pin combinations of each CPSW3G MDIO0 IOSET.

Table 7-33. CPSW3G MDIO0 IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL NAME	MUXMODE	BALL NAME	MUXMODE
MDIO0_MDIO	PRG0_PRU1_GPO18	4	PRG1_MDIO0_MDIO	4
MDIO0_MDC	PRG0_PRU1_GPO19	4	PRG1_MDIO0_MDC	4

Table 7-34 defines valid pin combinations of each CPSW3G RMII1 and RMII2 IOSET.

Table 7-34. CPSW3G RMII1 and RMII2 IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL NAME	MUXMODE	BALL NAME	MUXMODE
RMII_REF_CLK(1)	PRG1_PRU0_GPO10	5	PRG0_PRU0_GPO10	5
RMII1_CRS_DV	PRG1_PRU1_GPO19	5	PRG0_PRU1_GPO19	5
RMII1_RX_ER	PRG1_PRU0_GPO9	5	PRG0_PRU0_GPO9	5
RMII1_RXD0	PRG1_PRU1_GPO7	5	PRG0_PRU1_GPO7	5
RMII1_RXD1	PRG1_PRU1_GPO9	5	PRG0_PRU1_GPO9	5
RMII1_TXD0	PRG1_PRU1_GPO10	5	PRG0_PRU1_GPO10	5
RMII1_TXD1	PRG1_PRU1_GPO17	5	PRG0_PRU1_GPO17	5
RMII1_TX_EN	PRG1_PRU1_GPO18	5	PRG0_PRU1_GPO18	5
RMII2_CRS_DV	PRG1_PRU1_GPO13	5	PRG1_PRU1_GPO13	5
RMII2_RX_ER	PRG1_PRU1_GPO4	5	PRG1_PRU1_GPO4	5
RMII2_RXD0	PRG1_PRU1_GPO0	5	PRG1_PRU1_GPO0	5
RMII2_RXD1	PRG1_PRU1_GPO1	5	PRG1_PRU1_GPO1	5
RMII2_TXD0	PRG1_PRU1_GPO11	5	PRG1_PRU1_GPO11	5
RMII2_TXD1	PRG1_PRU1_GPO12	5	PRG1_PRU1_GPO12	5
RMII2_TX_EN	PRG1_PRU1_GPO15	5	PRG1_PRU1_GPO15	5

(1) RMII_REF_CLK is common to both RMII1 and RMII2. For proper operation, all pin multiplexed signal assignments must use the same IOSET.

Table 7-35 defines valid pin combinations of each CPSW3G RGMII1 IOSET.

Table 7-35. CPSW3G RGMII1 IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL NAME	MUXMODE	BALL NAME	MUXMODE
RGMII1_TX_CTL	PRG1_PRU0_GPO9	4	PRG1_PRU0_GPO9	4
RGMII1_TXC	PRG1_PRU0_GPO10	4	PRG1_PRU0_GPO10	4
RGMII1_TD0	PRG1_PRU1_GPO7	4	PRG1_PRU1_GPO7	4
RGMII1_TD1	PRG1_PRU1_GPO9	4	PRG1_PRU1_GPO9	4
RGMII1_TD2	PRG1_PRU1_GPO10	4	PRG1_PRU1_GPO10	4
RGMII1_TD3	PRG1_PRU1_GPO17	4	PRG1_PRU1_GPO17	4
RGMII1_RX_CTL	PRG0_PRU0_GPO9	4	PRG1_PRU0_GPO5	4
RGMII1_RXC	PRG0_PRU0_GPO10	4	PRG1_PRU0_GPO8	4
RGMII1_RD0	PRG0_PRU1_GPO7	4	PRG1_PRU1_GPO5	4
RGMII1_RD1	PRG0_PRU1_GPO9	4	PRG1_PRU1_GPO8	4
RGMII1_RD2	PRG0_PRU1_GPO10	4	PRG1_PRU1_GPO18	4
RGMII1_RD3	PRG0_PRU1_GPO17	4	PRG1_PRU1_GPO19	4

7.10.5.2 DDRSS

For more details about features and additional description information on the device (LP)DDR4 Memory Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 7-36 and Figure 7-28 present switching characteristics for DDRSS.

Table 7-36. DDRSS Switching Characteristics

see Figure 7-28

NO.	PARAMETER		DDR TYPE	MIN	MAX	UNIT
1	$t_{c(DDR\_CKP/DDR\_CKN)}$	Cycle time, DDR_CKP and DDR_CKN	LPDDR4	1.25(1)	20	ns
			DDR4	1.25(1)	1.6	ns

(1) Minimum DDR clock Cycle time will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. Refer to AM64x\AM243x DDR Board Design and Layout Guidelines for the proper PCB implementation to achieve maximum DDR frequency.

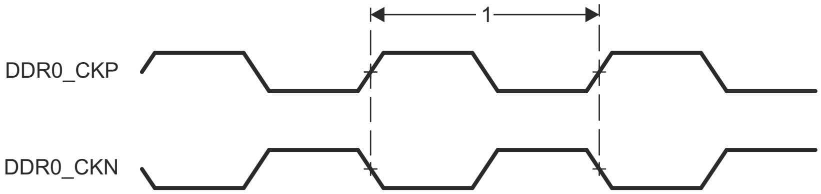


Figure 7-28. DDRSS Switching Characteristics

For more information, see *DDR Subsystem (DDRSS)* section in *Memory Controllers* chapter in the device TRM.

7.10.5.3 ECAP

Table 7-37, Table 7-38, Figure 7-29, Table 7-39, and Figure 7-30 present timing conditions, requirements, and switching characteristics for ECAP.

Table 7-37. ECAP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

Table 7-38. ECAP Timing Requirements

see Figure 7-29

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP1	$t_{w(CAP)}$	Pulse duration, CAP (asynchronous)	2 + 2P(1)		ns

(1) P = sysclk period in ns.

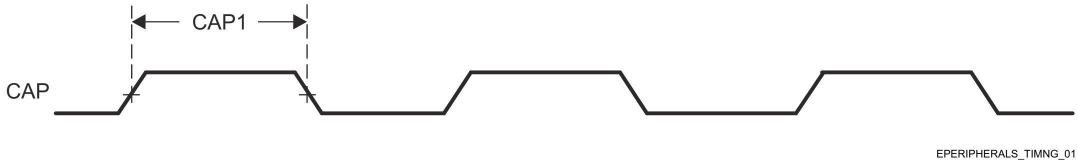


Figure 7-29. ECAP Timings Requirements

Table 7-39. ECAP Switching Characteristics

see Figure 7-30

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP2	$t_{w(APWM)}$	Pulse duration, APWMx high/low	-2 + 2P(1)		ns

(1) P = sysclk period in ns.

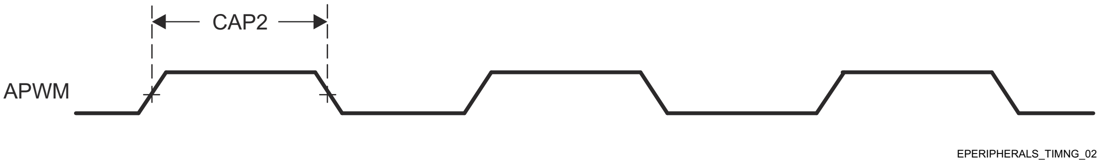


Figure 7-30. ECAP Switching Characteristics

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

7.10.5.4 EPWM

Table 7-40, Table 7-41, Figure 7-31, Table 7-42, Figure 7-32, Figure 7-33, and Figure 7-34 present timing conditions, requirements, and switching characteristics for EPWM.

Table 7-40. EPWM Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

Table 7-41. EPWM Timing Requirements

see Figure 7-31

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM6	$t_{w(SYNCIN)}$	Pulse duration, EHRPWM_SYNCI	2 + 2P(1)		ns
PWM7	$t_{w(TZ)}$	Pulse duration, EHRPWM_TZn_IN low	2 + 3P(1)		ns

(1) P = sysclk period in ns.

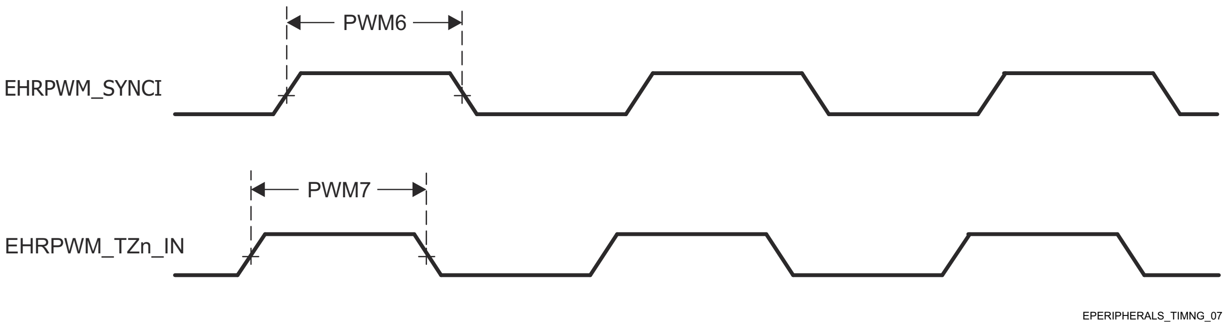


Figure 7-31. EPWM Timing Requirements

Table 7-42. EPWM Switching Characteristics

see Figure 7-32, Figure 7-33, and Figure 7-34

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM1	$t_{w(PWM)}$	Pulse duration, EHRPWM_A/B high/low	P - 3(1)		ns
PWM2	$t_{w(SYNCOUT)}$	Pulse duration, EHRPWM_SYNCO	P - 3(1)		ns
PWM3	$t_{d(TZ-PWM)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B forced high/low		11	ns
PWM4	$t_{d(TZ-PWMZ)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B Hi-Z		11	ns
PWM5	$t_{w(SOC)}$	Pulse duration, EHRPWM_SOCA/B output	P - 3(1)		ns

(1) P = sysclk period in ns.

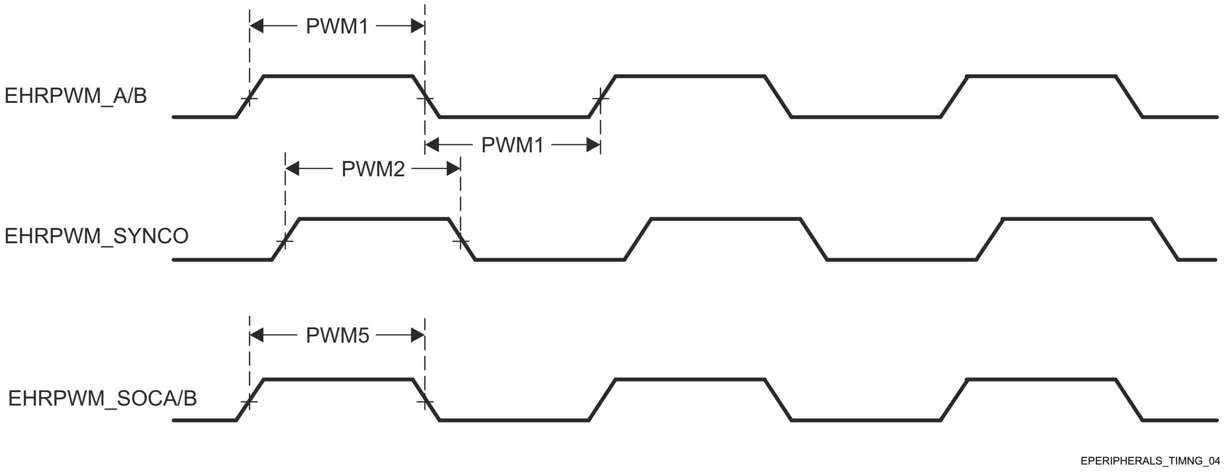


Figure 7-32. EHRPWM Switching Characteristics

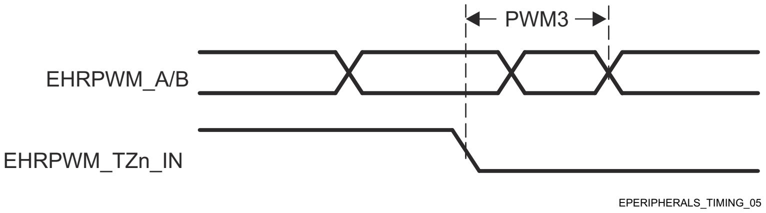


Figure 7-33. EHRPWM_TZn_IN to EHRPWM_A/B Forced Switching Characteristics

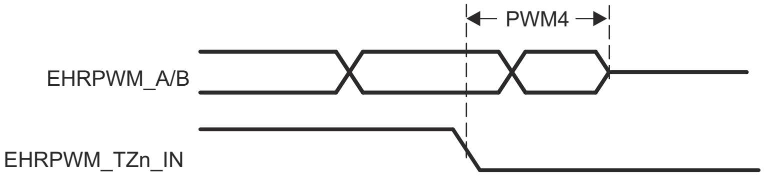


Figure 7-34. EHRPWM_TZn_IN to EHRPWM_A/B Hi-Z Switching Characteristics

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

7.10.5.5 EQEP

Table 7-43, Table 7-44, Figure 7-35, and Table 7-45 present timing conditions, requirements, and switching characteristics for EQEP.

Table 7-43. EQEP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

Table 7-44. EQEP Timing Requirements

see Figure 7-35

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP1	$t_{w(QEP)}$	Pulse duration, QEP_A/B	2 + 2P(1)		ns
QEP2	$t_{w(QEPIH)}$	Pulse duration, QEP_I high	2 + 2P(1)		ns
QEP3	$t_{w(QEPIL)}$	Pulse duration, QEP_I low	2 + 2P(1)		ns
QEP4	$t_{w(QEPSH)}$	Pulse duration, QEP_S high	2 + 2P(1)		ns
QEP5	$t_{w(QEPSL)}$	Pulse duration, QEP_S low	2 + 2P(1)		ns

(1) P = sysclk period in ns

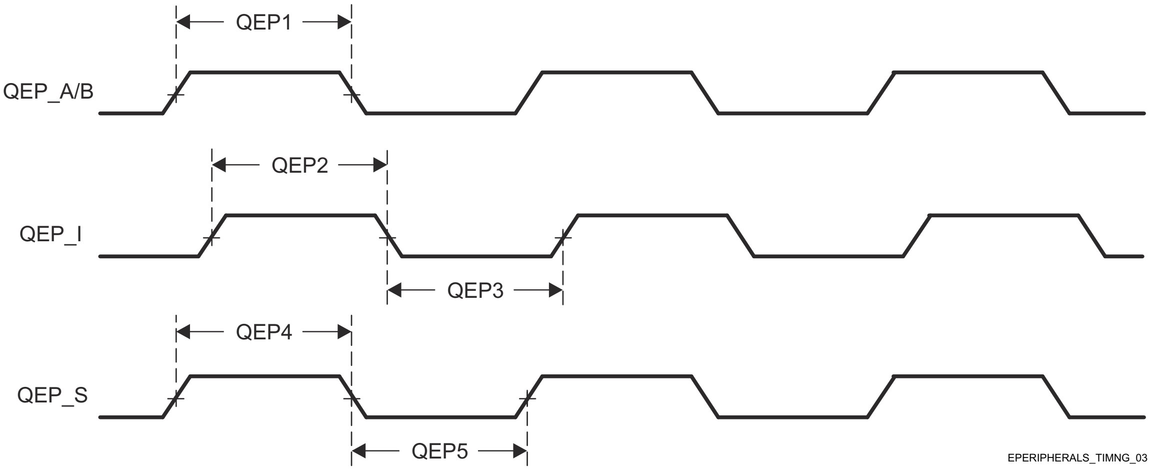


Figure 7-35. EQEP Timing Requirements

Table 7-45. EQEP Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP6	$t_{d(QEP-CNTR)}$	Delay time, external clock to counter increment		24	ns

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

7.10.5.6 FSI

Table 7-46, Table 7-47, Figure 7-36, Table 7-48, Figure 7-37, Table 7-49, and Figure 7-38 present timing conditions, requirements, and switching characteristics for FSI.

Table 7-46. FSI Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.8	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	7	pF

Table 7-47. FSI Timing Requirements

see Figure 7-36

NO.			MIN	MAX	UNIT
FSIR1	$t_{c(RX\_CLK)}$	Cycle time, FSI_RXn_CLK	20		ns
FSIR2	$t_{w(RX\_CLK)}$	Pulse width, FSI_RXn_CLK low or FSI_RXn_CLK high	0.5P - 1(1)	0.5P + 1(1)	ns
FSIR3	$t_{su(RX\_D-RX\_CLK)}$	Setup time, FSI_RXn_D[1:0] valid before FSI_RXn_CLK	3		ns
FSIR4	$t_{h(RX\_CLK-RX\_D)}$	Hold time, FSI_RXn_D[1:0] valid after FSI_RXn_CLK	2.5		ns

(1) P = FSI_RXn_CLK period in ns.

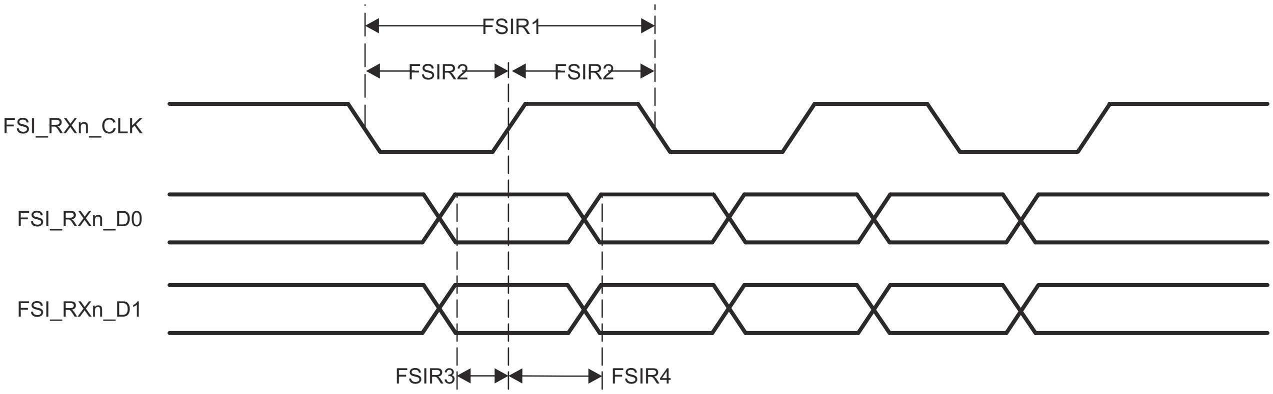


Figure 7-36. FSI Timing Requirements

Table 7-48. FSI Switching Characteristics - FSI Mode

see Figure 7-37

NO.	PARAMETER		MODE	MIN	MAX	UNIT
FSIT1	$t_{c(TX\_CLK)}$	Cycle time, FSI_TXn_CLK	FSI Mode	20		ns
FSIT2	$t_{w(TX\_CLK)}$	Pulse width, FSI_TXn_CLK low or FSI_TXn_CLK high	FSI Mode	0.5p + 1(1)	0.5P - 1(1)	ns
FSIT3	$t_{d(TX\_CLK-TX\_D)}$	Delay time, FSI_TXn_D[1:0] valid after FSI_TXn_CLK high or FSI_TXn_CLK low	FSI Mode	0.25P - 2(1)	0.25P + 2.5(1)	ns

(1) P = FSI_TXn_CLK period in ns.

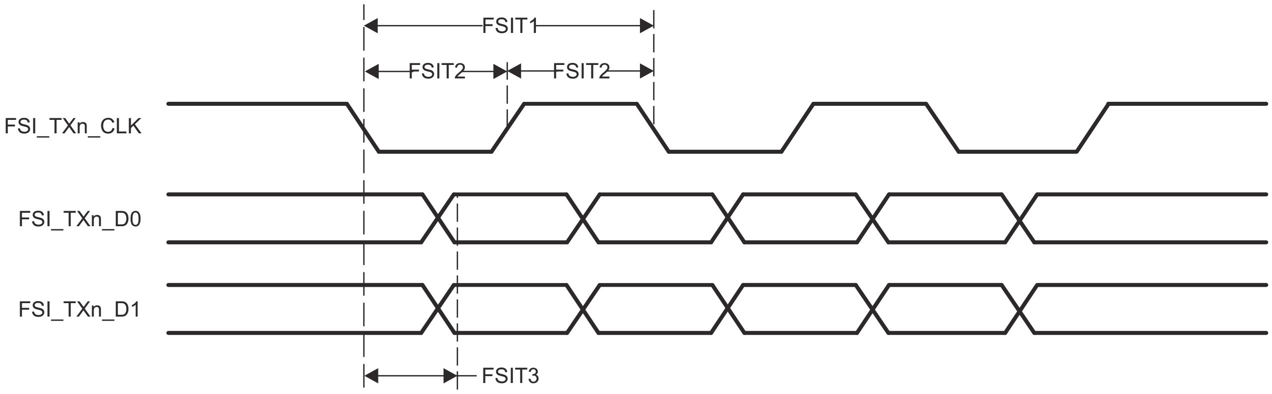


Figure 7-37. FSI Switching Characteristics - FSI Mode

Table 7-49. FSI Switching Characteristics - SPI Mode

see Figure 7-38

NO.	PARAMETER		MODE	MIN	MAX	UNIT
FSIT4	$t_{c(TX\_CLK)}$	Cycle time, FSI_TXn_CLK	SPI Mode	20		ns
FSIT5	$t_{w(TX\_CLK)}$	Pulse width, FSI_TXn_CLK low or FSI_TXn_CLK high	SPI Mode	0.5P + 1(1)	0.5P - 1(1)	ns
FSIT6	$t_{d(TX\_CLKH-TX\_D0)}$	Delay time, FSI_TXn_CLK high to FSI_TXn_D0 valid	SPI Mode		3	ns
FSIT7	$t_{d(TX\_D1-TX\_CLK)}$	Delay time, FSI_TXn_D1 low to FSI_TXn_CLK high	SPI Mode	P - 3(1)		ns
FSIT8	$t_{d(TX\_CLK-TX\_D1)}$	Delay time, FSI_TXn_CLK low to FSI_TXn_D1 high	SPI Mode	P - 2(1)		ns

(1) P = FSI_TXn_CLK period in ns.

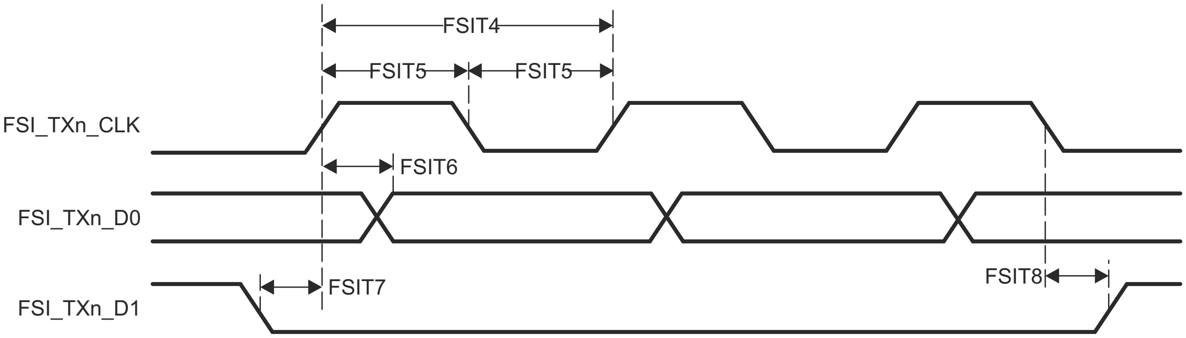


Figure 7-38. FSI Switching Characteristics - SPI Mode

For more information, see *Fast Serial Interface* section in *Peripherals* chapter in the device TRM.

7.10.5.7 GPIO

Table 7-50, Table 7-51, and Table 7-52 present timing conditions, requirements, and switching characteristics for GPIO.

The device has three instances of the GPIO module.

- MCU_GPIO0
- GPIO0
- GPIO1

Note

GPIOn_x is generic name used to describe a GPIO signal, where n represents the specific GPIO module and x represents one of the input/output signals associated with the module.

For additional description information on the device GPIO, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 7-50. GPIO Timing Conditions

PARAMETER		BUFFER TYPE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	LVCMOS	0.2	6.6	V/ns
		I2C OD FS	0.2	0.8	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	LVCMOS	3	10	pF
		I2C OD FS	3	100	pF

Table 7-51. GPIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
GPIO1	$t_{w(GPIO\_IN)}$	Pulse width, GPIOn_x	1.8 V	2P + 2.6(1)		ns
			3.3 V	2P + 3.5(1)		ns

(1) P = functional clock period in ns.

Table 7-52. GPIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
GPIO2	$t_{w(GPIO\_OUT)}$	Pulse width, GPIOn_x	LVCMOS	0.975P(1) - 3.6		ns
			I2C OD FS	160		ns

(1) P = functional clock period in ns.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

7.10.5.8 GPMC

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Note

GPMC has one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface is shown in Section 7.10.5.8.4.

Table 7-53 presents timing conditions for GPMC.

Table 7-53. GPMC Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		1.65	4	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		5	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	133 MHz Synchronous Mode	140	360	ps
		All other modes	140	720	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces			200	ps

For more information, see *General-Purpose Memory Controller (GPMC)* section in *Peripherals* chapter in the device TRM.

7.10.5.8.1 GPMC and NOR Flash — Synchronous Mode

Hold time, input wait GPMC_WAIT[j] valid after output clock GPMC_CLK high ($t_{h(clkH-waitV)}$)

Table 7-54 and Table 7-55 present timing requirements and switching characteristics for GPMC and NOR Flash - Synchronous Mode.

Table 7-54. GPMC and NOR Flash Timing Requirements — Synchronous Mode

see Figure 7-39, Figure 7-40, and Figure 7-43

NO.	PARAMETER	DESCRIPTION	MODE[5]	MIN GPMC_FCLK = 100 MHz[2]	MAX GPMC_FCLK = 100 MHz[2]	MIN GPMC_FCLK = 133 MHz[2]	MAX GPMC_FCLK = 133 MHz[2]	UNIT
F12	$t_{su(dV-clkH)}$	Setup time, input data GPMC_AD[n:0][1] valid before output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.81		1.12		ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.06		3.5		ns
F13	$t_{h(clkH-dV)}$	Hold time, input data GPMC_AD[n:0][1] valid after output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.29		2.29		ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.29		2.29		ns
F21	$t_{su(waitV-clkH)}$	Setup time, input wait GPMC_WAIT[j][3] [4] valid before output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.81		1.12		ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.06		3.5		ns

Table 7-54. GPMC and NOR Flash Timing Requirements — Synchronous Mode (continued)

see Figure 7-39, Figure 7-40, and Figure 7-43

NO.	PARAMETER	DESCRIPTION	MODE[5]	MIN	MAX	MIN	MAX	UNIT
				GPMC_FCLK = 100 MHz[2]		GPMC_FCLK = 133 MHz[2]		
F22	$t_{h(clkH-waitV)}$	Hold time, input wait GPMC_WAIT[j][3] [4] valid after output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.29		2.29		ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.29		2.29		ns

(1) Synchronous Mode supports 16-bit data bus up to 133 MHz and 32-bit data bus up to 100 MHz

(2) GPMC_FCLK select
- gpmc_fclk_sel[1:0] = 2b01 to select the 100MHz GPMC_FCLK
- gpmc_fclk_sel[1:0] = 2b00 to select the 133MHz GPMC_FCLK

(3) In GPMC_WAIT[j], j is equal to 0 or 1.

(4) Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see *General-Purpose Memory Controller (GPMC)* section in the device TRM.

(5) For div_by_1_mode:
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For not_div_by_1_mode:
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 1h to 3h:
  - GPMC_CLK frequency = GPMC_FCLK frequency / (2 to 4)

For GPMC_FCLK_MUX:
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = PER1_PLL_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY_X1:
- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

Table 7-55. GPMC and NOR Flash Switching Characteristics – Synchronous Mode

see Figure 7-39, Figure 7-40, Figure 7-41, Figure 7-42, and Figure 7-43

NO.[3]	PARAMETER	DESCRIPTION	MODE[17]	MIN	MAX	MIN	MAX	UNIT
				100 MHz		133 MHz		
F0	1 / tc(clk)	Period, output clock GPMC_CLK[16]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	10.00		7.52		ns
F1	$t_{w(clkH)}$	Typical pulse duration, output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.475P - 0.3[15]		0.475P - 0.3[15]		ns
F1	$t_{w(clkL)}$	Typical pulse duration, output clock GPMC_CLK low	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.475P - 0.3[15]		0.475P - 0.3[15]		ns
F2	$t_{d(clkH-csnV)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] transition[14]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	F - 2.2[6]	F + 3.75	F - 2.2[6]	F + 3.75	ns
F3	$t_{d(clkH-CSn[i]V)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] invalid[14]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	E - 2.2[5]	E + 3.18	E - 2.2[5]	E + 4.5	ns

Table 7-55. GPMC and NOR Flash Switching Characteristics – Synchronous Mode (continued)

see Figure 7-39, Figure 7-40, Figure 7-41, Figure 7-42, and Figure 7-43

NO. (3)	PARAMETER	DESCRIPTION	MODE(17)	MIN	MAX	MIN	MAX	UNIT
				100 MHz		133 MHz		
F4	$t_{d(aV-clk)}$	Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2.3 (3)	B + 4.5	B - 2.3 (3)	B + 4.5	ns
F5	$t_{d(clkH-aIV)}$	Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	-2.3	4.5	-2.3	4.5	ns
F6	$t_{d(be[x]nV-clk)}$	Delay time, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n valid to output clock GPMC_CLK first edge	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2.3 (3)	B + 1.9	B - 2.3 (3)	B + 1.9	ns
F7	$t_{d(clkH-be[x]nIV)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n invalid(11)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3(4)	D + 1.9	D - 2.3 (4)	D + 1.9	ns
F7	$t_{d(clkL-be[x]nIV)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid(12)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3 (4)	D + 1.9	D - 2.3 (4)	D + 1.9	ns
F7	$t_{d(clkL-be[x]nIV).}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid(13)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3 (4)	D + 1.9	D - 2.3 (4)	D + 1.9	ns
F8	$t_{d(clkH-advn)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	G - 2.3(7)	G + 4.5	G - 2.3 (7)	G + 4.5	ns
F9	$t_{d(clkH-advnIV)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	D - 2.3 (4)	D + 4.5	D - 2.3 (4)	D + 4.5	ns
F10	$t_{d(clkH-oen)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	H - 2.3(8)	H + 3.5	H - 2.3 (8)	H + 3.5	ns
F11	$t_{d(clkH-oenIV)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	H - 2.3 (8)	H + 3.5	H - 2.3 (8)	H + 3.5	ns
F14	$t_{d(clkH-wen)}$	Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	I - 2.3 (9)	I + 4.5	I - 2.3 (9)	I + 4.5	ns
F15	$t_{d(clkH-do)}$	Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[n:0](1) transition(11)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (10)	J + 2.7	J - 2.3 (10)	J + 2.7	ns
F15	$t_{d(clkL-do)}$	Delay time, GPMC_CLK falling edge to GPMC_AD[n:0](1) data bus transition(12)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (10)	J + 2.7	J - 2.3 (10)	J + 2.7	ns
F15	$t_{d(clkL-do).}$	Delay time, GPMC_CLK falling edge to GPMC_AD[n:0](1) data bus transition(13)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (10)	J + 2.7	J - 2.3 (10)	J + 2.7	ns
F17	$t_{d(clkH-be[x]n)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition(11)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (10)	J + 1.9	J - 2.3 (10)	J + 1.9	ns

Table 7-55. GPMC and NOR Flash Switching Characteristics – Synchronous Mode (continued)

see Figure 7-39, Figure 7-40, Figure 7-41, Figure 7-42, and Figure 7-43

NO.(3)	PARAMETER	DESCRIPTION	MODE(17)	MIN	MAX	MIN	MAX	UNIT
				100 MHz		133 MHz		
F17	$t_{d(clkL-be[x]n)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition(12)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3(10)	J + 1.9	J - 2.3(10)	J + 1.9	ns
F17	$t_{d(clkL-be[x]n).}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition(13)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3(10)	J + 1.9	J - 2.3(10)	J + 1.9	ns
F18	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[i](14) low	Read	A		A		ns
			Write	A		A		ns
F19	$t_{w(be[x]nV)}$	Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low	Read	C		C		ns
			Write	C		C		ns
F20	$t_{w(advnV)}$	Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low	Read	K		K		ns
			Write	K		K		ns

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(1) Synchronous Mode supports 16-bit data bus up to 133 MHz and 32-bit data bus up to 100 MHz

(2) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(15)
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(15)
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(15)
With n being the page burst access number.

(3) B = ClkActivationTime × GPMC_FCLK(15)

(4) For single read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(15)
For burst read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(15)
For burst write: D = (WrCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(15)

(5) For single read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(15)
For burst read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(15)
For burst write: E = (CSWrOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(15)

(6) For csn falling edge (CS activated):

- Case GPMCFCLKDIVIDER = 0:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(15)
- Case GPMCFCLKDIVIDER = 1:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(15) if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(15) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(15) if ((CSOnTime - ClkActivationTime) is a multiple of 3)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(15) if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
  - F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK(15) if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):

- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(15)
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(15) if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(15) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(15) if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(15) if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(15) if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(15)

- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(15) if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(15) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(15) if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(15) if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(15) if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(15)
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(15) if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(15) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(15) if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(15) if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(15) if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GPMCFCLKDIVIDER = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(15)
- Case GPMCFCLKDIVIDER = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(15) if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(15) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(15) if ((OEOnTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(15) if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(15) if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

For OE rising edge (OE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(15)
- Case GPMCFCLKDIVIDER = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(15) if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(15) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(15) if ((OEOffTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(15) if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(15) if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

(9) For WE falling edge (WE activated):

- Case GPMCFCLKDIVIDER = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(15)
- Case GPMCFCLKDIVIDER = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(15) if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(15) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(15) if ((WEOnTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(15) if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK(15) if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)

For WE rising edge (WE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK (15)
- Case GPMCFCLKDIVIDER = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(15) if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(15) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(15) if ((WEOffTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(15) if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK(15) if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)

(10) J = GPMC_FCLK(15)
(11) First transfer only for CLK DIV 1 mode.
(12) Half cycle; for all data after initial transfer for CLK DIV 1 mode.
(13) Half cycle of GPMC_CLKOUT; for all data for modes other than CLK DIV 1 mode. GPMC_CLKOUT divide down from GPMC_FCLK.
(14) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
(15) P = GPMC_CLK period in ns
(16) Related to the GPMC_CLK output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC_CONFIG1_i configuration register bit field GPMCFCLKDIVIDER.
(17) For div_by_1_mode:

- GPMC_CONFIG1_i register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

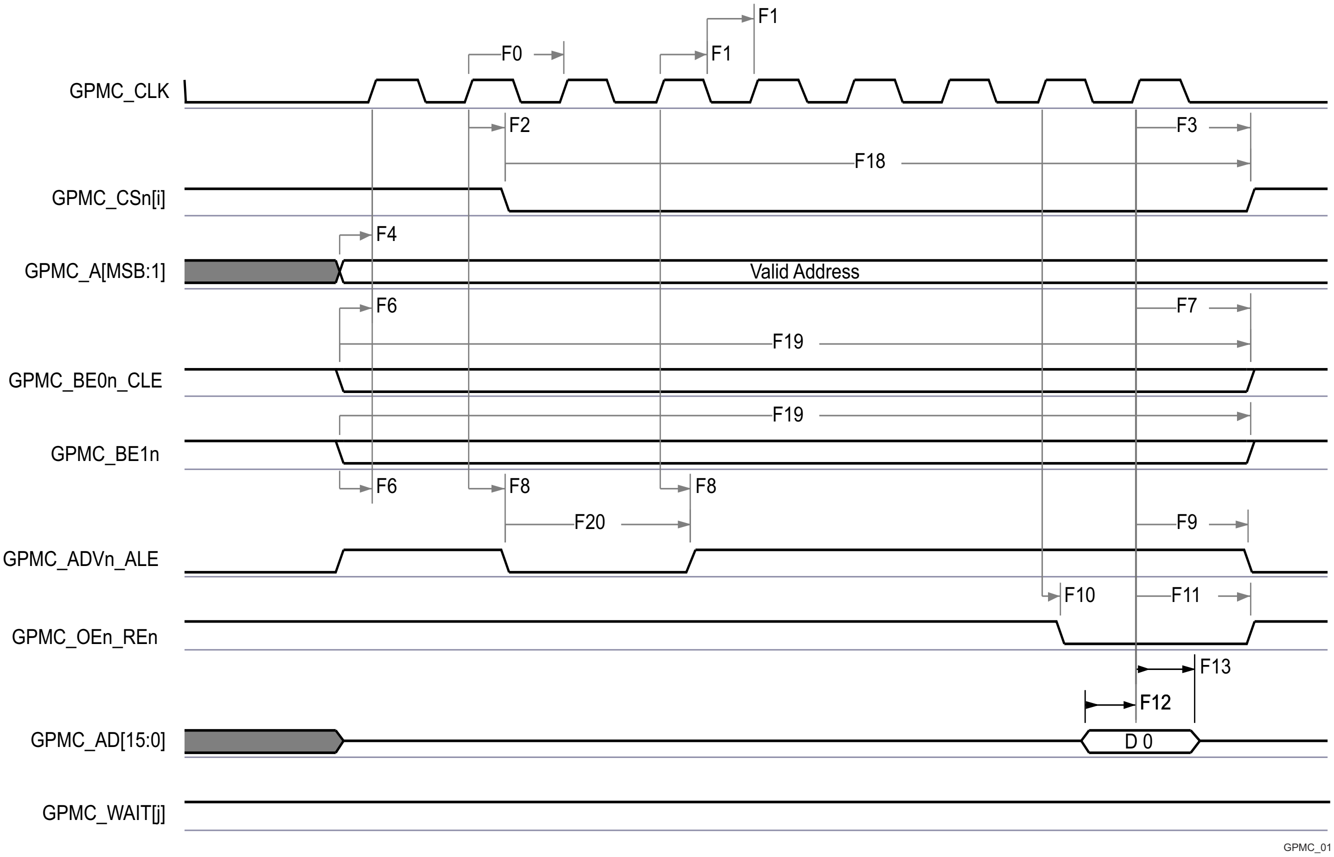
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = PER1_PLL_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

For no extra_delay:

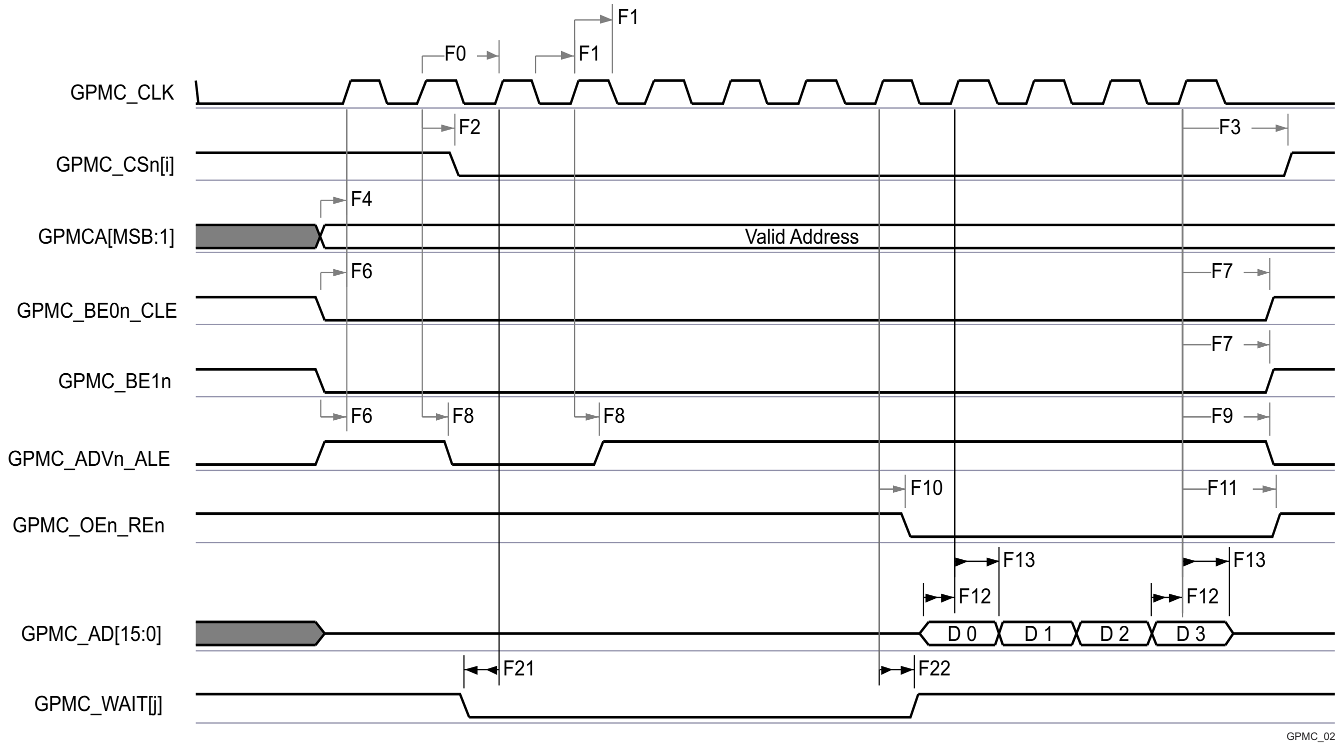
- GPMC_CONFIG2_i Register: CSEXTRADELAY = 0h = CSn Timing control signal is not delayed
- GPMC_CONFIG4_i Register: WEEXTRADELAY = 0h = nWE timing control signal is not delayed
- GPMC_CONFIG4_i Register: OEEXTRADELAY = 0h = nOE timing control signal is not delayed
- GPMC_CONFIG3_i Register: ADVEXTRADELAY = 0h = nADV timing control signal is not delayed



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

B. In GPMC_WAIT[j], j is equal to 0 or 1.

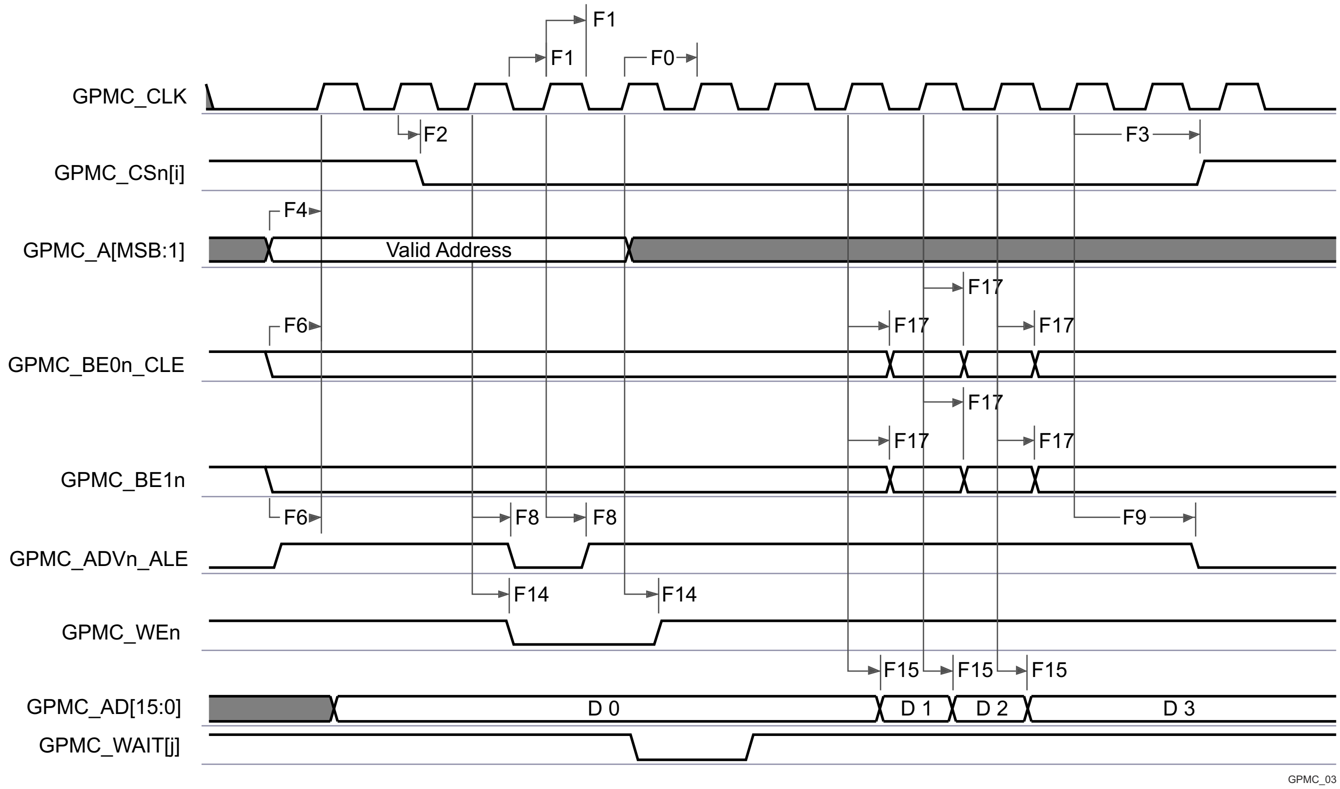
Figure 7-39. GPMC and NOR Flash — Synchronous Single Read (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

B. In GPMC_WAIT[j], j is equal to 0 or 1.

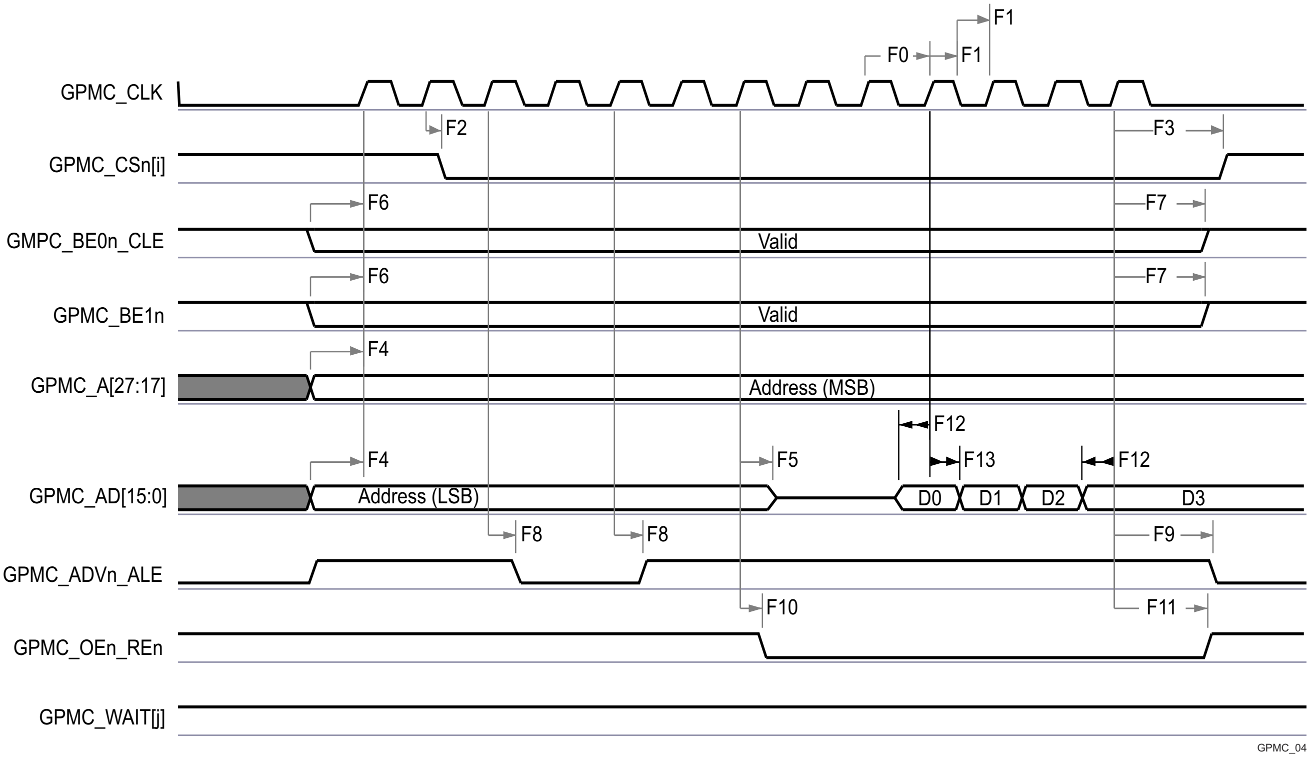
Figure 7-40. GPMC and NOR Flash — Synchronous Burst Read — 4x16–bit (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

B. In GPMC_WAIT[j], j is equal to 0 or 1.

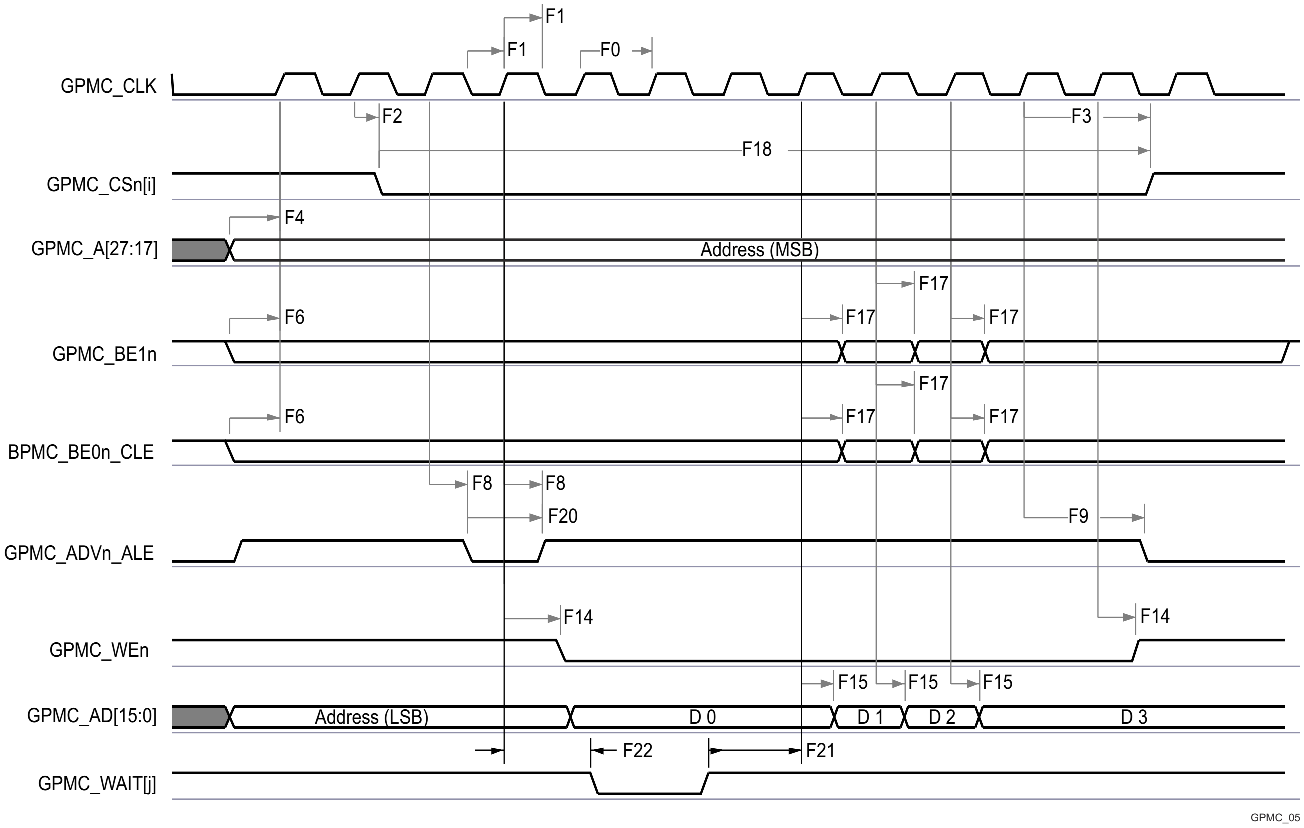
Figure 7-41. GPMC and NOR Flash—Synchronous Burst Write (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

B. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 7-42. GPMC and Multiplexed NOR Flash — Synchronous Burst Read



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

B. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 7-43. GPMC and Multiplexed NOR Flash — Synchronous Burst Write

7.10.5.8.2 GPMC and NOR Flash — Asynchronous Mode

Table 7-56 and Table 7-57 present timing requirements and switching characteristics for GPMC and NOR Flash — Asynchronous Mode.

Table 7-56. GPMC and NOR Flash Timing Requirements – Asynchronous Mode

see Figure 7-44, Figure 7-45, Figure 7-46, and Figure 7-48

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
FA5(1)	$t_{acc(d)}$	Data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H(4)	ns
FA20(2)	$t_{acc1\text{-}pgmode(d)}$	Page mode successive data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		P(3)	ns
FA21(1)	$t_{acc2\text{-}pgmode(d)}$	Page mode first data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H(4)	ns

(1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
(2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
(3) P = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(5)
(4) H = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(5)
(5) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

Table 7-57. GPMC and NOR Flash Switching Characteristics – Asynchronous Mode

see Figure 7-44, Figure 7-45, Figure 7-46, Figure 7-47, Figure 7-48, and Figure 7-49

NO.	PARAMETER	DESCRIPTION	MODE(15)	MIN	MAX	UNIT
				133 MHz		
FA0	$t_{w(be[x]nV)}$	Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time	Read		N (12)	ns
			Write		N (12)	
FA1	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[i](13) low	Read		A (1)	ns
			Write		A (1)	
FA3	$t_{d(csnV\text{-}advnIV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output address valid and address latch enable GPMC_ADVn_ALE invalid	Read	B - 2.1 (2)	B + 2.1 (2)	ns
			Write	B - 2.1 (2)	B + 2.1 (2)	
FA4	$t_{d(csnV\text{-}oenIV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output enable GPMC_OEn_REn invalid (Single read)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2.1 (3)	C + 2.1 (3)	ns
FA9	$t_{d(aV\text{-}csnV)}$	Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CSn[i](13) valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.1 (9)	J + 2.1 (9)	ns
FA10	$t_{d(be[x]nV\text{-}csnV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CSn[i](13) valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.1 (9)	J + 2.1 (9)	ns
FA12	$t_{d(csnV\text{-}advnV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output address valid and address latch enable GPMC_ADVn_ALE valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	K - 2.1 (10)	K + 2.1 (10)	ns
FA13	$t_{d(csnV\text{-}oenV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	L - 2.1 (11)	L + 2.1 (11)	ns
FA16	$t_{w(aIV)}$	Pulse duration output address GPMC_A[26:1] invalid between 2 successive read and write accesses	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	G (7)		ns

Table 7-57. GPMC and NOR Flash Switching Characteristics – Asynchronous Mode (continued)

see Figure 7-44, Figure 7-45, Figure 7-46, Figure 7-47, Figure 7-48, and Figure 7-49

NO.	PARAMETER	DESCRIPTION	MODE(15)	MIN	MAX	UNIT
				133 MHz		
FA18	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output enable GPMC_OEn_REn invalid (Burst read)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	I - 2.1 (8)	I + 2.1 (8)	ns
FA20	$t_{w(aV)}$	Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D (4)		ns
FA25	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	E - 2.1 (5)	E + 2.1 (5)	ns
FA27	$t_{d(csnV-wenIV)}$	Delay time, output chip select GPMC_CSn[i](13) valid to output write enable GPMC_WEn invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2.1 (6)	F + 2.1 (6)	ns
FA28	$t_{d(wenV-dV)}$	Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2.1	ns
FA29	$t_{d(dV-csnV)}$	Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CSn[i](13) valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.1 (9)	J + 2.1 (9)	ns
FA37	$t_{d(oenV-aIV)}$	Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2.1	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For single write: A = (CSWrOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
with n being the page burst access number
(2) For reading: B = ((ADVRdOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
For writing: B = ((ADVWrOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
(3) C = ((OEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
(4) D = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(14)
(5) E = ((WEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
(6) F = ((WEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
(7) G = Cycle2CycleDelay × GPMC_FCLK(14)
(8) I = ((OEOffTime + (n - 1) × PageBurstAccessTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
(9) J = (CSOnTime × (TimeParaGranularity + 1) + 0.5 × CSExtraDelay) × GPMC_FCLK(14)
(10) K = ((ADVOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
(11) L = ((OEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
(12) For single read: N = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For single write: N = WrCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: N = (RdCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: N = (WrCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
(13) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(15) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

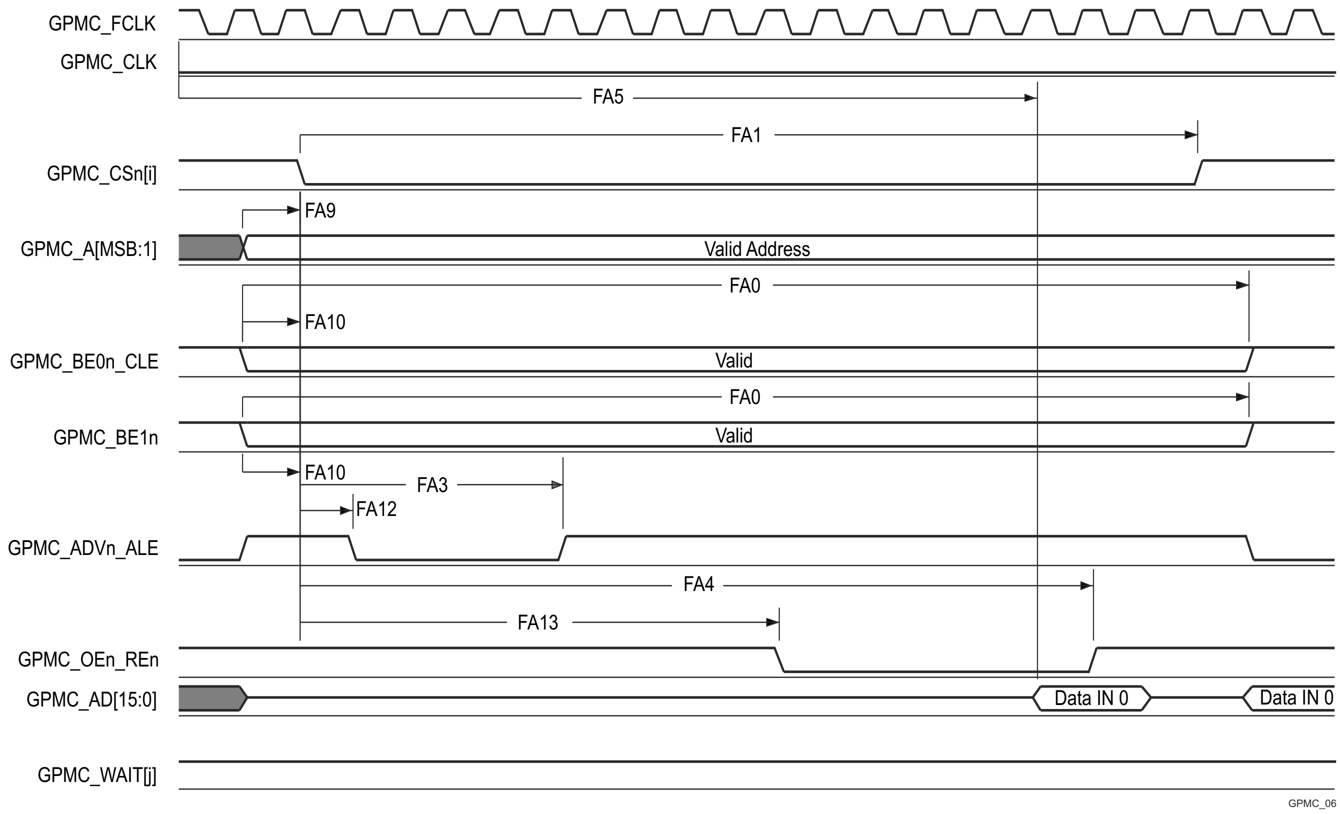
For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY_X1:

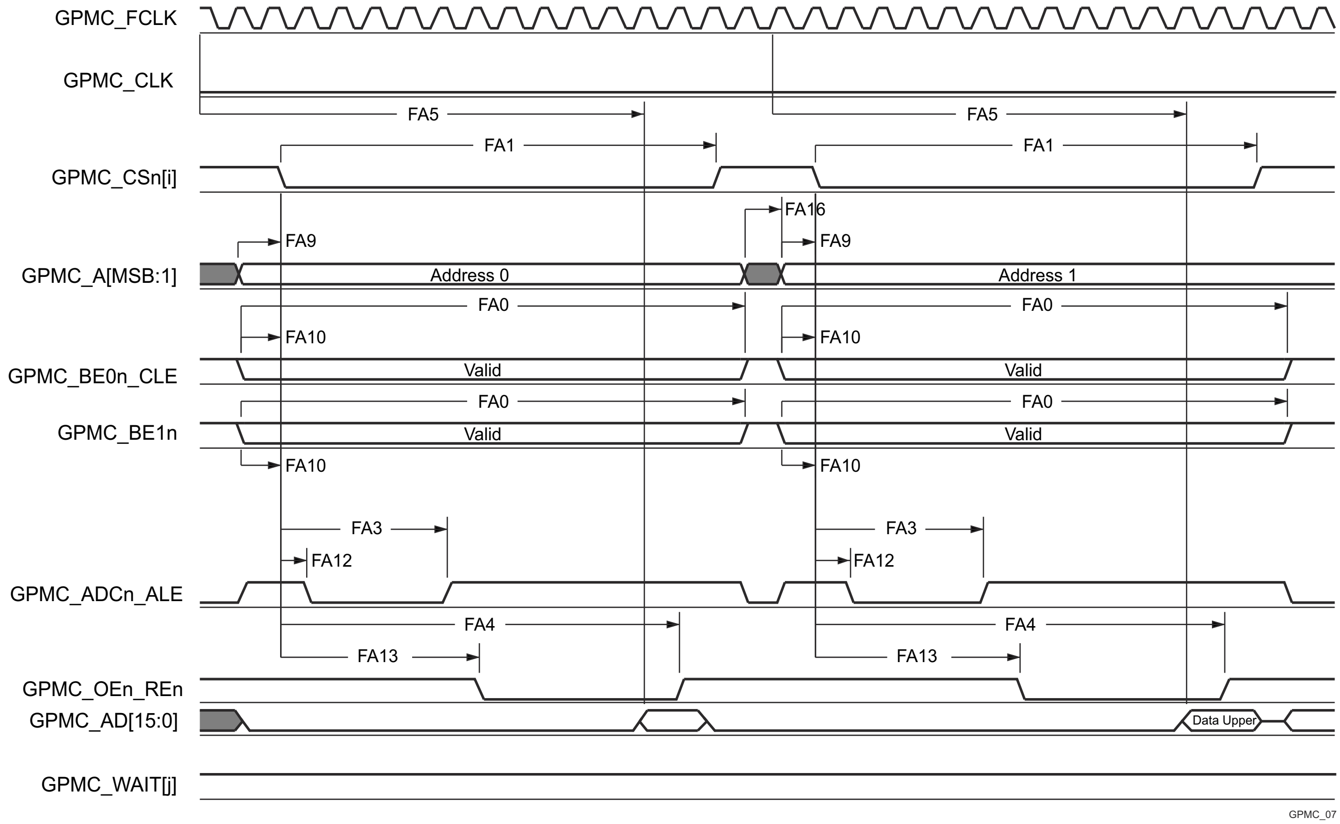
- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME,

OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], jis equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 7-44. GPMC and NOR Flash — Asynchronous Read — Single Word

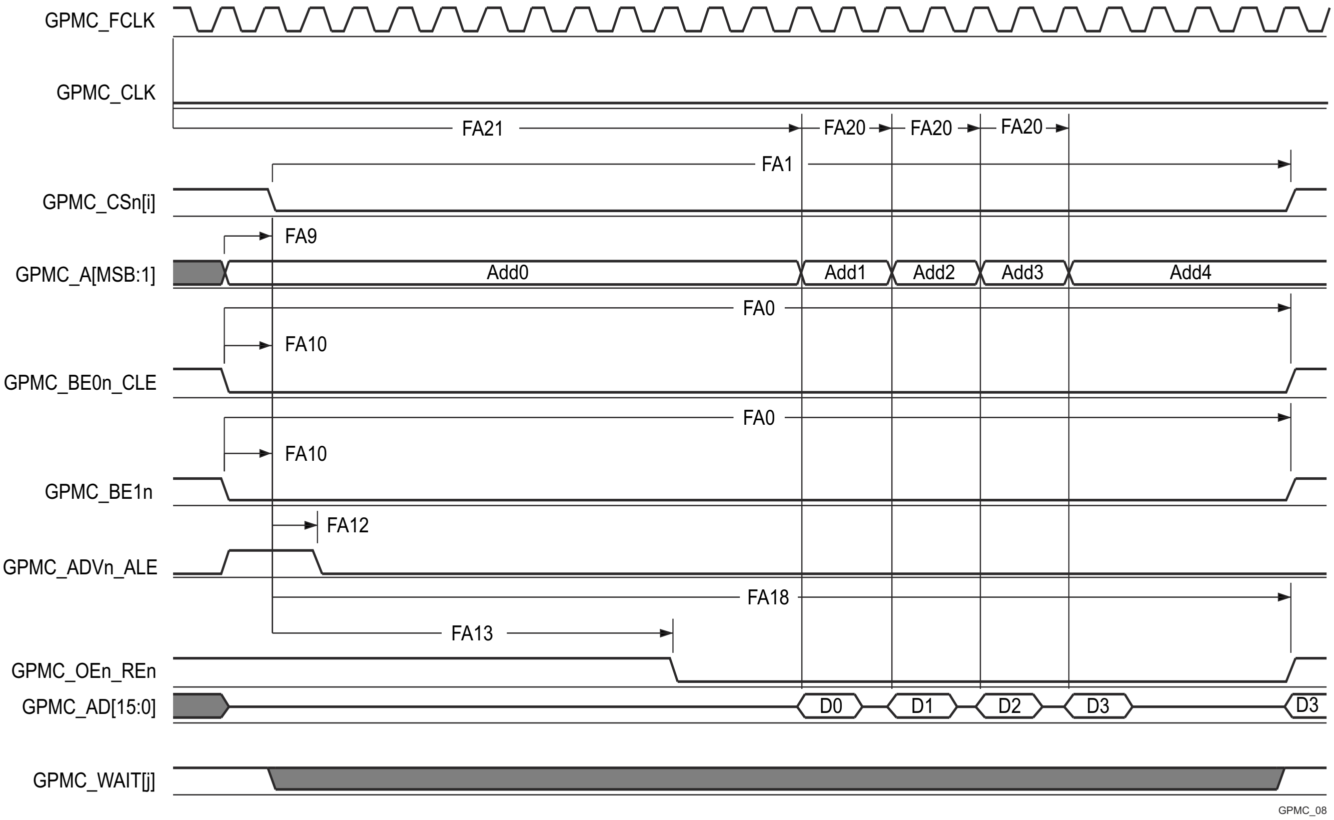


A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 7-45. GPMC and NOR Flash — Asynchronous Read — 32–Bit



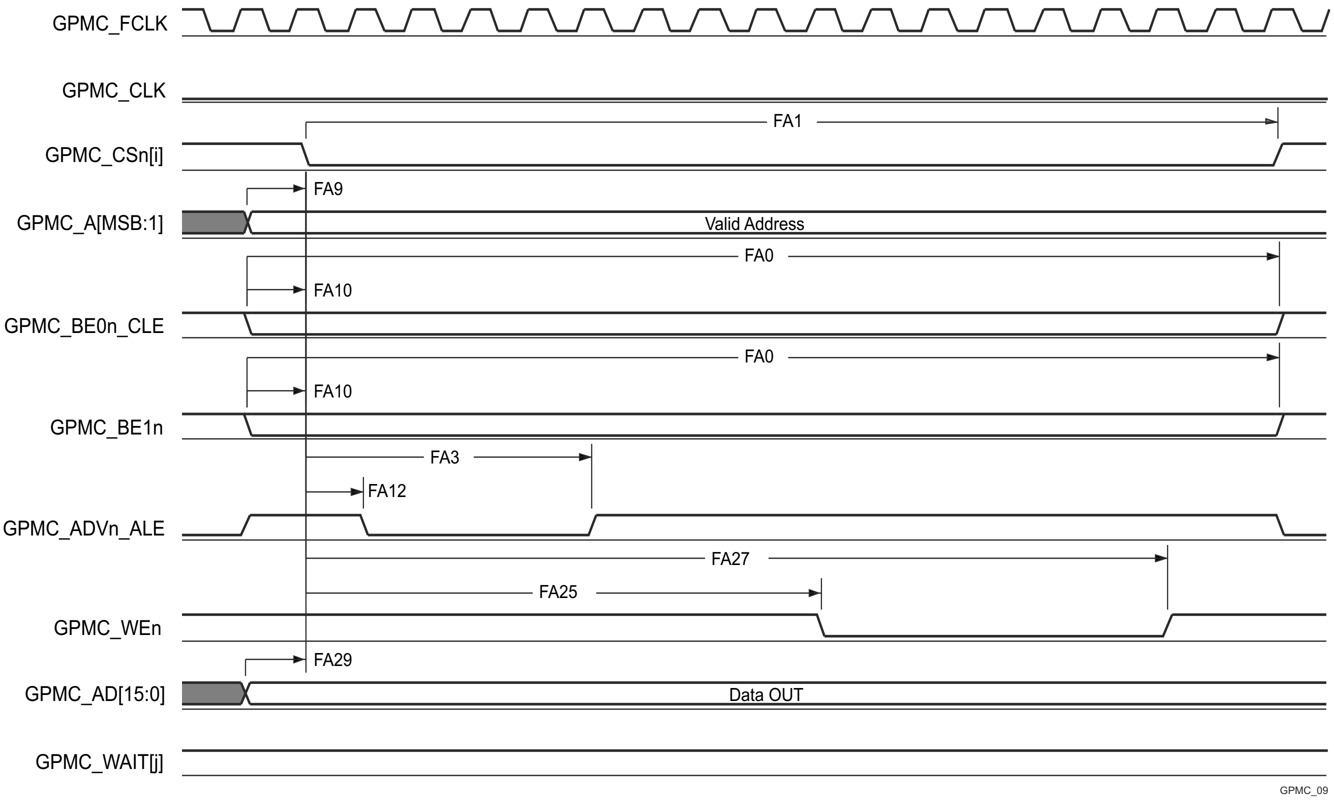
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

B. FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.

C. FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.

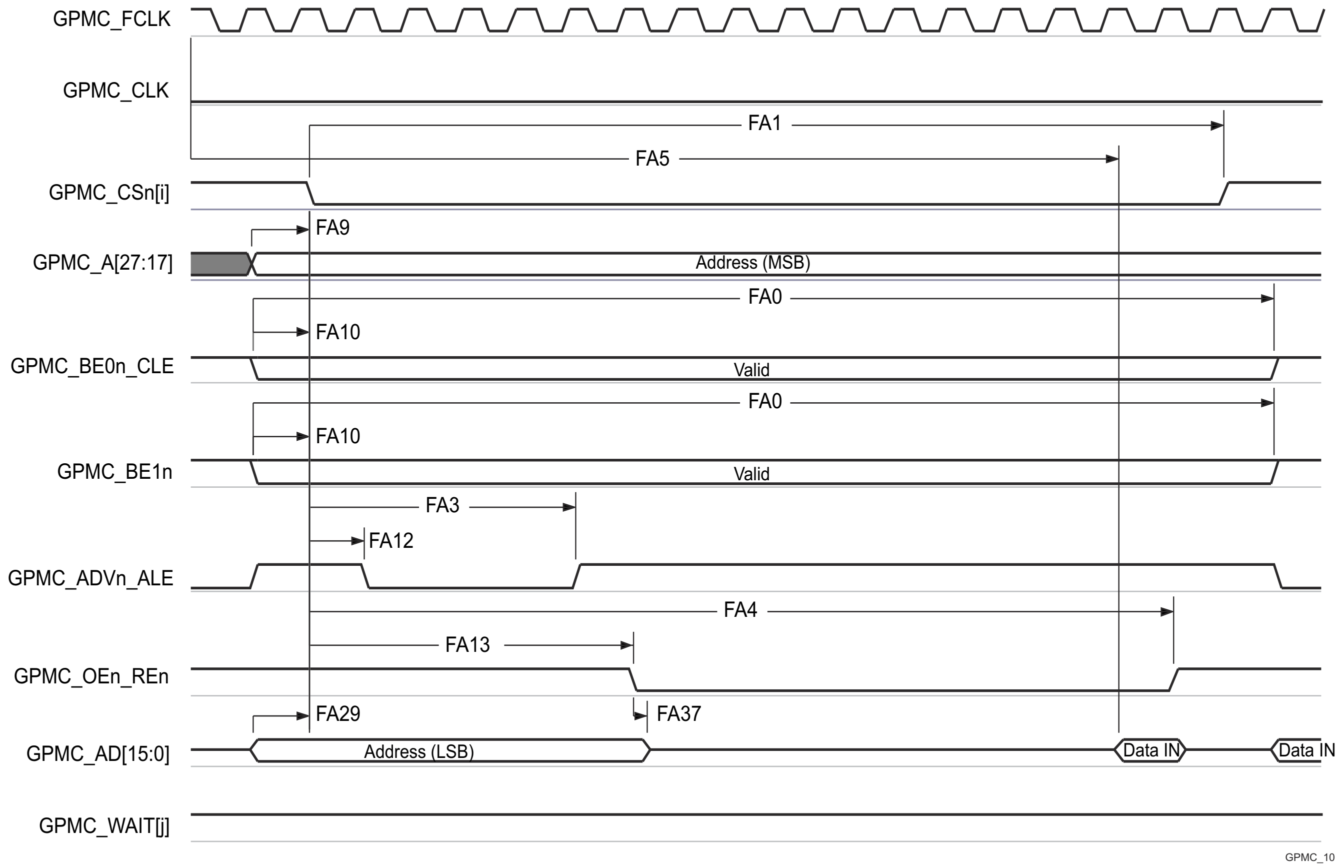
D. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 7-46. GPMC and NOR Flash — Asynchronous Read — Page Mode 4x16–Bit



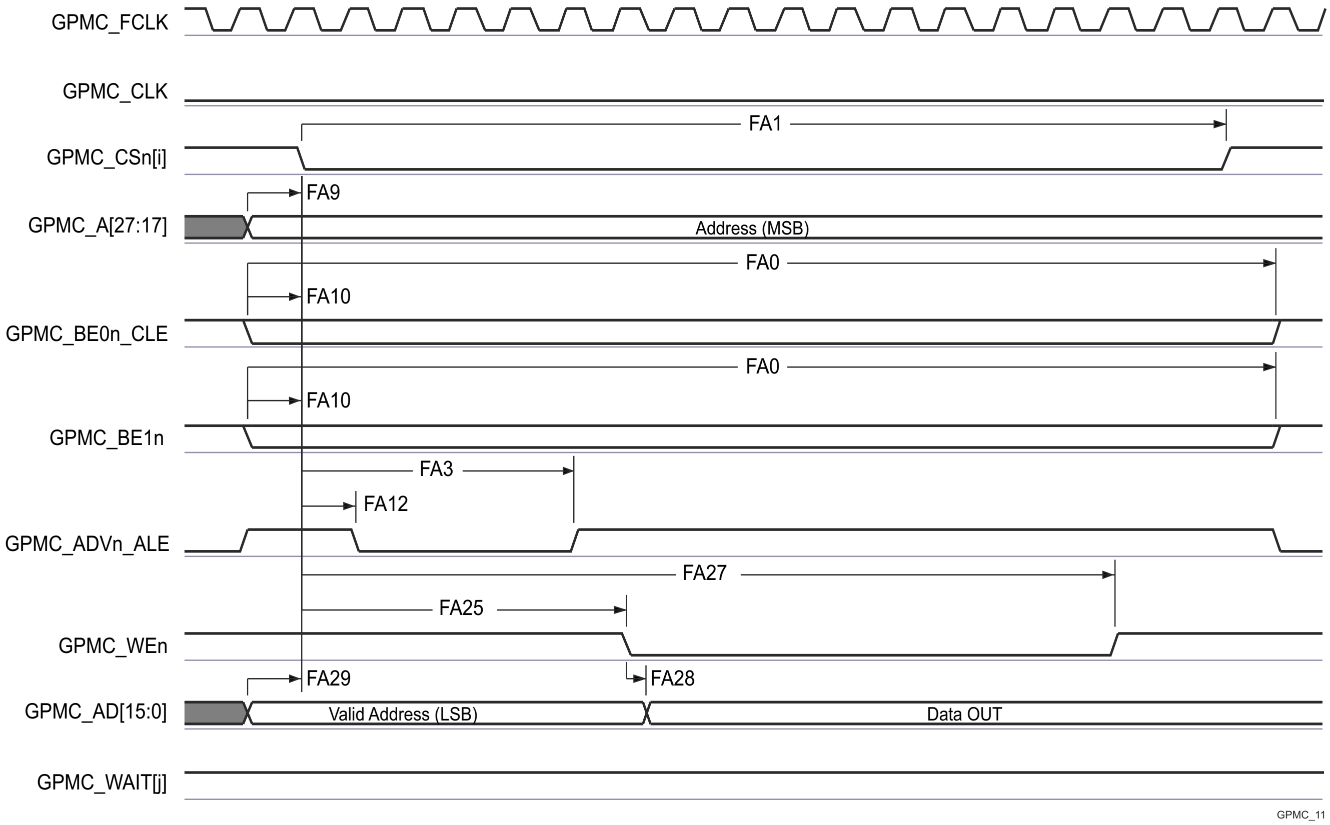
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 7-47. GPMC and NOR Flash — Asynchronous Write — Single Word



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 7-48. GPMC and Multiplexed NOR Flash — Asynchronous Read — Single Word



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 7-49. GPMC and Multiplexed NOR Flash — Asynchronous Write — Single Word

7.10.5.8.3 GPMC and NAND Flash — Asynchronous Mode

Table 7-58 and Table 7-59 present timing requirements and switching characteristics for GPMC and NAND Flash — Asynchronous Mode.

Table 7-58. GPMC and NAND Flash Timing Requirements – Asynchronous Mode

see Figure 7-52

NO.	PARAMETER	DESCRIPTION	MODE[4]	MIN	MAX	UNIT
				133 MHz		
GNF12[1]	$t_{acc(d)}$	Access time, input data GPMC_AD[15:0][3]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		J[2]	ns

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
(2) J = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[3]
(3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(4) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

Table 7-59. GPMC and NAND Flash Switching Characteristics – Asynchronous Mode

see Figure 7-50, Figure 7-51, Figure 7-52 and Figure 7-53

NO.	PARAMETER		MODE[4]	MIN	MAX	UNIT
GNF0	$t_{w(wenV)}$	Pulse duration, output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	A		ns
GNF1	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CSn[i][2] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2	B + 2	ns
GNF2	$t_{w(cleH-wenV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2	C + 2	ns
GNF3	$t_{w(wenV-dV)}$	Delay time, output data GPMC_AD[15:0] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2	D + 2	ns
GNF4	$t_{w(wenIV-dIV)}$	Delay time, output write enable GPMC_WEn invalid to output data GPMC_AD[15:0] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	E - 2	E + 2	ns
GNF5	$t_{w(wenIV-cleIV)}$	Delay time, output write enable GPMC_WEn invalid to output lower-byte enable and command latch enable GPMC_BE0n_CLE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2	F + 2	ns
GNF6	$t_{w(wenIV-CSn[i]V)}$	Delay time, output write enable GPMC_WEn invalid to output chip select GPMC_CSn[i][2] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	G - 2	G + 2	ns
GNF7	$t_{w(aleH-wenV)}$	Delay time, output address valid and address latch enable GPMC_ADVn_ALE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2	C + 2	ns

Table 7-59. GPMC and NAND Flash Switching Characteristics – Asynchronous Mode (continued)

see Figure 7-50, Figure 7-51, Figure 7-52 and Figure 7-53

NO.	PARAMETER		MODE[4]	MIN	MAX	UNIT
GNF8	$t_{w(wenIV-aleIV)}$	Delay time, output write enable GPMC_WEn invalid to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2	F + 2	ns
GNF9	$t_{c(wen)}$	Cycle time, write	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H	ns
GNF10	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CSn[i][2] valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	I - 2	I + 2	ns
GNF13	$t_{w(oenV)}$	Pulse duration, output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		K	ns
GNF14	$t_{c(oen)}$	Cycle time, read	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	L		ns
GNF15	$t_{w(oenIV-CSn[i]V)}$	Delay time, output enable GPMC_OEn_REn invalid to output chip select GPMC_CSn[i][2] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	M - 2	M + 2	ns

(1) A = (WEOffTime - WEOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[3]
(2) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
(3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(4) For div_by_1_mode:

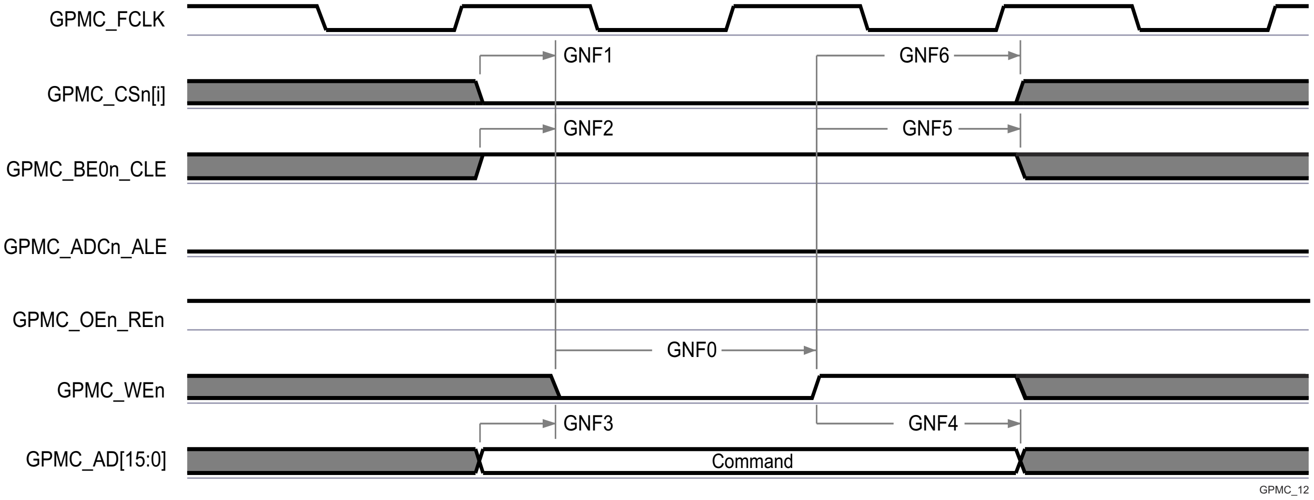
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33 MHz

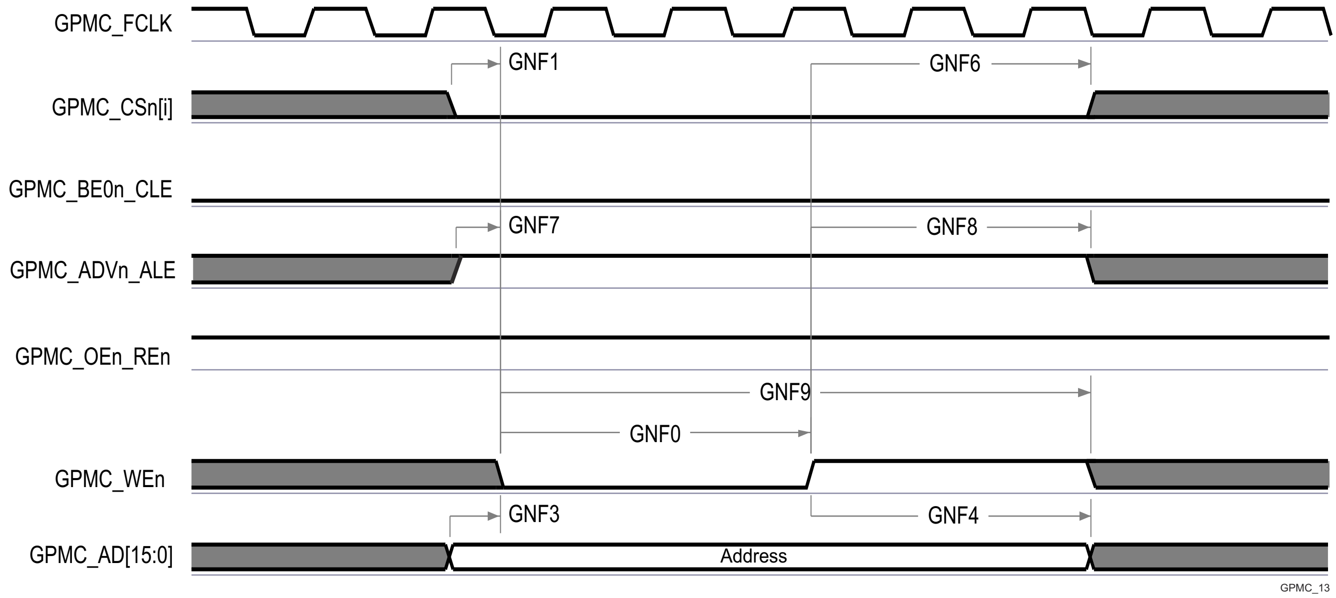
For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



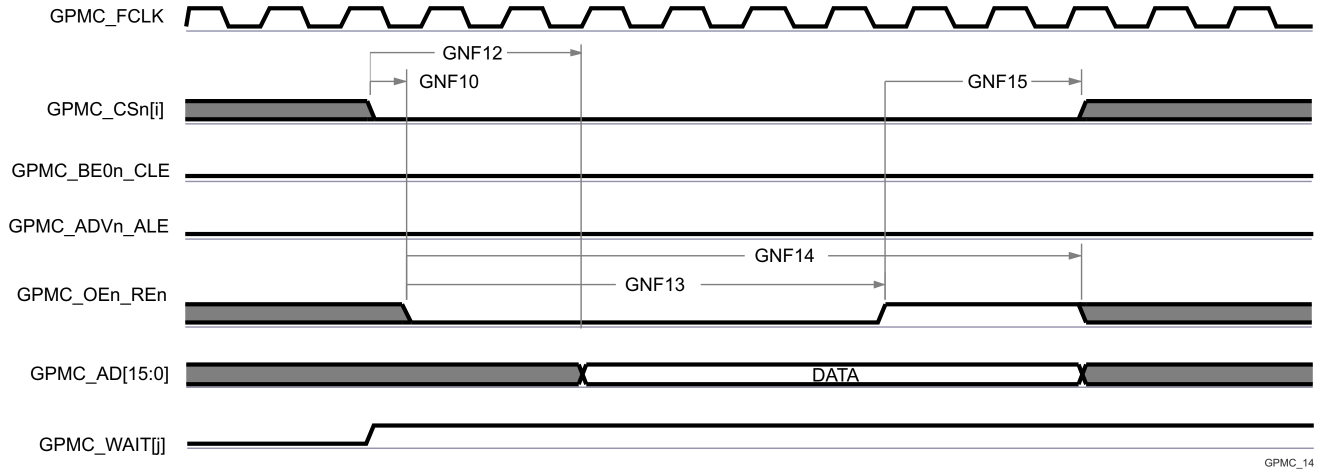
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

Figure 7-50. GPMC and NAND Flash — Command Latch Cycle



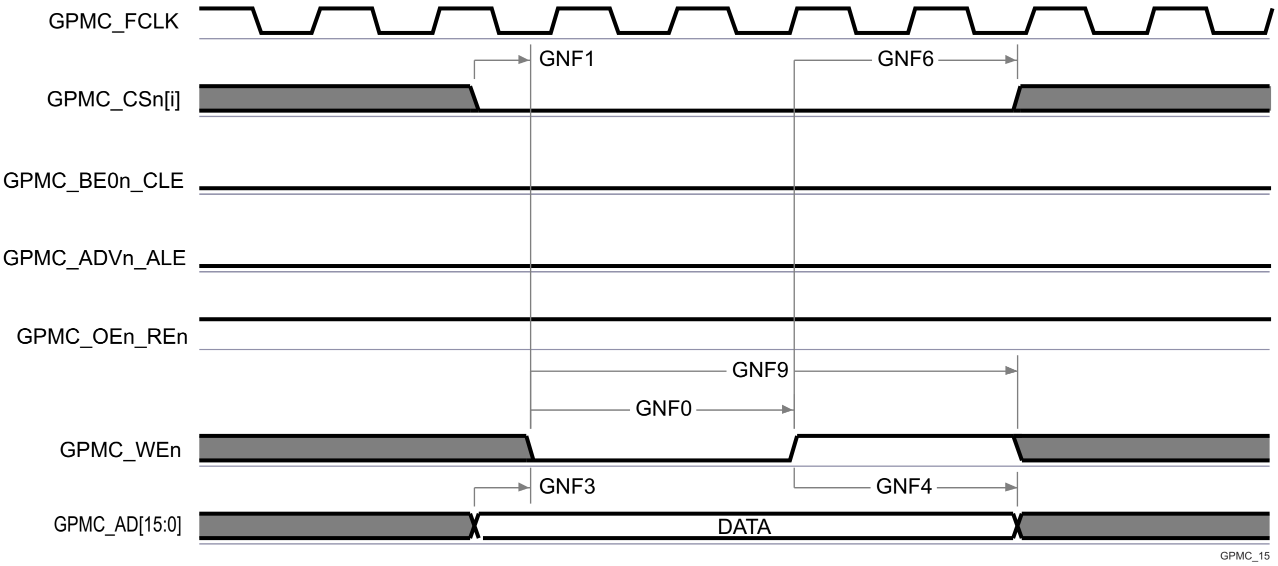
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

Figure 7-51. GPMC and NAND Flash — Address Latch Cycle



A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
B. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
C. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 7-52. GPMC and NAND Flash — Data Read Cycle



A. `In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

Figure 7-53. GPMC and NAND Flash — Data Write Cycle

7.10.5.8.4 GPMC0 IOSETs

Table 7-60 defines valid pin combinations of each GPMC0 IOSET.

Table 7-60. GPMC0 IOSETs

SIGNALS	IOSET1		IOSET2	
	BALL NAME	MUXMODE	BALL NAME	MUXMODE
GPMC0_AD0	GPMC0_AD0	0	GPMC0_AD0	0
GPMC0_AD1	GPMC0_AD1	0	GPMC0_AD1	0
GPMC0_AD2	GPMC0_AD2	0	GPMC0_AD2	0
GPMC0_AD3	GPMC0_AD3	0	GPMC0_AD3	0
GPMC0_AD4	GPMC0_AD4	0	GPMC0_AD4	0
GPMC0_AD5	GPMC0_AD5	0	GPMC0_AD5	0
GPMC0_AD6	GPMC0_AD6	0	GPMC0_AD6	0
GPMC0_AD7	GPMC0_AD7	0	GPMC0_AD7	0
GPMC0_AD8	GPMC0_AD8	0	GPMC0_AD8	0
GPMC0_AD9	GPMC0_AD9	0	GPMC0_AD9	0
GPMC0_AD10	GPMC0_AD10	0	GPMC0_AD10	0
GPMC0_AD11	GPMC0_AD11	0	GPMC0_AD11	0
GPMC0_AD12	GPMC0_AD12	0	GPMC0_AD12	0
GPMC0_AD13	GPMC0_AD13	0	GPMC0_AD13	0
GPMC0_AD14	GPMC0_AD14	0	GPMC0_AD14	0
GPMC0_AD15	GPMC0_AD15	0	GPMC0_AD15	0
GPMC0_CLK	GPMC0_CLK	0	GPMC0_CLK	0
GPMC0_ADVn_ALE	GPMC0_ADVn_ALE	0	GPMC0_ADVn_ALE	0
GPMC0_OEn_REn	GPMC0_OEn_REn	0	GPMC0_OEn_REn	0
GPMC0_WEn	GPMC0_WEn	0	GPMC0_WEn	0
GPMC0_BE0n_CLE	GPMC0_BE0n_CLE	0	GPMC0_BE0n_CLE	0
GPMC0_BE1n	GPMC0_BE1n	0	GPMC0_BE1n	0
GPMC0_WAIT0	GPMC0_WAIT0	0	GPMC0_WAIT0	0
GPMC0_WAIT1	GPMC0_WAIT1	0	GPMC0_WAIT1	0
GPMC0_WPn	GPMC0_WPn	0	GPMC0_WPn	0
GPMC0_DIR	GPMC0_DIR	0	GPMC0_DIR	0
GPMC0_CSn0	GPMC0_CSn0	0	GPMC0_CSn0	0
GPMC0_CSn1	GPMC0_CSn1	0	GPMC0_CSn1	0
GPMC0_CSn2	GPMC0_CSn2	0	GPMC0_CSn2	0
GPMC0_CSn3	GPMC0_CSn3	0	GPMC0_CSn3	0
GPMC0_AD16	PRG1_PRU0_GPO0	8	PRG1_PRU0_GPO0	8
GPMC0_AD17	PRG1_PRU0_GPO1	8	PRG1_PRU0_GPO1	8
GPMC0_AD18	PRG1_PRU0_GPO2	8	PRG1_PRU0_GPO2	8
GPMC0_AD19	PRG1_PRU0_GPO3	8	PRG1_PRU0_GPO3	8
GPMC0_AD20	PRG1_PRU0_GPO4	8	PRG1_PRU0_GPO4	8
GPMC0_AD21	PRG1_PRU0_GPO5	8	PRG1_PRU0_GPO5	8
GPMC0_AD22	PRG1_PRU0_GPO6	8	PRG1_PRU0_GPO6	8
GPMC0_AD23	PRG1_PRU0_GPO7	8	PRG1_PRU0_GPO7	8
GPMC0_AD24	PRG1_PRU0_GPO8	8	PRG1_PRU0_GPO8	8
GPMC0_AD25	PRG1_PRU0_GPO9	8	PRG1_PRU0_GPO9	8
GPMC0_AD26	PRG1_PRU0_GPO10	8	PRG1_PRU0_GPO10	8

Table 7-60. GPMC0 IOSETs (continued)

SIGNALS	IOSET1		IOSET2	
	BALL NAME	MUXMODE	BALL NAME	MUXMODE
GPMC0_AD27	PRG1_PRU0_GPO11	8	PRG1_PRU0_GPO11	8
GPMC0_AD28	PRG1_PRU0_GPO12	8	PRG1_PRU0_GPO12	8
GPMC0_AD29	PRG1_PRU0_GPO13	8	PRG1_PRU0_GPO13	8
GPMC0_AD30	PRG1_PRU0_GPO14	8	PRG1_PRU0_GPO14	8
GPMC0_AD31	PRG1_PRU0_GPO15	8	PRG1_PRU0_GPO15	8
GPMC0_BE2n	PRG1_PRU0_GPO16	8	PRG1_PRU0_GPO16	8
GPMC0_A0	PRG1_PRU0_GPO17	8	PRG0_PRU0_GPO2	9
GPMC0_A1	PRG1_PRU0_GPO18	8	PRG0_PRU0_GPO4	9
GPMC0_A2	PRG1_PRU0_GPO19	8	PRG0_PRU0_GPO8	9
GPMC0_A3	PRG1_PRU1_GPO0	8	PRG0_PRU0_GPO14	9
GPMC0_A4	PRG1_PRU1_GPO1	8	PRG0_PRU0_GPO16	9
GPMC0_A5	PRG1_PRU1_GPO2	8	PRG0_PRU0_GPO18	9
GPMC0_A6	PRG1_PRU1_GPO3	8	PRG0_PRU0_GPO19	9
GPMC0_A7	PRG1_PRU1_GPO4	8	PRG0_PRU1_GPO12	9
GPMC0_A8	PRG1_PRU1_GPO5	8	PRG0_PRU1_GPO13	9
GPMC0_A9	PRG1_PRU1_GPO6	8	PRG0_PRU1_GPO14	9
GPMC0_A10	PRG1_PRU1_GPO7	8	PRG0_PRU1_GPO15	9
GPMC0_A11	PRG1_PRU1_GPO8	8	PRG0_PRU1_GPO16	9
GPMC0_A12	PRG1_PRU1_GPO9	8	PRG0_MDIO0_MDIO	9
GPMC0_A13	PRG1_PRU1_GPO10	8	PRG0_MDIO0_MDC	9
GPMC0_A14	PRG1_PRU1_GPO11	8	PRG0_PRU0_GPO12	9
GPMC0_A15	PRG1_PRU1_GPO12	8	PRG0_PRU0_GPO13	9
GPMC0_A16	PRG1_PRU1_GPO13	8	PRG0_PRU0_GPO15	9
GPMC0_A17	PRG1_PRU1_GPO14	8	PRG0_PRU0_GPO17	9
GPMC0_A18	PRG1_PRU1_GPO15	8	PRG0_PRU1_GPO3	9
GPMC0_A19	PRG1_PRU1_GPO16	8	PRG0_PRU1_GPO6	9
GPMC0_BE3n	PRG1_PRU1_GPO17	8	PRG1_PRU1_GPO17	8
GPMC0_A20	GPMC0_CSn3	4	GPMC0_CSn3	4
GPMC0_A21	GPMC0_WAIT1	4	GPMC0_WAIT1	4
GPMC0_A22	GPMC0_WPn	4	GPMC0_WPn	4

7.10.5.9 I2C

The device contains six multicontroller Inter-Integrated Circuit (I2C) controllers. Each I2C controller was designed to be compliant to the Philips I^2C-bus™ specification version 2.1. However, the device IOs are not fully compliant to the I2C electrical specification. The speeds supported and exceptions are described per port below:

- MCU_I2C1, I2C1, I2C2, and I2C3
    - Speeds:
        - Standard-mode (up to 100 Kbits/s)
            - 1.8 V
            - 3.3 V
        - Fast-mode (up to 400 Kbits/s)
            - 1.8 V
            - 3.3 V
    - Exceptions:
        - The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification because they are implemented with higher performance LVCMOS push-pull IOs that were designed to support other signal functions that could not be implemented with I2C compatible IOs. The LVCMOS IOs being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.
        - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5 V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.
- MCU_I2C0 and I2C0
    - Speeds:
        - Standard-mode (up to 100 Kbits/s)
            - 1.8 V
            - 3.3 V
        - Fast-mode (up to 400 Kbits/s)
            - 1.8 V
            - 3.3 V
        - Hs-mode (up to 3.4 Mbit/s)
            - 1.8 V
    - Exceptions:
        - The IOs associated with these ports were not design to support Hs-mode while operating at 3.3 V. So Hs-mode is limited to 1.8-V operation.
        - The rise and fall times of the I2C signals connected to these ports must not exceed a slew rate of 0.8 V/ns (or 8E+7 V/s). This limit is more restrictive than the minimum fall time limits defined in the I2C specification. Therefore, it may be necessary to add additional capacitance to the I2C signals to slow the rise and fall times such that they do not exceed a slew rate of 0.8 V/ns.
        - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5 V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.

Refer to the Philips I2C-bus specification version 2.1 for timing details.

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

7.10.5.10 MCAN

Table 7-61 and Table 7-62 presents timing conditions and switching characteristics for MCAN.

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Note

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

Table 7-61. MCAN Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	2	15	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	5	20	pF

Table 7-62. MCAN Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MCAN1	$t_{d(MCAN\_TX)}$	Delay time, transmit shift register to MCANn_TX		10	ns
MCAN2	$t_{d(MCAN\_RX)}$	Delay time, MCANn_RX to receive shift register		10	ns

For more information, see *Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

7.10.5.11 MCSPI

For more details about features and additional description information on the device Serial Port Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 7-63 presents timing conditions for MCSPI.

Table 7-63. MCSPI Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	2	8.5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	6	12	pF

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

7.10.5.11.1 MCSPI — Controller Mode

Table 7-64, Figure 7-54, Table 7-65, and Figure 7-55 present timing requirements and switching characteristics for SPI – Controller Mode.

Table 7-64. MCSPI Timing Requirements – Controller Mode

see Figure 7-54

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SM4	$t_{su(POCI-SPICLK)}$	Setup time, SPIn_D[x] valid before SPIn_CLK active edge	2.8		ns
SM5	$t_{h(SPICLK-POCI)}$	Hold time, SPIn_D[x] valid after SPIn_CLK active edge	3		ns

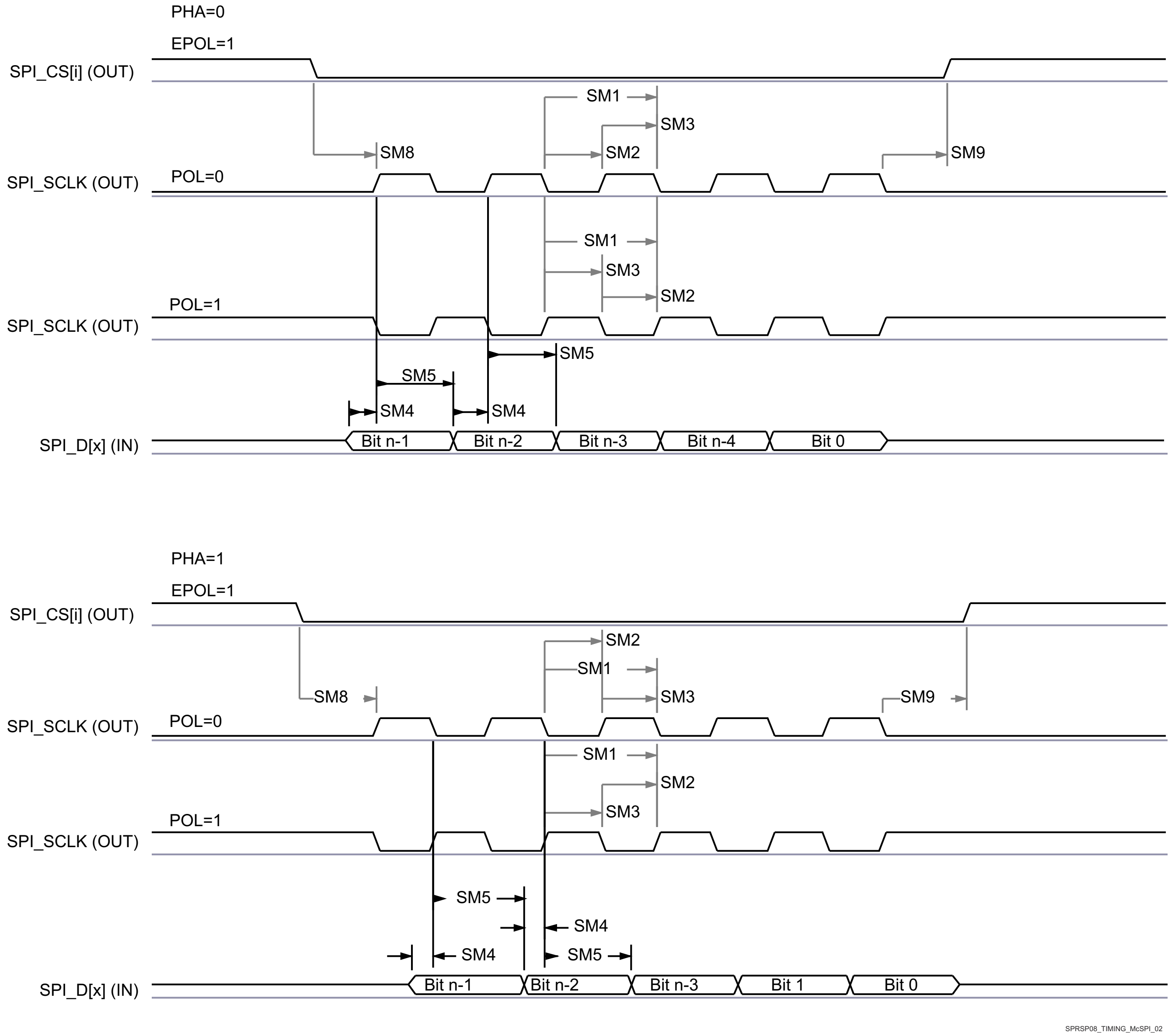


Figure 7-54. MCSPI Controller Mode Receive Timing

Table 7-65. MCSPI Switching Characteristics - Controller Mode

see Figure 7-55

NO.	PARAMETER			MIN	MAX	UNIT
SM1	$t_{c(SPICLK)}$	Cycle time, SPIn_CLK		20		ns
SM2	$t_{w(SPICLKL)}$	Pulse duration, SPIn_CLK low		0.5P - 1(1)		ns
SM3	$t_{w(SPICLKH)}$	Pulse duration, SPIn_CLK high		0.5P - 1(1)		ns
SM6	$t_{d(SPICLK-PICO)}$	Delay time, SPIn_CLK active edge to SPIn_D[x]		-3	2.5	ns
SM7	$t_{d(CS-PICO)}$	Delay time, SPIn_CSi active edge to SPIn_D[x]		5		ns
SM8	$t_{d(CS-SPICLK)}$	Delay time, SPIn_CSi active to SPIn_CLK first edge	PHA = 0	B - 4(2)		ns
			PHA = 1	A - 4(3)		ns
SM9	$t_{d(SPICLK-CS)}$	Delay time, SPIn_CLK last edge to SPIn_CSi inactive	PHA = 0	A - 4(4)		ns
			PHA = 1	B - 4(5)		ns

(1) P = SPI_CLK period in ns.

(2) T_ref is the period of the McSPI functional clock in ns. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.

- When Fratio = 1; B = (TCS(i) + 0.5) * T_ref.
- When Fratio ≥ 2 and even value; B = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; B = ((TCS(i) * Fratio) + ((Fratio + 1) / 2)) * T_ref.

(3) T_ref is the period of the McSPI functional clock. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.

- When Fratio = 1; A = (TCS(i) + 1) * T_ref.
- When Fratio ≥ 2 and even value; A = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; A = ((TCS(i) * Fratio) + ((Fratio - 1) / 2)) * T_ref.

(4) T_ref is the period of the McSPI functional clock. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.

- When Fratio = 1; A = (TCS(i) + 1) * T_ref.
- When Fratio ≥ 2 and even value; A = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; A = ((TCS(i) * Fratio) + ((Fratio + 1) / 2)) * T_ref.

(5) T_ref is the period of the McSPI functional clock. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.

- When Fratio = 1; B = (TCS(i) + 0.5) * T_ref.
- When Fratio ≥ 2 and even value; B = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; B = ((TCS(i) * Fratio) + ((Fratio - 1) / 2)) * T_ref.

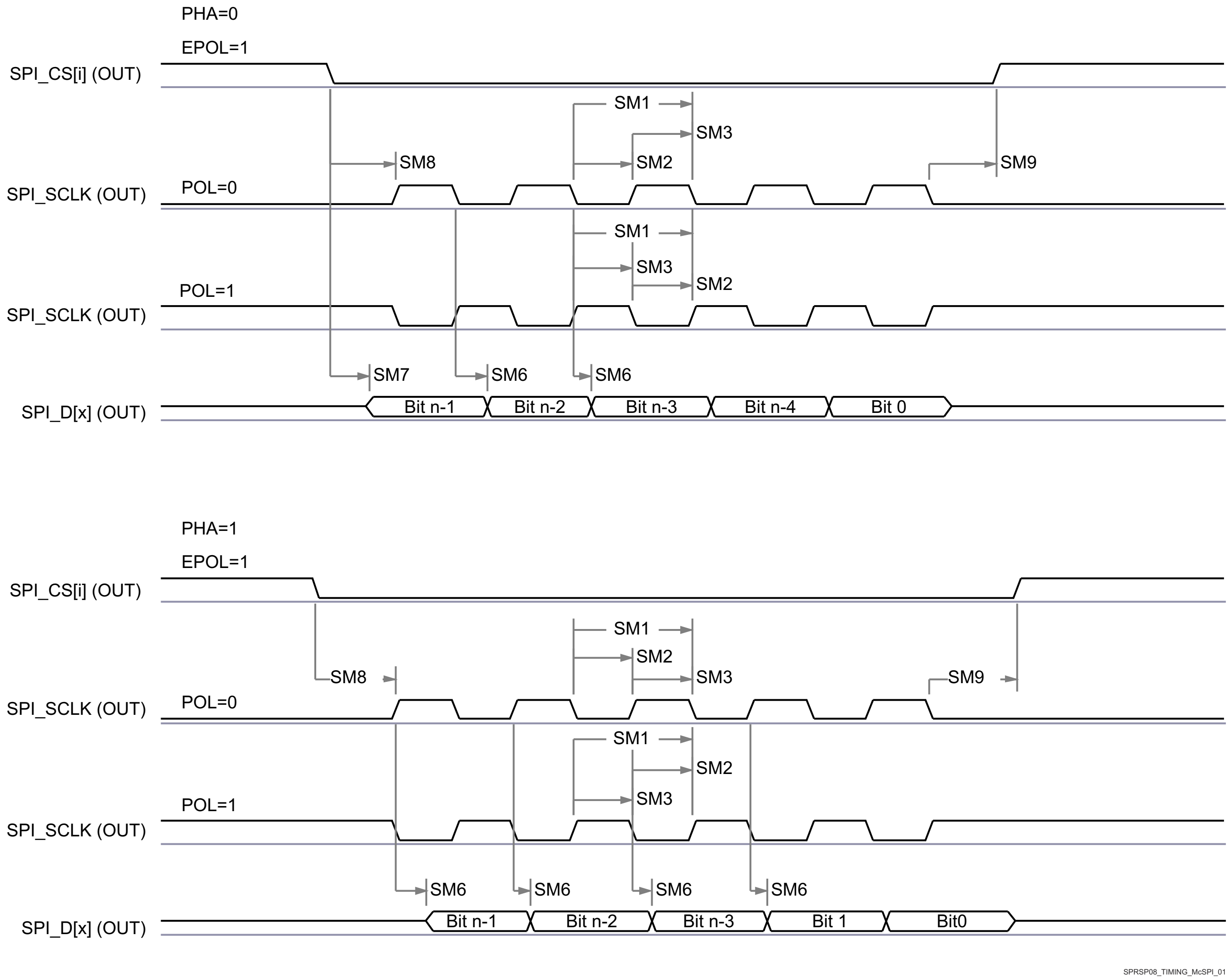


Figure 7-55. MCSPI Controller Mode Transmit Timing

7.10.5.11.2 MCSPI — Peripheral Mode

Table 7-66, Figure 7-56, Table 7-67, and Figure 7-57 present timing requirements and switching characteristics for SPI – Peripheral Mode.

Table 7-66. MCSPI Timing Requirements – Peripheral Mode

see Figure 7-56

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS1	$t_{c(SPICLK)}$	Cycle time, SPIn_CLK	20		ns
SS2	$t_{w(SPICLKL)}$	Pulse duration, SPIn_CLK low	0.45P(1)		ns
SS3	$t_{w(SPICLKH)}$	Pulse duration, SPIn_CLK high	0.45P(1)		ns
SS4	$t_{su(PICO-SPICLK)}$	Setup time, SPIn_D[x] valid before SPIn_CLK active edge	5		ns
SS5	$t_{h(SPICLK-PICO)}$	Hold time, SPIn_D[x] valid after SPIn_CLK active edge	5		ns
SS8	$t_{su(CS-SPICLK)}$	Setup time, SPIn_CSi valid before SPIn_CLK first edge	5		ns
SS9	$t_{h(SPICLK-CS)}$	Hold time, SPIn_CSi valid after SPIn_CLK last edge	5		ns

(1) P = SPIn_CLK period in ns.

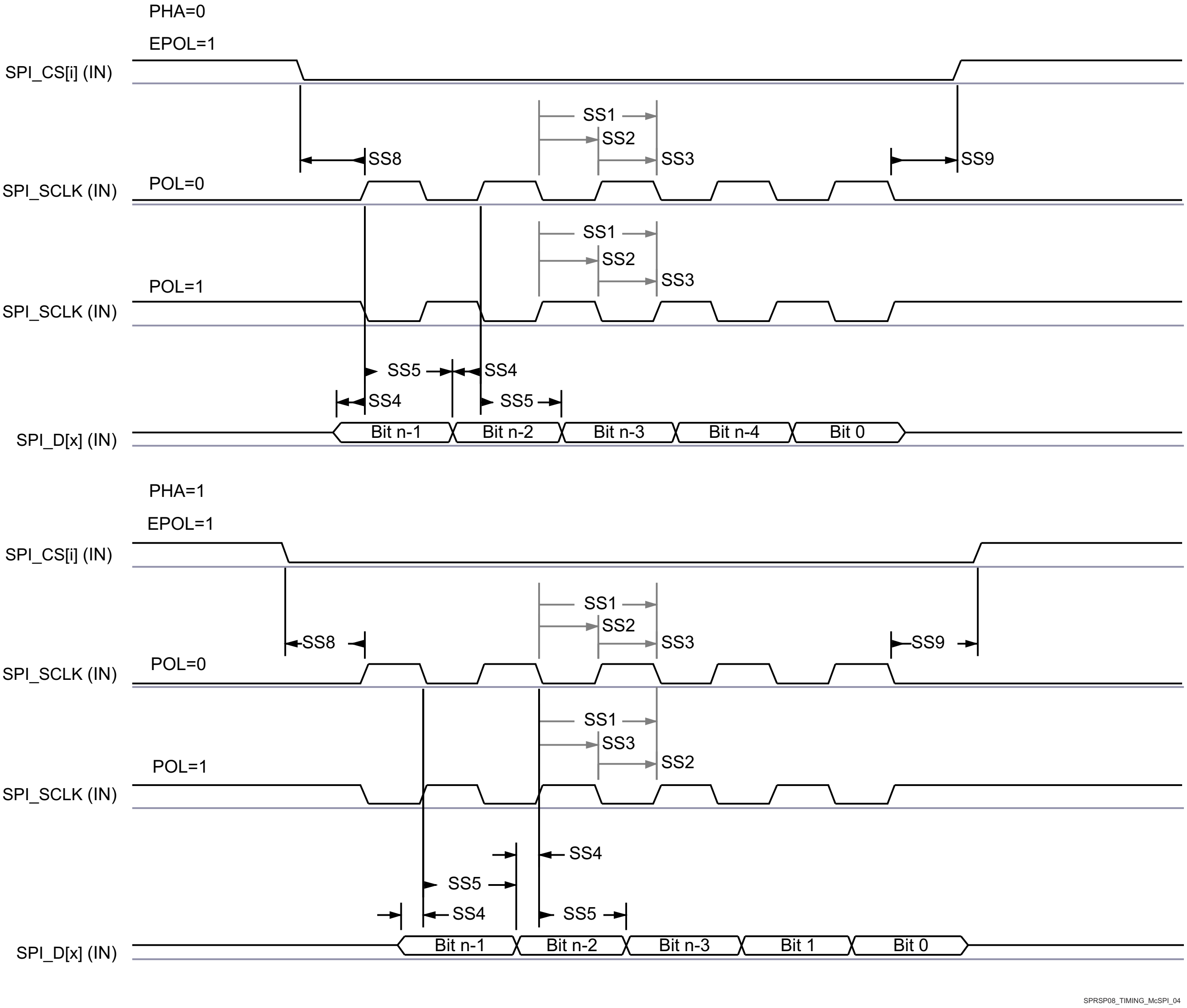


Figure 7-56. SPI Peripheral Mode Receive Timing

Table 7-67. MCSPI Switching Characteristics – Peripheral Mode

see Figure 7-57

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS6	$t_{d(SPICLK-POCI)}$	Delay time, SPIn_CLK active edge to SPIn_D[x]	2	17.12	ns
SS7	$t_{sk(CS-POCI)}$	Delay time, SPIn_CSi active edge to SPIn_D[x]	20.95		ns

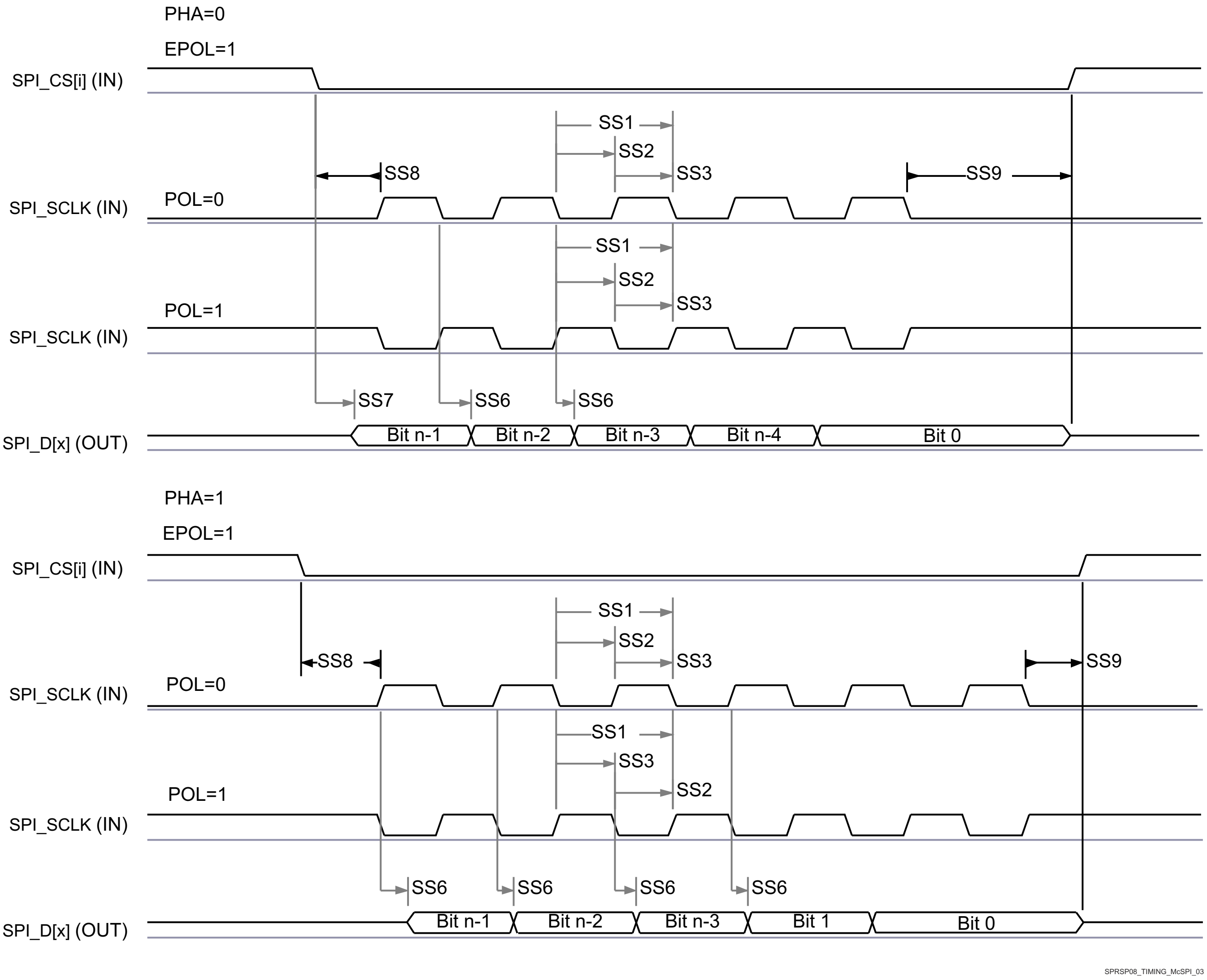


Figure 7-57. SPI Peripheral Mode Transmit Timing

7.10.5.12 MMCSD

The MMCSD Host Controller provides an interface to embedded Multi-Media Card (MMC), Secure Digital (SD), and Secure Digital IO (SDIO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about MMCSD interfaces, see the corresponding MMC0 and MMC1 subsections within *Signal Descriptions* and *Detailed Description* sections.

Note

Some operating modes require software configuration of the MMC DLL delay settings, as shown in Table 7-68 and Table 7-77.

The modes which show a value of "Tuning" in the ITAPDLYSEL column of Table 7-68 and Table 7-77 require a tuning algorithm to be used for optimizing input timing. Refer to the MMCSD Programming Guide in the device TRM for more information on the tuning algorithm and configuration of input delays required to optimize input timing.

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

7.10.5.12.1 MMC0 - eMMC Interface

MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and supports the following eMMC applications:

- Legacy speed
- High speed SDR
- High speed DDR
- HS200

Table 7-68 presents the required DLL software configuration settings for MMC0 timing modes.

Table 7-68. MMC0 DLL Delay Mapping for all Timing Modes

REGISTER NAME		MMCSD0_SS_PHY_CTRL_4_REG					MMCSD0_SS_PHY_CTRL_5_REG		
BIT FIELD		[31:24]	[20]	[15:12]	[8]	[4:0]	[17:16]	[10:8]	[2:0]
BIT FIELD NAME		STRBSEL	OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	SELDLYTXCLK SELDLYRXCLK	FRQSEL	CLKBUFSEL
MODE	DESCRIPTION	STROBE DELAY	OUTPUT DELAY ENABLE	OUTPUT DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DLL DELAY CHAIN SELECT	DLL REF FREQUENCY	DELAY BUFFER DURATION
Legacy SDR	8-bit PHY operating 1.8 V, 25 MHz	0x0	0x0	NA(1)	0x1	0x10	0x1	0x0	0x7
High Speed SDR	8-bit PHY operating 1.8 V, 50 MHz	0x0	0x0	NA(1)	0x1	0xA	0x1	0x0	0x7
High Speed DDR	8-bit PHY operating 1.8 V, 50 MHz	0x0	0x1	0x6	0x1	0x3	0x0	0x4	0x7
HS200	8-bit PHY operating 1.8 V, 200 MHz	0x0	0x1	0x7	0x1	Tuning(2)	0x0	0x0	0x7

(1) NA means Not Applicable
(2) Tuning means this mode requires a tuning algorithm to optimize input timing

Table 7-69 presents timing conditions for MMC0.

Table 7-69. MMC0 Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	Legacy SDR	0.14	1.44	V/ns
		High Speed SDR	0.3	0.9	V/ns
		High Speed DDR (CMD)	0.3	0.9	V/ns
		High Speed DDR (DAT[7:0])	0.45	0.9	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	Legacy SDR	1	12	pF
		High Speed SDR	1	12	pF
		High Speed DDR	1	12	pF
		HS200	1	6	pF
		PCB CONNECTIVITY REQUIREMENTS			
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	All modes	126	756	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	Legacy SDR, High Speed SDR		100	ps
		High Speed DDR, HS200		8	ps

7.10.5.12.1.1 Legacy SDR Mode

Table 7-70, Figure 7-58, Table 7-71, and Figure 7-59 present timing requirements and switching characteristics for MMC0 – Legacy SDR Mode.

Table 7-70. MMC0 Timing Requirements – Legacy SDR Mode

see Figure 7-58

NO.			MIN	MAX	UNIT
LSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	1.56		ns
LSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	5.44		ns
LSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	1.56		ns
LSDR4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	5.44		ns

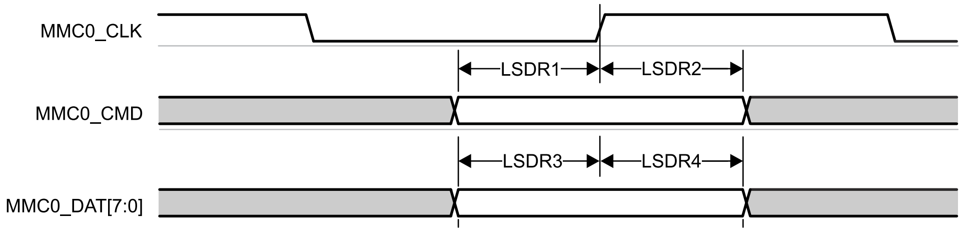


Figure 7-58. MMC0 – Legacy SDR – Receive Mode

Table 7-71. MMC0 Switching Characteristics – Legacy SDR Mode

see Figure 7-59

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		25	MHz
LSDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK	40		ns
LSDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	18.7		ns
LSDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	18.7		ns
LSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	-2.3	2.9	ns
LSDR9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition	-2.3	2.9	ns

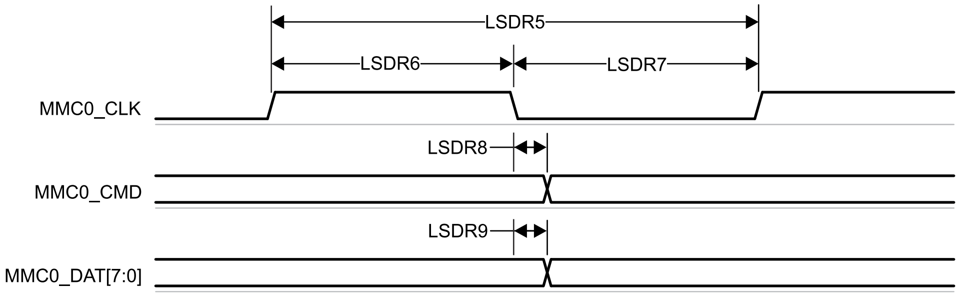


Figure 7-59. MMC0 – Legacy SDR – Transmit Mode

7.10.5.12.1.2 High Speed SDR Mode

Table 7-72, Figure 7-60, Table 7-73, and Figure 7-61 present timing requirements and switching characteristics for MMC0 – High Speed SDR Mode.

Table 7-72. MMC0 Timing Requirements – High Speed SDR Mode

see Figure 7-60

NO.			MIN	MAX	UNIT
HSSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	2.55		ns
HSSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	2.67		ns
HSSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	2.55		ns
HSSDR4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	2.67		ns

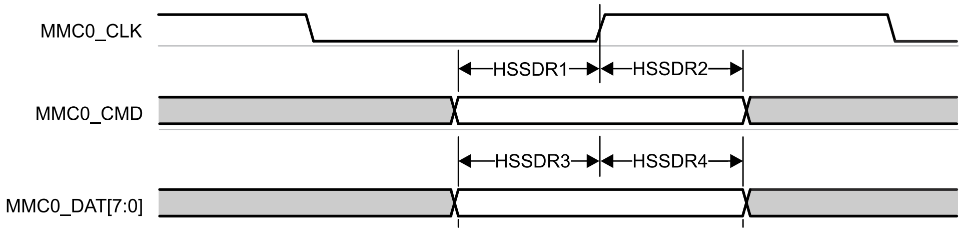


Figure 7-60. MMC0 – High Speed SDR Mode – Receive Mode

Table 7-73. MMC0 Switching Characteristics – High Speed SDR Mode

see Figure 7-61

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
HSSDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK	20		ns
HSSDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
HSSDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
HSSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	-2.3	2.9	ns
HSSDR9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition	-2.3	2.9	ns

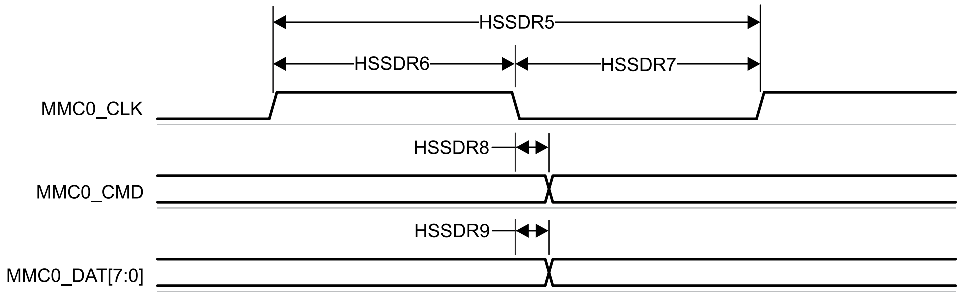


Figure 7-61. MMC0 – High Speed SDR Mode – Transmit Mode

7.10.5.12.1.3 High Speed DDR Mode

Table 7-74, Figure 7-62, Table 7-75, and Figure 7-63 present timing requirements and switching characteristics for MMC0 – High Speed DDR Mode.

Table 7-74. MMC0 Timing Requirements – High Speed DDR Mode

see Figure 7-62

NO.			MIN	MAX	UNIT
HSDDR1	$t_{su(cmdV-clk)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	1.62		ns
HSDDR2	$t_{h(clk-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	2.52		ns
HSDDR3	$t_{su(dV-clk)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK transition	0.83		ns
HSDDR4	$t_{h(clk-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK transition	1.76		ns

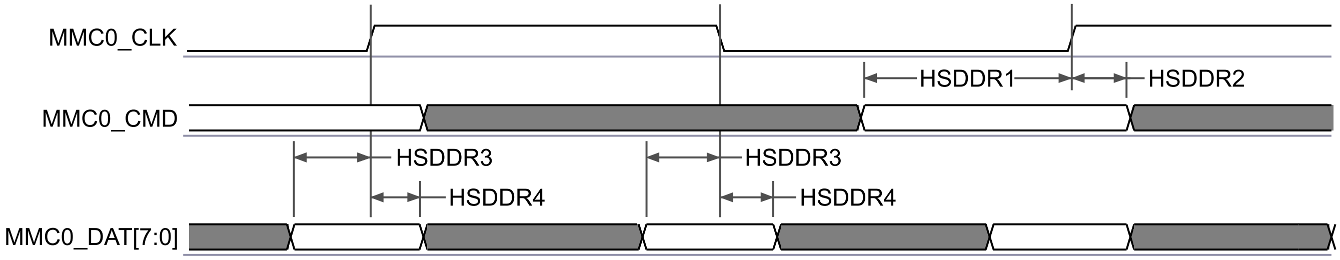


Figure 7-62. MMC0 – High Speed DDR Mode – Receive Mode

Table 7-75. MMC0 Switching Characteristics – High Speed DDR Mode

see Figure 7-63

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
HSDDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK	20		ns
HSDDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
HSDDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
HSDDR8	$t_{d(clk-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	3.31	7.65	ns
HSDDR9	$t_{d(clk-dV)}$	Delay time, MMC0_CLK transition to MMC0_DAT[7:0] transition	2.81	6.94	ns

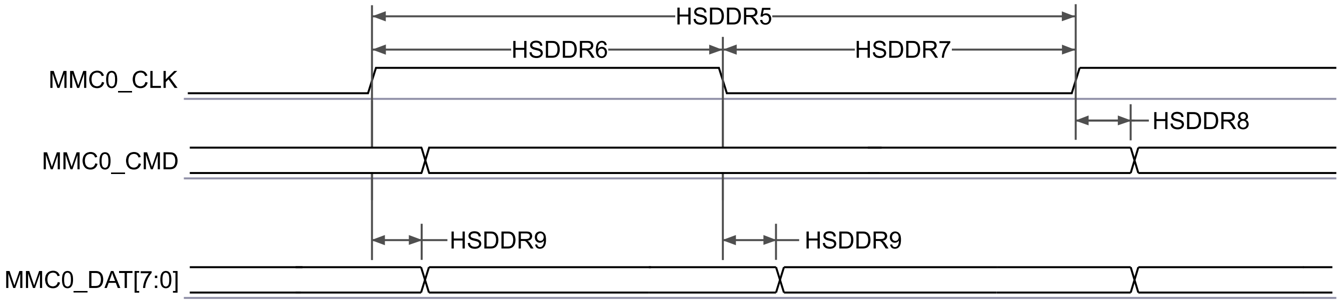


Figure 7-63. MMC0 – High Speed DDR Mode – Transmit Mode

7.10.5.12.1.4 HS200 Mode

Table 7-76 and Figure 7-64 present switching characteristics for MMC0 – HS200 Mode.

Table 7-76. MMC0 Switching Characteristics – HS200 Mode

see Figure 7-64

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		200	MHz
HS2005	$t_{c(clk)}$	Cycle time, MMC0_CLK	5		ns
HS2006	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	2.08		ns
HS2007	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	2.08		ns
HS2008	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	0.99	3.28	ns
HS2009	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[7:0] transition	0.99	3.28	ns

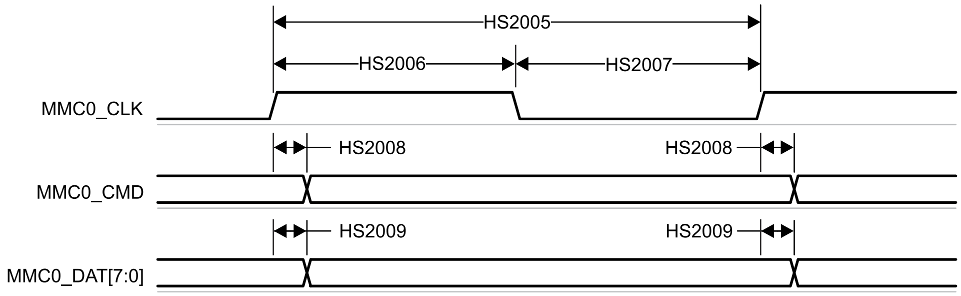


Figure 7-64. MMC0 – HS200 Mode – Transmit Mode

7.10.5.12.2 MMC1 - SD/SDIO Interface

MMC1 interface is compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and it supports the following SD Card applications:

- Default speed
- High speed
- UHS–I SDR12
- UHS–I SDR25
- UHS–I SDR50
- UHS–I SDR104
- UHS–I DDR50

Table 7-77 presents the required DLL software configuration settings for MMC1 timing modes.

Table 7-77. MMC1 DLL Delay Mapping for all Timing Modes

REGISTER NAME		MMCSD1_SS_PHY_CTRL_4_REG				MMCSD1_SS_PHY_CTRL_5_REG
BIT FIELD		[20]	[15:12]	[8]	[4:0]	[2:0]
BIT FIELD NAME		OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	CLKBUFSEL
MODE	DESCRIPTION	DELAY ENABLE	DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DELAY BUFFER DURATION
Default Speed	4-bit PHY operating 3.3 V, 25 MHz	0x1	0x0	0x1	0x0	0x7
High Speed	4-bit PHY operating 3.3 V, 50 MHz	0x1	0x0	0x1	0x0	0x7
UHS-I SDR12	4-bit PHY operating 1.8 V, 25 MHz	0x1	0xF	0x1	0x0	0x7
UHS-I SDR25	4-bit PHY operating 1.8 V, 50 MHz	0x1	0xF	0x1	0x0	0x7
UHS-I SDR50	4-bit PHY operating 1.8 V, 100 MHz	0x1	0xC	0x1	Tuning(1)	0x7
UHS-I DDR50	4-bit PHY operating 1.8 V, 50 MHz	0x1	0x9	0x1	Tuning(1)	0x7
UHS-I SDR104	4-bit PHY operating 1.8, V 200 MHz	0x1	0x6	0x1	Tuning(1)	0x7

(1) Tuning means this mode requires a tuning algorithm to be used for optimal input timing

Table 7-78 presents timing conditions for MMC1.

Table 7-78. MMC1 Timing Conditions

PARAMETER			MIN	MAX	UNIT
Input Conditions					
SR_I	Input slew rate	Default Speed, High Speed	0.69	2.06	V/ns
		UHS–I SDR12, UHS–I SDR25	0.34	1.34	V/ns
		UHS–I DDR50	1	2	V/ns
Output Conditions					
C_L	Output load capacitance	UHS–I DDR50	3	10	pF
		All other modes	1	10	pF
PCB Connectivity Requirements					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	UHS–I DDR50	240	1134	ps
		All other modes	126	1386	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	UHS–I DDR50, UHS–I SDR104		20	ps
		All other modes		100	ps

7.10.5.12.2.1 Default Speed Mode

Table 7-79, Figure 7-65, Table 7-80, and Figure 7-66 present timing requirements and switching characteristics for MMC1 – Default Speed Mode.

Table 7-79. Timing Requirements for MMC1 – Default Speed Mode

see Figure 7-65

NO.			MIN	MAX	UNIT
DS1	$t_{su(cmdV-clkH)}$	Setup time, MMC1_CMD valid before MMCi_CLK rising edge	2.15		ns
DS2	$t_{h(clkH-cmdV)}$	Hold time, MMC1_CMD valid after MMC1_CLK rising edge	1.67		ns
DS3	$t_{su(dV-clkH)}$	Setup time, MMC1_DAT[3:0] valid before MMC1_CLK rising edge	2.15		ns
DS4	$t_{h(clkH-dV)}$	Hold time, MMC1_DAT[3:0] valid after MMC1_CLK rising edge	1.67		ns

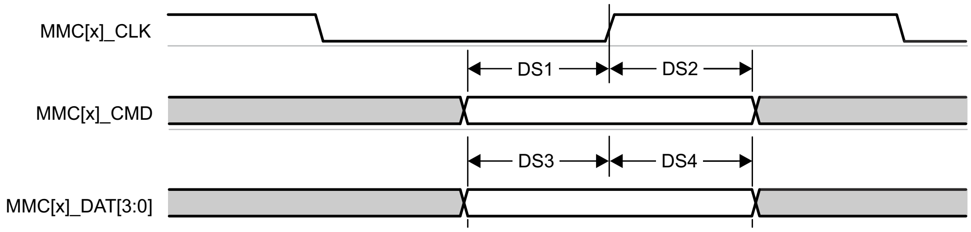


Figure 7-65. MMC1 – Default Speed – Receive Mode

Table 7-80. Switching Characteristics for MMC1 – Default Speed Mode

see Figure 7-66

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC1_CLK		25	MHz
DS5	$t_{c(clk)}$	Cycle time, MMC1_CLK	40		ns
DS6	$t_{w(clkH)}$	Pulse duration, MMC1_CLK high	18.7		ns
DS7	$t_{w(clkL)}$	Pulse duration, MMC1_CLK low	18.7		ns
DS8	$t_{d(clkL-cmdV)}$	Delay time, MMC1_CLK falling edge to MMC1_CMD transition	-1.8	1.8	ns
DS9	$t_{d(clkL-dV)}$	Delay time, MMC1_CLK falling edge to MMC1_DAT[3:0] transition	-1.8	1.8	ns

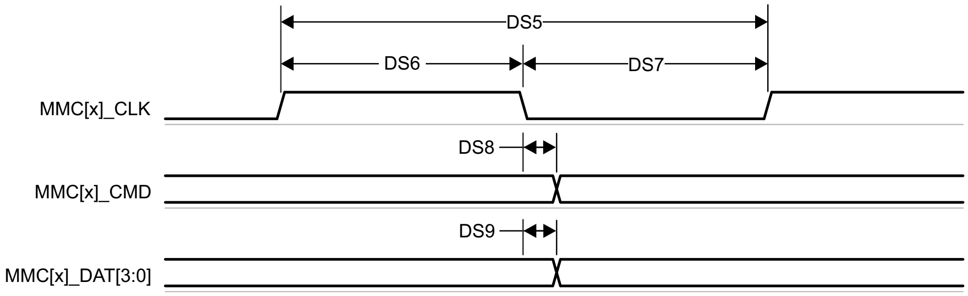


Figure 7-66. MMC1 – Default Speed – Transmit Mode

7.10.5.12.2.2 High Speed Mode

Table 7-81, Figure 7-67, Table 7-82, and Figure 7-68 present timing requirements and switching characteristics for MMC1 – High Speed Mode.

Table 7-81. Timing Requirements for MMC1 – High Speed Mode

see Figure 7-67

NO.			MIN	MAX	UNIT
HS1	$t_{su(cmdV-clkH)}$	Setup time, MMC1_CMD valid before MMC1_CLK rising edge	2.15		ns
HS2	$t_{h(clkH-cmdV)}$	Hold time, MMC1_CMD valid after MMC1_CLK rising edge	1.67		ns
HS3	$t_{su(dV-clkH)}$	Setup time, MMC1_DAT[3:0] valid before MMC1_CLK rising edge	2.15		ns
HS4	$t_{h(clkH-dV)}$	Hold time, MMC1_DAT[3:0] valid after MMC1_CLK rising edge	1.67		ns

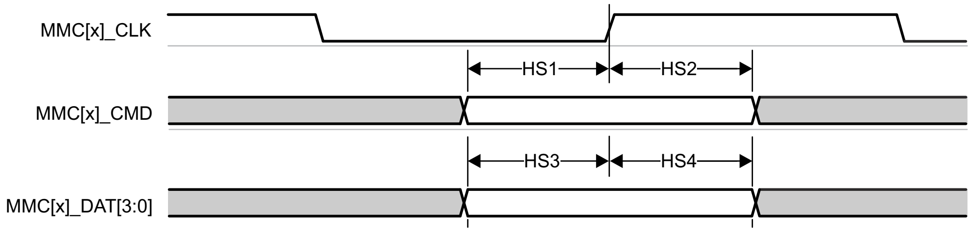


Figure 7-67. MMC1 – High Speed – Receive Mode

Table 7-82. Switching Characteristics for MMC1 – High Speed Mode

see Figure 7-68

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC1_CLK		50	MHz
HS5	$t_{c(clk)}$	Cycle time. MMC1_CLK	20		ns
HS6	$t_{w(clkH)}$	Pulse duration, MMC1_CLK high	9.2		ns
HS7	$t_{w(clkL)}$	Pulse duration, MMC1_CLK low	9.2		ns
HS8	$t_{d(clkL-cmdV)}$	Delay time, MMC1_CLK falling edge to MMC1_CMD transition	-1.8	1.8	ns
HS9	$t_{d(clkL-dV)}$	Delay time, MMC1_CLK falling edge to MMC1_DAT[3:0] transition	-1.8	1.8	ns

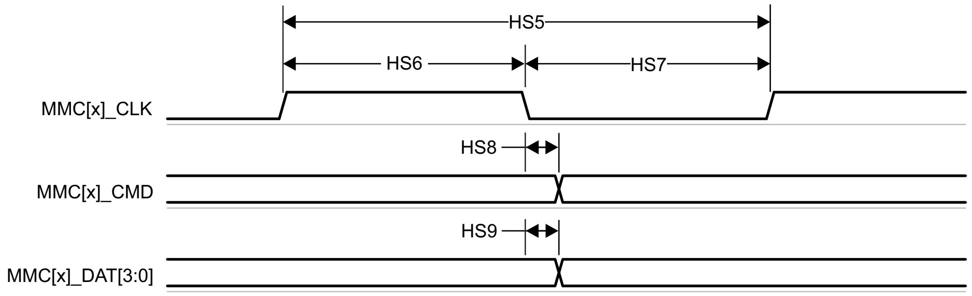


Figure 7-68. MMC1 – High Speed – Transmit Mode

7.10.5.12.2.3 UHS–I SDR12 Mode

Table 7-83, Figure 7-69, Table 7-84, and Figure 7-70 present timing requirements and switching characteristics for MMC1 – UHS-I SDR12 Mode.

Table 7-83. Timing Requirements for MMC1 – UHS-I SDR12 Mode

see Figure 7-69

NO.			MIN	MAX	UNIT
SDR121	$t_{su(cmdV-clkH)}$	Setup time, MMC1_CMD valid before MMC1_CLK rising edge	2.35		ns
SDR122	$t_{h(clkH-cmdV)}$	Hold time, MMC1_CMD valid after MMC1_CLK rising edge	1.67		ns
SDR123	$t_{su(dV-clkH)}$	Setup time, MMC1_DAT[3:0] valid before MMC1_CLK rising edge	2.35		ns
SDR124	$t_{h(clkH-dV)}$	Hold time, MMC1_DAT[3:0] valid after MMC1_CLK rising edge	1.67		ns

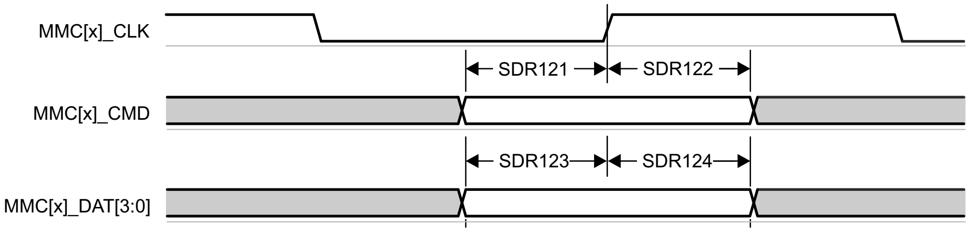


Figure 7-69. MMC1 – UHS-I SDR12 – Receive Mode

Table 7-84. Switching Characteristics for MMC1 – UHS-I SDR12 Mode

see Figure 7-70

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC1_CLK		25	MHz
SDR125	$t_{c(clk)}$	Cycle time, MMC1_CLK	40		ns
SDR126	$t_{w(clkH)}$	Pulse duration, MMC1_CLK high	18.7		ns
SDR127	$t_{w(clkL)}$	Pulse duration, MMC1_CLK low	18.7		ns
SDR128	$t_{d(clkL-cmdV)}$	Delay time, MMC1_CLK rising edge to MMC1_CMD transition	1.2	8	ns
SDR129	$t_{d(clkL-dV)}$	Delay time, MMC1_CLK rising edge to MMC1_DAT[3:0] transition	1.2	8	ns

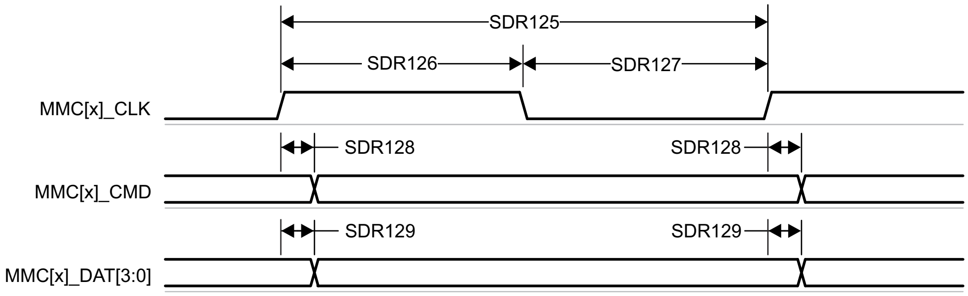


Figure 7-70. MMC1 – UHS-I SDR12 – Transmit Mode

7.10.5.12.2.4 UHS–I SDR25 Mode

Table 7-85, Figure 7-71, Table 7-86, and Figure 7-72 present timing requirements and switching characteristics for MMC1 – UHS-I SDR25 Mode.

Table 7-85. Timing Requirements for MMC1 – UHS-I SDR25 Mode

see Figure 7-71

NO.			MIN	MAX	UNIT
SDR251	$t_{su(cmdV-clkH)}$	Setup time, MMC1_CMD valid before MMC1_CLK rising edge	1.95		ns
SDR252	$t_{h(clkH-cmdV)}$	Hold time, MMC1_CMD valid after MMC1_CLK rising edge	1.67		ns
SDR253	$t_{su(dV-clkH)}$	Setup time, MMC1_DAT[3:0] valid before MMC1_CLK rising edge	1.95		ns
SDR254	$t_{h(clkH-dV)}$	Hold time, MMC1_DAT[3:0] valid after MMC1_CLK rising edge	1.67		ns

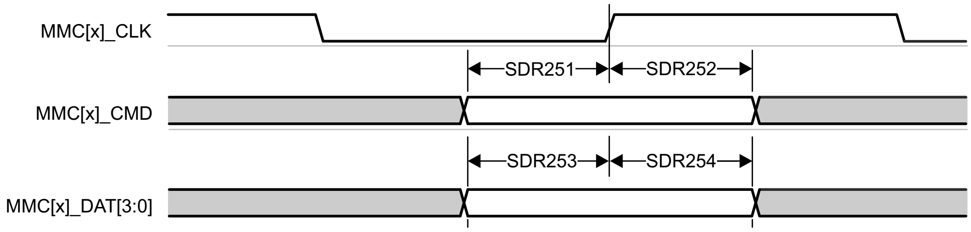


Figure 7-71. MMC1 – UHS-I SDR25 – Receive Mode

Table 7-86. Switching Characteristics for MMC1 – UHS-I SDR25 Mode

see Figure 7-72

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC1_CLK		50	MHz
SDR255	$t_{c(clk)}$	Cycle time, MMC1_CLK	20		ns
SDR256	$t_{w(clkH)}$	Pulse duration, MMC1_CLK high	9.2		ns
SDR257	$t_{w(clkL)}$	Pulse duration, MMC1_CLK low	9.2		ns
SDR258	$t_{d(clkL-cmdV)}$	Delay time, MMC1_CLK rising edge to MMC1_CMD transition	2.4	8	ns
SDR259	$t_{d(clkL-dV)}$	Delay time, MMC1_CLK rising edge to MMC1_DAT[3:0] transition	2.4	8	ns

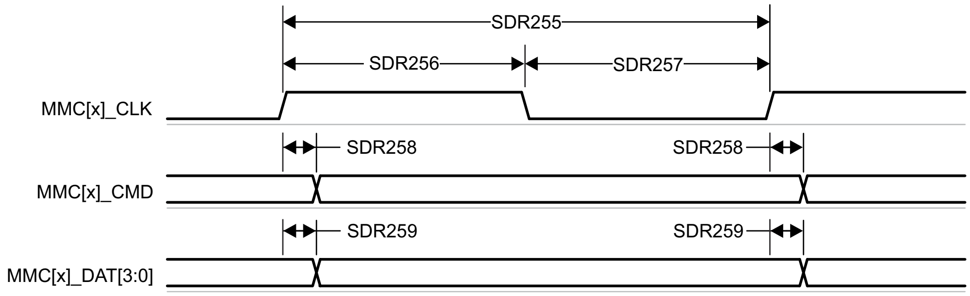


Figure 7-72. MMC1 – UHS-I SDR25 – Transmit Mode

7.10.5.12.2.5 UHS–I SDR50 Mode

Table 7-87, and Figure 7-73 presents switching characteristics for MMC1 – UHS-I SDR50 Mode.

Table 7-87. Switching Characteristics for MMC1 – UHS-I SDR50 Mode

see Figure 7-73

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC1_CLK		100	MHz
SDR505	$t_{c(clk)}$	Cycle time, MMC1_CLK	10		ns
SDR506	$t_{w(clkH)}$	Pulse duration, MMC1_CLK high	4.45		ns
SDR507	$t_{w(clkL)}$	Pulse duration, MMC1_CLK low	4.45		ns
SDR508	$t_{d(clkL-cmdV)}$	Delay time, MMC1_CLK rising edge to MMC1_CMD transition	1.2	6.35	ns
SDR509	$t_{d(clkL-dV)}$	Delay time, MMC1_CLK rising edge to MMC1_DAT[3:0] transition	1.2	6.35	ns

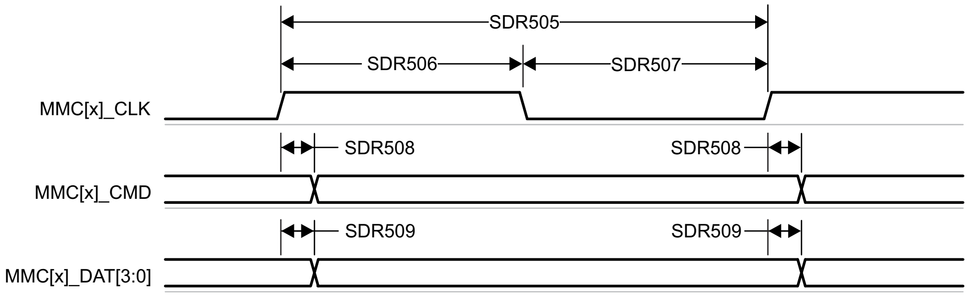


Figure 7-73. MMC1 – UHS-I SDR50 – Transmit Mode

7.10.5.12.2.6 UHS–I DDR50 Mode

Table 7-88, and Figure 7-74 present switching characteristics for MMC1 – UHS-I DDR50 Mode.

Table 7-88. Switching Characteristics for MMC1 – UHS-I DDR50 Mode

see Figure 7-74

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC1_CLK		50	MHz
DDR505	$t_{c(clk)}$	Cycle time, MMC1_CLK	20		ns
DDR506	$t_{w(clkH)}$	Pulse duration, MMC1_CLK high	9.2		ns
DDR507	$t_{w(clkL)}$	Pulse duration, MMC1_CLK low	9.2		ns
DDR508	$t_{d(clk-cmdV)}$	Delay time, MMC1_CLK rising edge to MMC1_CMD transition	1.2	6.35	ns
DDR509	$t_{d(clk-dV)}$	Delay time, MMC1_CLK transition to MMC1_DAT[3:0] transition	1.2	6.35	ns

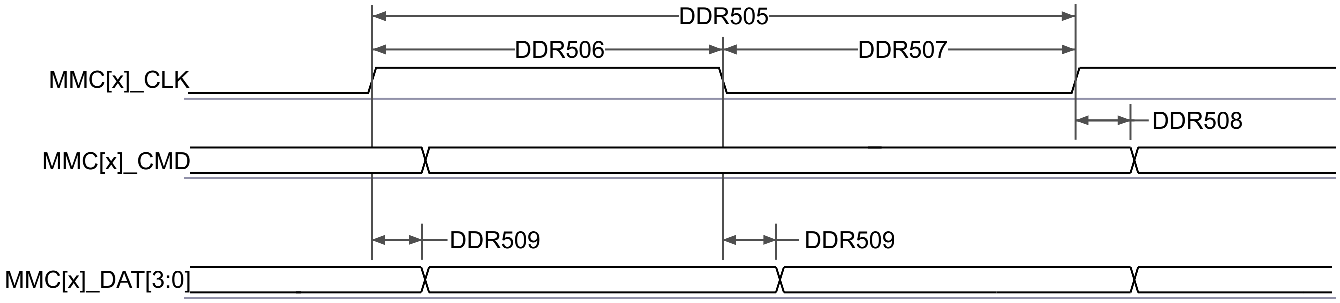


Figure 7-74. MMC1 – UHS-I DDR50 – Transmit Mode

7.10.5.12.2.7 UHS–I SDR104 Mode

Table 7-89, and Figure 7-75 present switching characteristics for MMC1 – UHS-I SDR104 Mode.

Table 7-89. Switching Characteristics for MMC1 – UHS-I SDR104 Mode

see Figure 7-75

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC1_CLK		200	MHz
SDR1045	$t_{c(clk)}$	Cycle time, MMC1_CLK	5		ns
SDR1046	$t_{w(clkH)}$	Pulse duration, MMC1_CLK high	2.12		ns
SDR1047	$t_{w(clkL)}$	Pulse duration, MMC1_CLK low	2.12		ns
SDR1048	$t_{d(clkL-cmdV)}$	Delay time, MMC1_CLK rising edge to MMC1_CMD transition	1.08	3.2	ns
SDR1049	$t_{d(clkL-dV)}$	Delay time, MMC1_CLK rising edge to MMC1_DAT[3:0] transition	1.08	3.2	ns

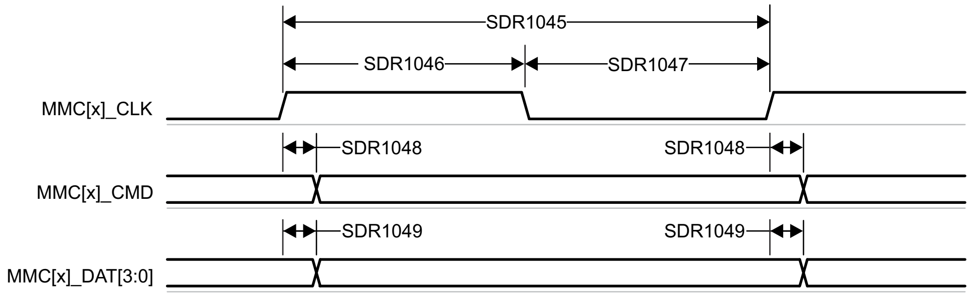


Figure 7-75. MMC1 – UHS-I SDR104 – Transmit Mode

7.10.5.13 CPTS

Table 7-90, Table 7-91, Figure 7-76, Table 7-92, and Figure 7-77 present timing conditions, requirements, and switching characteristics for CPTS.

Table 7-90. CPTS Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	10	pF

Table 7-91. CPTS Timing Requirements

see Figure 7-76

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T1	$t_{w(HWTSPUSHH)}$	Pulse duration, HWnTSPUSH high	12P(1) + 2		ns
T2	$t_{w(HWTSPUSHL)}$	Pulse duration, HWnTSPUSH low	12P(1) + 2		ns
T3	$t_{c(RFT\_CLK)}$	Cycle time, RFT_CLK	5	8	ns
T4	$t_{w(RFT\_CLKH)}$	Pulse duration, RFT_CLK high	0.45T(2)		ns
T5	$t_{w(RFT\_CLKL)}$	Pulse duration, RFT_CLK low	0.45T(2)		ns

(1) P = functional clock period in ns.
(2) T = RFT_CLK period in ns.

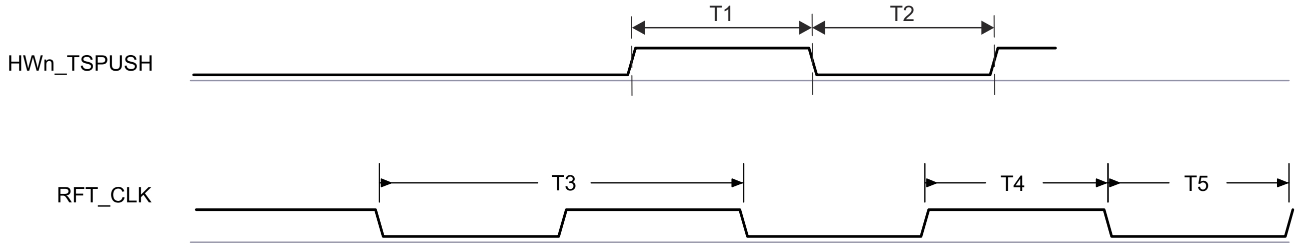


Figure 7-76. CPTS Timing Requirements

Table 7-92. CPTS Switching Characteristics

see Figure 7-77

NO.	PARAMETER	DESCRIPTION	SOURCE	MIN	MAX	UNIT
T6	$t_{w(TS\_COMPH)}$	Pulse duration, TS_COMP high		36P[1] - 2		ns
T7	$t_{w(TS\_COMPL)}$	Pulse duration, TS_COMP low		36P[1] - 2		ns
T8	$t_{w(TS\_SYNCH)}$	Pulse duration, TS_SYNC high		36P[1] - 2		ns
T9	$t_{w(TS\_SYNCL)}$	Pulse duration, TS_SYNC low		36P[1] - 2		ns
T10	$t_{w(SYNC\_OUTH)}$	Pulse duration, SYNCn_OUT high	TS_SYNC	36P[1] - 2		ns
			GENF	5P[1] - 2		ns
T11	$t_{w(SYNC\_OUTL)}$	Pulse duration, SYNCn_OUT low	TS_SYNC	36P[1] - 2		ns
			GENF	5P[1] - 2		ns

(1) P = functional clock period in ns.

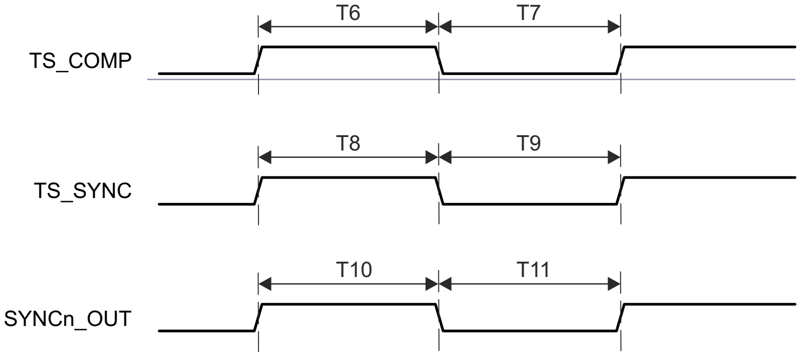


Figure 7-77. CPTS Switching Characteristics

For more information, see *Data Movement Architecture (DMA)* chapter in the device TRM.

7.10.5.14 OSPI

OSPI0 offers two data capture modes, PHY mode and Tap mode.

PHY mode uses an internal reference clock to transmit and receive data via a DLL based PHY, where each reference clock cycle produces a single cycle of OSPI0_CLK for Single Data Rate (SDR) transfers or a half cycle of OSPI0_CLK for Double Data Rate (DDR) transfers. PHY mode supports four clocking topologies for the receive data capture clock. Internal PHY Loopback - uses the internal reference clock as the PHY receive data capture clock. Internal Pad Loopback - uses OSPI0_LBCLKO looped back into the PHY from the OSPI0_LBCLKO pin as the PHY receive data capture clock. External Board Loopback - uses OSPI0_LBCLKO looped back into the PHY from the OSPI0_DQS pin as the PHY receive data capture clock. DQS - uses the DQS output from the attached device as the PHY receive data capture clock. SDR transfers are not supported when using the Internal Pad Loopback and DQS clocking topologies. DDR transfers are not supported when using the Internal PHY Loopback or Internal Pad Loopback clocking topologies.

Tap mode uses an internal reference clock with selectable taps to adjusted data transmit and receive capture delays relative to OSPI0_CLK, which is a divide by 4 of the internal reference clock for SDR transfers or a divide by 8 of the internal reference clock for DDR transfers. Tap mode only supports one clocking topology for the receive data capture clock. No Loopback - uses the internal reference clock as the Tap receive data capture clock. This clocking topology supports a maximum internal reference clock rate of 200 MHz, which produces an OSPI0_CLK rate up to 50 MHz for SDR mode or 25 MHz for DDR mode.

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Section 7.10.5.14.1 defines timing requirements and switching characteristics associated with PHY mode and Section 7.10.5.14.2 defines timing requirements and switching characteristics associated with Tap mode.

Table 7-93 presents timing conditions for OSPI0.

Table 7-93. OSPI0 Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		1	6	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	10	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of OSPI0_CLK trace	No Loopback Internal PHY Loopback Internal Pad Loopback		450	ps
	Propagation delay of OSPI0_LBCLKO trace	External Board Loopback	2L(1) - 30	2L(1) + 30	ps
	Propagation delay of OSPI0_DQS trace	DQS	L(1) - 30	L(1) + 30	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch of OSPI0_D[7:0] and OSPI0_CSn[3:0] relative to OSPI0_CLK	All modes		60	ps

(1) L = Propagation delay of OSPI0_CLK trace

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

7.10.5.14.1 OSPI0 PHY Mode

7.10.5.14.1.1 OSPI0 With PHY Data Training

Read and write data valid windows will shift due to variation in process, voltage, temperature, and operating frequency. A data training method may be implemented to dynamically configure optimal read and write timing. Implementing data training enables proper operation across temperature with a specific process, voltage, and frequency operating condition, while achieving a higher operating frequency.

Data transmit and receive timing parameters are not defined for the data training use case since they are dynamically adjusted based on the operating condition.

Table 7-94 defines DLL delays required for OSPI0 with Data Training. Table 7-95, Figure 7-78, Table 7-96, and Figure 7-79 present timing requirements and switching characteristics for OSPI0 with Data Training.

Table 7-94. OSPI0 DLL Delay Mapping for PHY Data Training

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD,	(1)
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	(2)

(1) Transmit DLL delay value determined by training software
(2) Receive DLL delay value determined by training software

Table 7-95. OSPI0 Timing Requirements – PHY Data Training

see Figure 7-78

NO.			MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	DDR with DQS	(1)		ns
O16	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	DDR with DQS	(1)		ns

(1) Minimum setup and hold time requirements for OSPI0_D[7:0] inputs are not defined when Data Training is used to find the optimum data valid window.

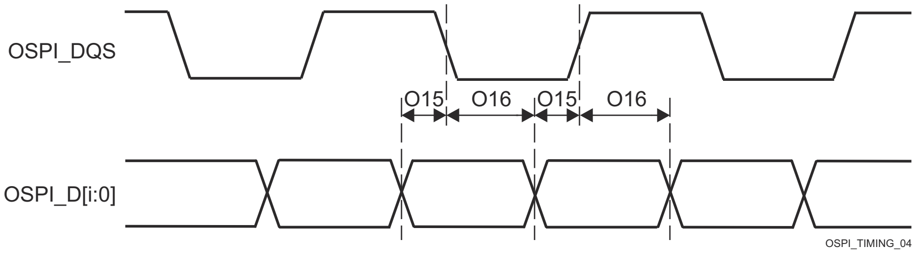


Figure 7-78. OSPI0 Timing Requirements – PHY Data Training, DDR with DQS

Table 7-96. OSPI Switching Characteristics – PHY Data Training

See Figure 7-79

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK	1.8V, DDR	6.02	7.52	ns
			3.3V, DDR	7.52	7.52	ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low	DDR	((0.475P[1]) - 0.3)		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high	DDR	((0.475P[1]) - 0.3)		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge	DDR	((0.475P[1]) + (0.975M[2]R[4]) + (0.04TD[5]) - 1)	((0.525P[1]) + (1.025M[2]R[4]) + (0.11TD[5]) + 1)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge	DDR	((0.475P[1]) + (0.975N[3]R[4]) - (0.04TD[5]) - 1)	((0.525P[1]) + (1.025N[3]R[4]) - (0.11TD[5]) + 1)	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	DDR	[6]	[6]	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns
(5) TD = PHY_CONFIG_TX_DLL_DELAY_FLD
(6) Minimum and maximum delay times for OSPI0_D[7:0] outputs are not defined when Data Training is used to find the optimum data valid window.

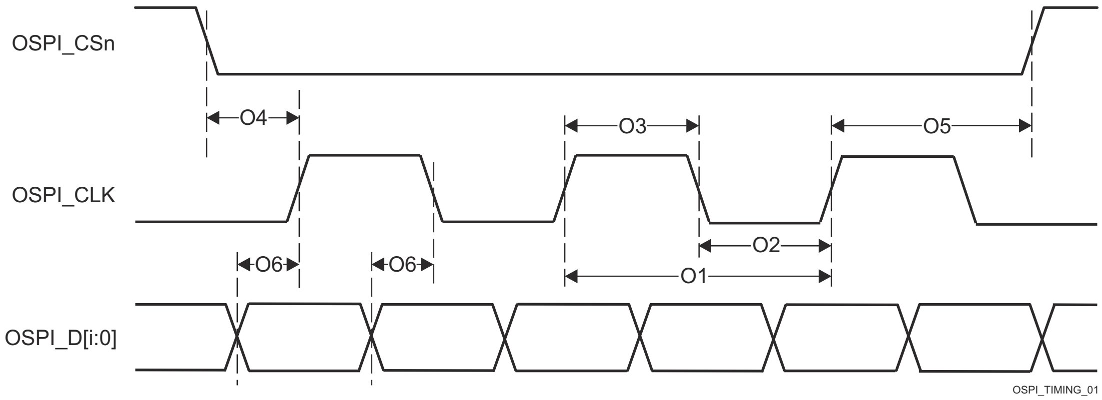


Figure 7-79. OSPI0 Switching Characteristics – PHY DDR Data Training

7.10.5.14.1.2 OSPI0 Without Data Training

Note

Timing parameters defined in this section are only applicable when data training is not implemented and DLL delays are configured as described in Table 7-97 and Table 7-100.

7.10.5.14.1.2.1 OSPI0 PHY SDR Timing

Table 7-97 defines DLL delays required for OSPI0 PHY SDR Mode. Table 7-98, Figure 7-80, Figure 7-81, Table 7-99, and Figure 7-82 present timing requirements and switching characteristics for OSPI0 PHY SDR Mode.

Table 7-97. OSPI0 DLL Delay Mapping for PHY SDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD,	0x0
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

Table 7-98. OSPI0 Timing Requirements – PHY SDR Mode

see Figure 7-80 and Figure 7-81

NO.			MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	1.8V, SDR with Internal PHY Loopback	4.8		ns
			3.3V, SDR with Internal PHY Loopback	5.19		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	1.8V, SDR with Internal PHY Loopback	-0.5		ns
			3.3V, SDR with Internal PHY Loopback	-0.5		ns
O21	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	1.8V, SDR with External Board Loopback	0.6		ns
			3.3V, SDR with External Board Loopback	0.9		ns
O22	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	1.8V, SDR with External Board Loopback	1.7		ns
			3.3V, SDR with External Board Loopback	2.0		ns

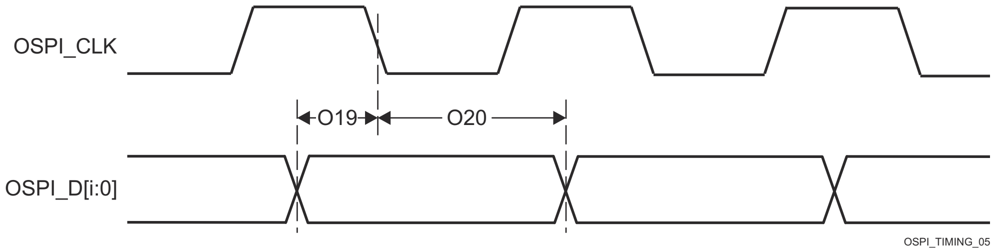


Figure 7-80. OSPI0 Timing Requirements – PHY SDR with Internal PHY Loopback

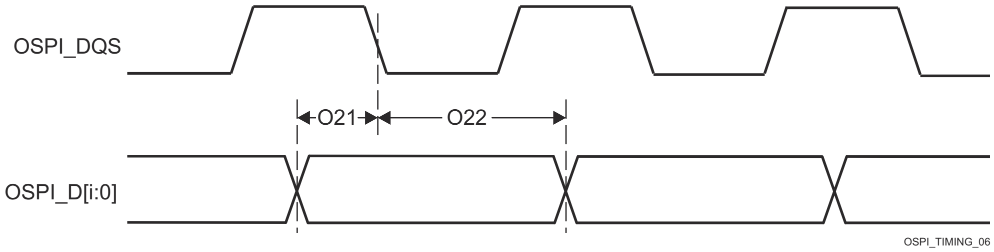


Figure 7-81. OSPI0 Timing Requirements – PHY SDR with External Board Loopback

Table 7-99. OSPI0 Switching Characteristics – PHY SDR Mode

see Figure 7-82

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0_CLK	1.8V	7		ns
			3.3V	6.03		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) + (0.975M(2)R(4)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + 1)	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) + 1)	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	1.8V	-1.16	1.25	ns
			3.3V	-1.33	1.51	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

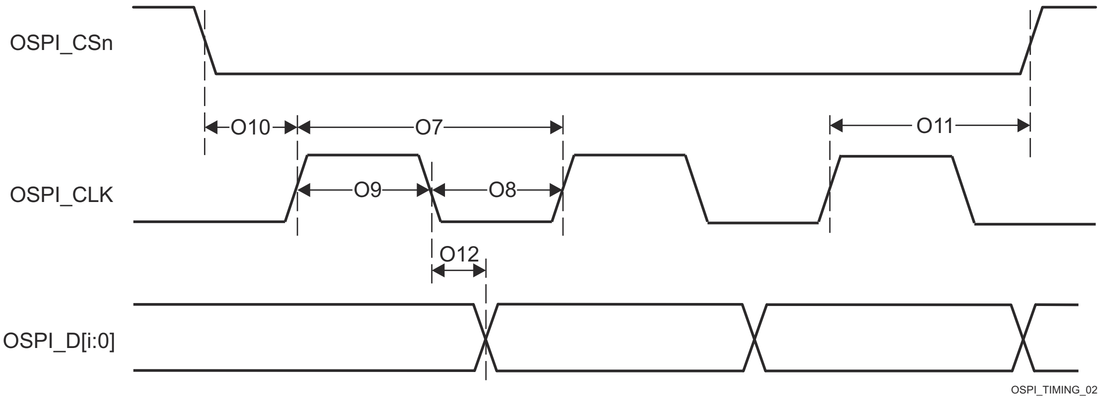


Figure 7-82. OSPI0 Switching Characteristics – PHY SDR

7.10.5.14.1.2.2 OSPI0 PHY DDR Timing

Table 7-100 defines DLL delays required for OSPI0 PHY DDR Mode. Table 7-101, Figure 7-83, Table 7-102, and Figure 7-84 present timing requirements and switching characteristics for OSPI0 PHY DDR Mode.

Table 7-100. OSPI0 DLL Delay Mapping for PHY DDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
1.8V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x3E
3.3V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x3B
Receive		
1.8V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x15
3.3V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x3A
All other modes	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

Table 7-101. OSPI0 Timing Requirements – PHY DDR Mode

see Figure 7-83

NO.			MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	1.8V, DDR with External Board Loopback	0.53		ns
			1.8V, DDR with DQS	-0.46		ns
			3.3V, DDR with External Board Loopback	1.23		ns
			3.3V, DDR with DQS	-0.66		ns
O16	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	1.8V, DDR with External Board Loopback	1.24(1)		ns
			1.8V, DDR with DQS	3.59		ns
			3.3V, DDR with External Board Loopback	1.44(1)		ns
			3.3V, DDR with DQS	7.92		ns

(1) This Hold time requirement is larger than the Hold time provided by a typical OSPI/QSPI/SPI device. Therefore, the trace length between the SoC and attached OSPI/QSPI/SPI device must be sufficiently long enough to ensure that the Hold time is met at the SoC. The length of the SoC's external loopback clock (OSPI0_LBCLKO to OSPI0_DQS) may need to be shortened to compensate.

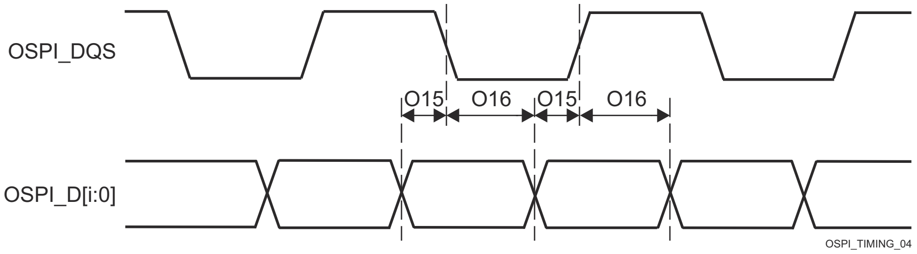


Figure 7-83. OSPI0 Timing Requirements – PHY DDR with External Board Loopback or DQS

Table 7-102. OSPI0 Switching Characteristics – PHY DDR Mode

see Figure 7-84

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		19		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O4	$t_{d(CSn\text{-}CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) - (0.975M(2)R(4)))	((0.525P(1)) - (1.025M(2)R(4)) + 7)	ns
O5	$t_{d(CLK\text{-}CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 7)	((0.525P(1)) + (1.025N(3)R(4)))	ns
O6	$t_{d(CLK\text{-}D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	1.8V	-7.71	-1.56	ns
			3.3V	-7.71	-1.56	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

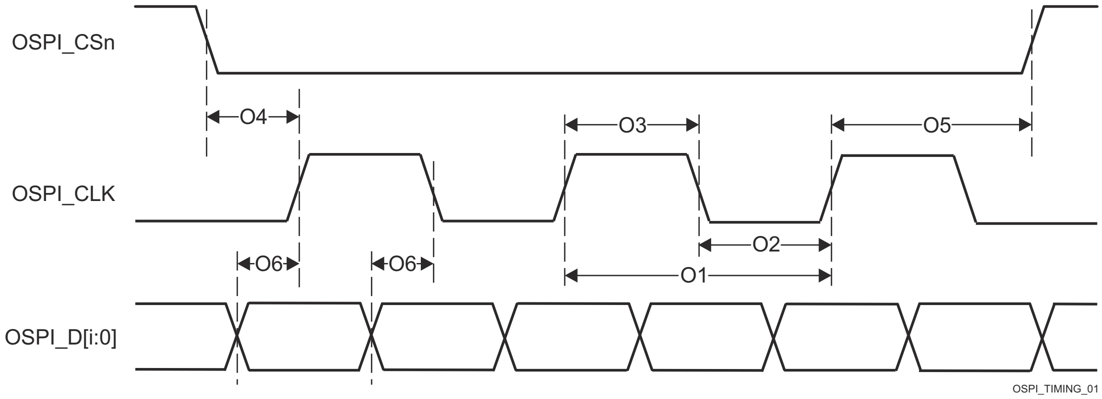


Figure 7-84. OSPI0 Switching Characteristics – PHY DDR

7.10.5.14.2 OSPI0 Tap Mode

7.10.5.14.2.1 OSPI0 Tap SDR Timing

Table 7-103, Figure 7-85, Table 7-104, and Figure 7-86 present timing requirements and switching characteristics for OSPI0 Tap SDR Mode.

Table 7-103. OSPI0 Timing Requirements – Tap SDR Mode

see Figure 7-85

NO.			MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	No Loopback	(15.4 - (0.975T(1)R(2)))		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	No Loopback	(- 4.3 + (0.975T(1)R(2)))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = reference clock cycle time in ns

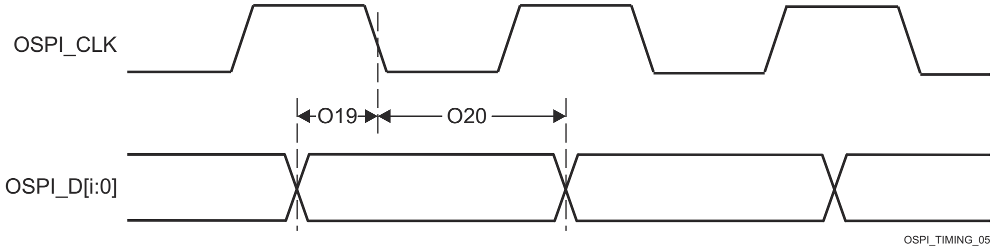


Figure 7-85. OSPI0 Timing Requirements – Tap SDR, No Loopback

Table 7-104. OSPI0 Switching Characteristics – Tap SDR Mode

see Figure 7-86

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		20		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O10	$t_{d(CSn\text{-}CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) + (0.975M(2)R(4)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + 1)	ns
O11	$t_{d(CLK\text{-}CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) + 1)	ns
O12	$t_{d(CLK\text{-}D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition		- 4.25	7.25	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

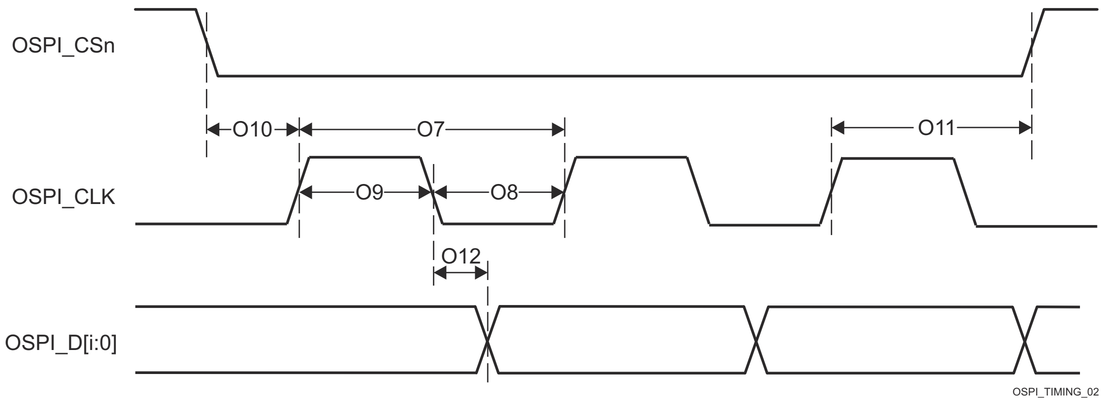


Figure 7-86. OSPI0 Switching Characteristics – Tap SDR, No Loopback

7.10.5.14.2.2 OSPI0 Tap DDR Timing

Table 7-105, Figure 7-87, Table 7-106, and Figure 7-88 present timing requirements and switching characteristics for OSPI0 Tap DDR Mode.

Table 7-105. OSPI0 Timing Requirements – Tap DDR Mode

see Figure 7-87

NO.			MODE	MIN	MAX	UNIT
O13	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	No Loopback	(17.04 - (0.975T[1]R[2]))		ns
O14	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	No Loopback	(- 3.16 + (0.975T[1]R[2]))		ns

[1] T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
[2] R = reference clock cycle time in ns

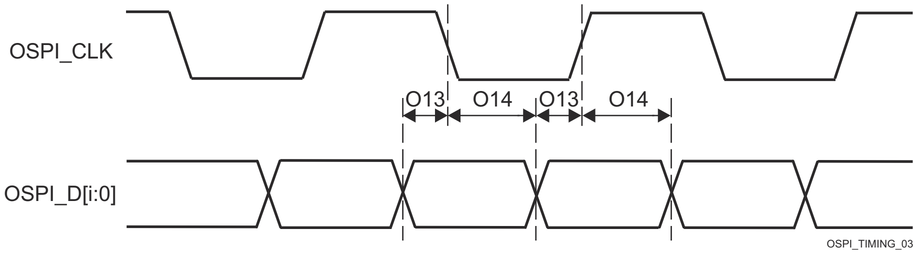


Figure 7-87. OSPI0 Timing Requirements – Tap DDR, No Loopback

Table 7-106. OSPI0 Switching Characteristics – Tap DDR Mode

see Figure 7-88

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		40		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) + ((0.975M(2)R(5)) - 1)	((0.525P(1)) + (1.025M(2)R(5)) + 1)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(5)) - 1)	((0.525P(1)) + (1.025N(3)R(5)) + 1)	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition		(- 5.04 + (0.975(T(4) + 1)R(5)) - (0.525P(1)))	(3.64 + (1.025(T(4) + 1)R(5)) - (0.475P(1)))	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) T = OSPI_RD_DATA_CAPTURE_REG[DDR_READ_DELAY_FLD]
(5) R = reference clock cycle time in ns

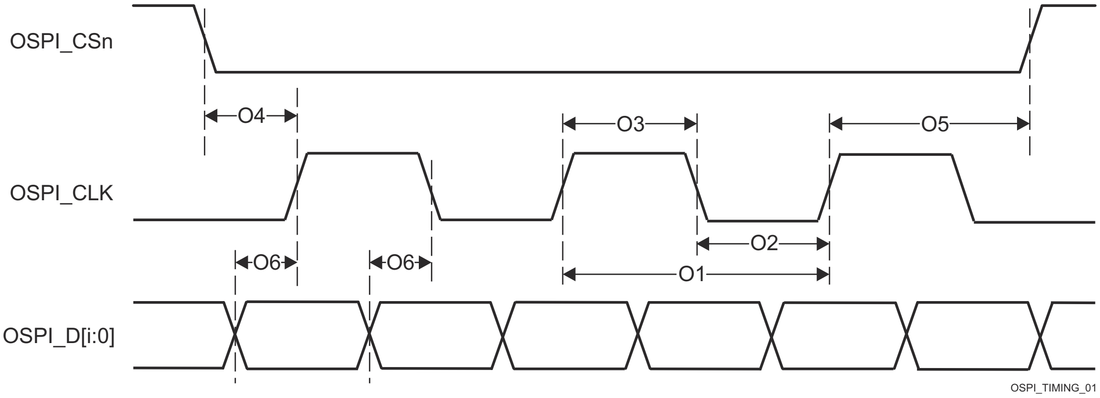


Figure 7-88. OSPI0 Switching Characteristics – Tap DDR, No Loopback

7.10.5.15 PCIe

The PCI-Express Subsystem is compliant with the PCIe® Base Specification, Revision 4.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Peripheral Component Interconnect Express (PCIe), see the *SERDES0 Signal Descriptions* and the corresponding subsection within *Detailed Description*.

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter of the device TRM.

7.10.5.16 PRU_ICSSG

The device has integrated two identical Programmable Real-Time Unit Subsystem and Industrial Communication Subsystems - Gigabit (PRU_ICSSG), PRU_ICSSG0 and PRU_ICSSG1. The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores in the device.

For more details about features and additional description information on the device PRU_ICSSG, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Note

The PRU_ICSSG contains a second layer of multiplexing to enable additional functionality on the PRU GPO and GPI signals. This internal wrapper multiplexing is described in the PRU_ICSSG chapter in the device TRM.

7.10.5.16.1 PRU_ICSSG Programmable Real-Time Unit (PRU)

Note

The PRU_ICSSG PRU signals have different functionality depending on the mode of operation. The signal naming in this section matches the naming used in the *PRU Module Interface* section in the device TRM.

Table 7-107. PRU_ICSSG PRU Timing Conditions

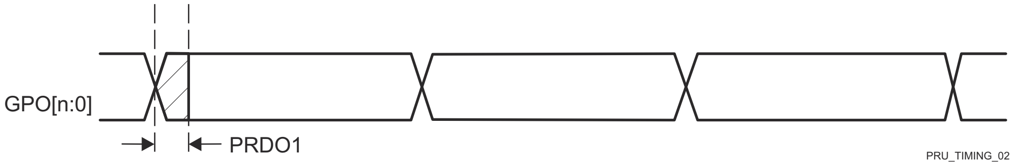
PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	30	pF

7.10.5.16.1.1 PRU_ICSSG PRU Direct Output Mode Timing

Table 7-108. PRU_ICSSG PRU Switching Characteristics – Direct Output Mode

see Figure 7-89

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRDO1	$t_{sk(GPO-GPO)}$	Skew, GPO to GPO		2	ns



A. n in GPO[n:0] = 19.

Figure 7-89. PRU_ICSSG PRU Direct Output Timing

7.10.5.16.1.2 PRU_ICSSG PRU Parallel Capture Mode Timing

Table 7-109. PRU_ICSSG PRU Timing Requirements – Parallel Capture Mode

see Figure 7-90 and Figure 7-91

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPC1	$t_{c(CLOCK)}$	Cycle time, CLOCKIN	20		ns
PRPC2	$t_{w(CLOCKL)}$	Pulse duration, CLOCKIN low	0.45P(1)		ns
PRPC3	$t_{w(CLOCKH)}$	Pulse duration, CLOCKIN high	0.45P(1)		ns
PRPC4	$t_{su(DATAIN-CLOCK)}$	Setup time, DATAIN valid before CLOCKIN active edge	4		ns
PRPC5	$t_{h(CLOCK-DATAIN)}$	Hold time, DATAIN valid after CLOCKIN active edge	0		ns

(1) P = CLOCKIN cycle time in ns

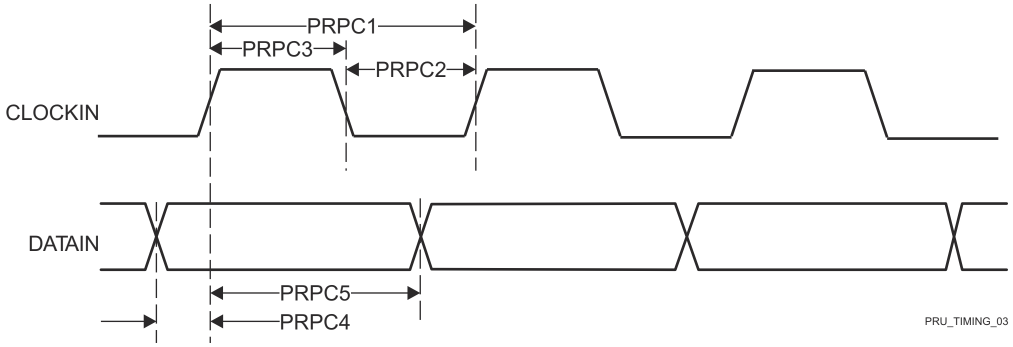


Figure 7-90. PRU_ICSSG PRU Parallel Capture Timing Requirements – Rising Edge Mode

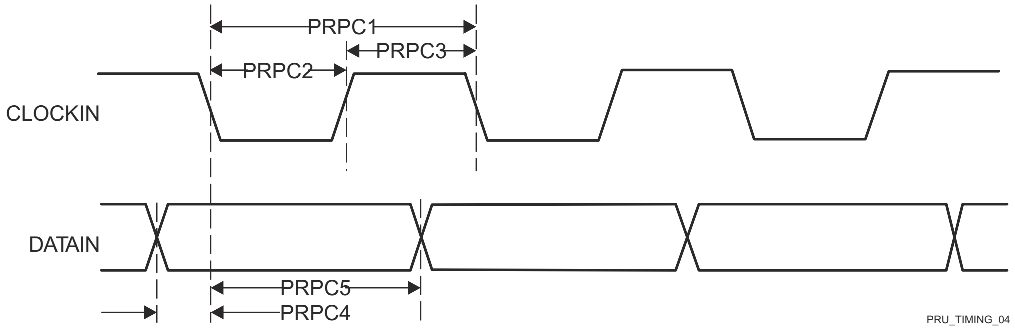


Figure 7-91. PRU_ICSSG PRU Parallel Capture Timing Requirements – Falling Edge Mode

7.10.5.16.1.3 PRU_ICSSG PRU Shift Mode Timing

Table 7-110. PRU_ICSSG PRU Timing Requirements – Shift In Mode

see Figure 7-92

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSI1	$t_{w(DATAINH)}$	Pulse duration, DATAIN high	2P(1) + 2		ns
PRSI2	$t_{w(DATAINL)}$	Pulse duration, DATAIN low	2P(1) + 2		ns

(1) P = Internal shift in clock period, defined by PRUn_GPI_DIV0 and PRUn_GPI_DIV1 bit fields in the ICSSG_GPCFGn_REG register. PRUn represents the respective PRU0 or PRU1 instance.

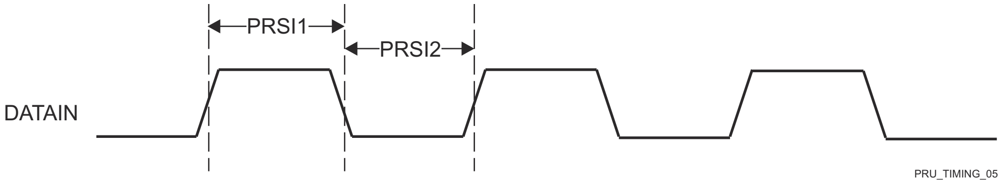


Figure 7-92. PRU_ICSSG PRU Shift In Timing

Table 7-111. PRU_ICSSG PRU Switching Characteristics – Shift Out Mode

see Figure 7-93

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSO1	$t_{c(CLOCKOUT)}$	Cycle time, CLOCKOUT	10		ns
PRSO2L	$t_{w(CLOCKOUTL)}$	Pulse duration, CLOCKOUT low	0.475P[1]Z[2] - 0.3		ns
PRSO2H	$t_{w(CLOCKOUTH)}$	Pulse duration, CLOCKOUT high	0.475P[1]Y[3] - 0.3		ns
PRSO3	$t_{d(CLOCKOUT-DATAOUT)}$	Delay time, CLOCKOUT to DATAOUT valid	-1	4	ns

(1) P = Software programmable shift out clock period, defined by PRUn_GPO_DIV0 and PRUn_GPO_DIV1 bit fields in the ICSSG_GPCFGn_REG register, where PRUn represents the respective PRU0 or PRU1 instance.

(2) The Z parameter is defined as follows, where PRUn represents the respective PRU0 or PRU1 instance.

a. If PRUn_GPI_DIV0 and PRUn_GPI_DIV1 are INTEGERS -or- if PRUn_GPI_DIV0 is a NON-INTEGER and PRUn_GPI_DIV1 is an EVEN INTEGER then, Z equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1).

b. If PRUn_GPI_DIV0 is a NON-INTEGER and PRUn_GPI_DIV1 is an ODD INTEGER then, Z equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 + 0.5).

c. If PRUn_GPI_DIV0 is an INTEGER and PRUn_GPI_DIV1 is a NON-INTEGER then, Z equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 + 0.5 * PRUn_GPI_DIV0).

d. If PRUn_GPI_DIV0 and PRUn_GPI_DIV1 are NON-INTEGERS then, Z equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 + 0.25 * PRUn_GPI_DIV0).

(3) The Y parameter is defined as follows, where PRUn represents the respective PRU0 or PRU1 instance.

a. If PRUn_GPI_DIV0 and PRUn_GPI_DIV1 are INTEGERS -or- if PRUn_GPI_DIV0 is a NON-INTEGER and PRUn_GPI_DIV1 is an EVEN INTEGER then, Y equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1).

b. If PRUn_GPI_DIV0 is a NON-INTEGER and PRUn_GPI_DIV1 is an ODD INTEGER then, Y equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 - 0.5).

c. If PRUn_GPI_DIV0 is an INTEGER and PRUn_GPI_DIV1 is a NON-INTEGER then, Y equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 - 0.5 * PRUn_GPI_DIV0).

d. If PRUn_GPI_DIV0 and PRUn_GPI_DIV1 are NON-INTEGERS then, Y1 equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 - 0.25 * PRUn_GPI_DIV0) and Y2 equals (PRUn_GPI_DIV0 * PRUn_GPI_DIV1 + 0.25 * PRUn_GPI_DIV0), where Y1 is the first high pulse and Y2 is the second high pulse.

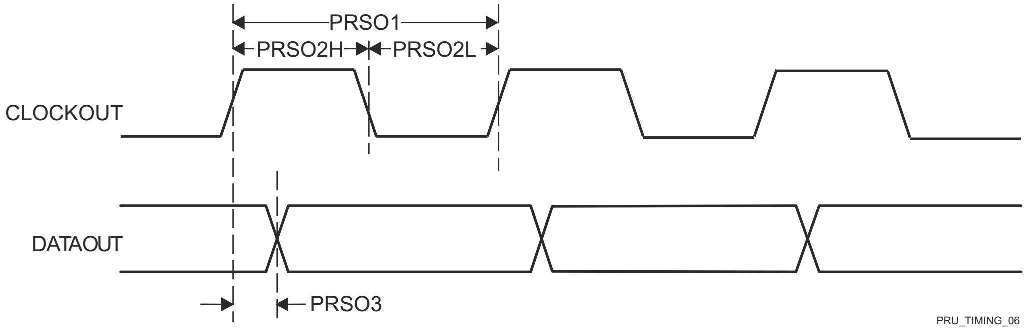


Figure 7-93. PRU_ICSSG PRU Shift Out Timing

7.10.5.16.1.4 PRU_ICSSG PRU Sigma Delta and Peripheral Interface

Table 7-112. PRU_ICSSG PRU Sigma Delta and Peripheral Interface Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	18	pF

7.10.5.16.1.4.1 PRU_ICSSG PRU Sigma Delta and Peripheral Interface Timing

Table 7-113. PRU_ICSSG PRU Timing Requirements – Sigma Delta Mode

see Figure 7-94 and Figure 7-95

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSD1	$t_{c(SD\_CLK)}$	Cycle time, SDx_CLK	40		ns
PRSD2L	$t_{w(SD\_CLKL)}$	Pulse duration, SDx_CLK low	20		ns
PRSD2H	$t_{w(SD\_CLKH)}$	Pulse duration, SDx_CLK high	20		ns
PRSD3	$t_{su(SD\_D-SD\_CLK)}$	Setup time, SDx_D valid before SDx_CLK active edge	10		ns
PRSD4	$t_{h(SD\_CLK-SD\_D)}$	Hold time, SDx_D valid before SDx_CLK active edge	5		ns

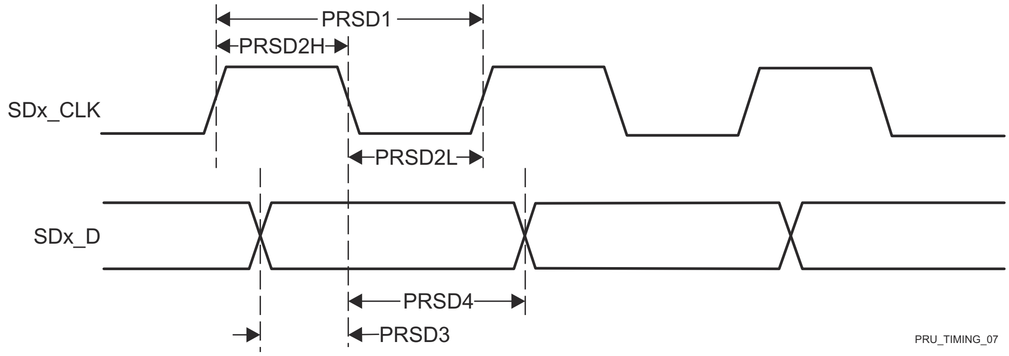


Figure 7-94. PRU_ICSSG PRU SD_CLK Falling Active Edge

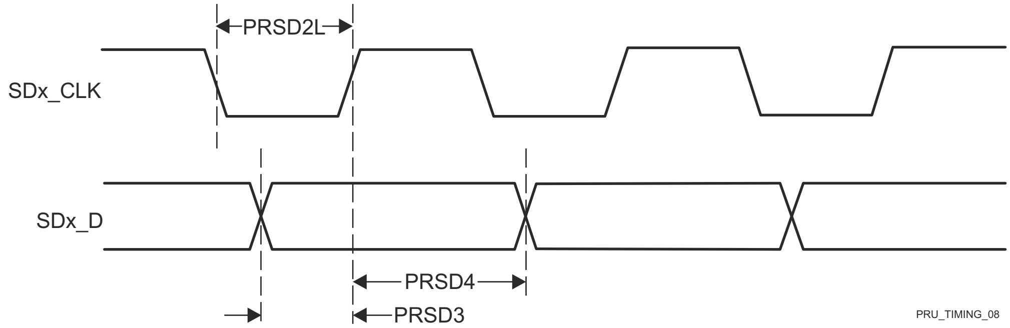


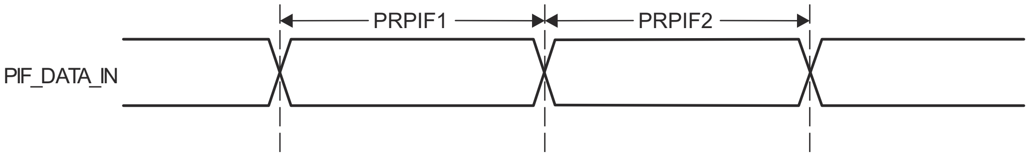
Figure 7-95. PRU_ICSSG PRU SD_CLK Rising Active Edge

Table 7-114. PRU_ICSSG PRU Timing Requirements – Peripheral Interface Mode

see Figure 7-96

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPIF1	$t_{w(PIF\_DATA\_INH)}$	Pulse duration, PIF_DATA_IN high	2 + 0.475*(4*P)[(1)]		ns
PRPIF2	$t_{w(PIF\_DATA\_INL)}$	Pulse duration, PIF_DATA_IN low	2 + 0.475*(4*P)[(1)]		ns

(1) P = 1x (or TX) clock period in ns, defined by PRUn_ED_TX_DIV_FACTOR and PRUn_ED_TX_DIV_FACTOR_FRAC in the ICSSG_PRUn_ED_TX_CFG_REG register. PRUn represents the respective PRU0 or PRU1 instance.



PRUPIF_TIMING_01

Figure 7-96. PRU_ICSSG PRU Peripheral Interface Timing Requirements

Table 7-115. PRU_ICSSG PRU Switching Characteristics – Peripheral Interface Mode

see Figure 7-97

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPIF3	$t_{c(PIF\_CLK)}$	Cycle time, PIF_CLK	30		ns
PRPIF4	$t_{w(PIF\_CLKH)}$	Pulse duration, PIF_CLK high	0.475*P[(1)]		ns
PRPIF5	$t_{w(PIF\_CLKL)}$	Pulse duration, PIF_CLK low	0.475*P[(1)]		ns
PRPIF6	$t_{d(PIF\_CLK-PIF\_DATA\_OUT)}$	Delay time, PIF_CLK fall to PIF_DATA_OUT	-5	5	ns
PRPIF7	$t_{d(PIF\_CLK-PIF\_DATA\_EN)}$	Delay time, PIF_CLK fall to PIF_DATA_EN	-5	5	ns

(1) P = 1x (or TX) clock period in ns, defined by PRUn_ED_TX_DIV_FACTOR and PRUn_ED_TX_DIV_FACTOR_FRAC in the ICSSG_PRUn_ED_TX_CFG_REG register. PRUn represents the respective PRU0 or PRU1 instance.

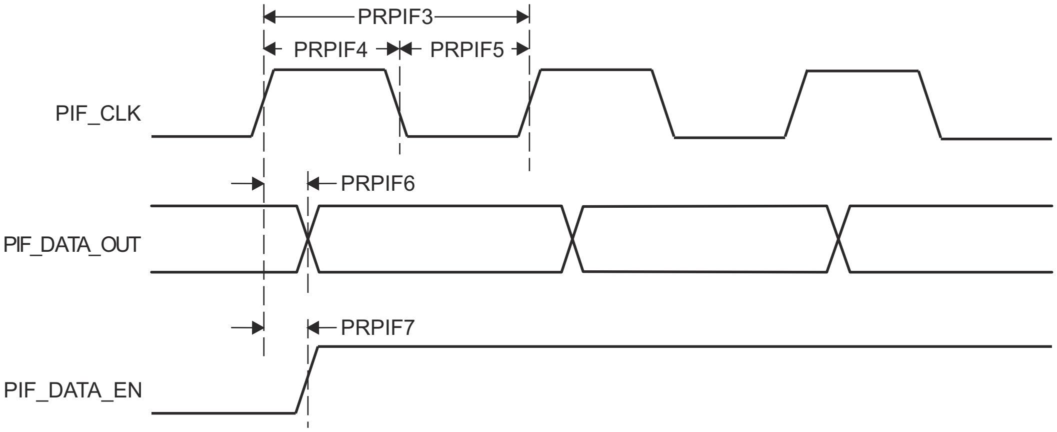


Figure 7-97. PRU_ICSSG PRU Peripheral Interface Switching Characteristics

7.10.5.16.2 PRU_ICSSG Pulse Width Modulation (PWM)

Table 7-116. PRU_ICSSG PWM Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

7.10.5.16.2.1 PRU_ICSSG PWM Timing

Table 7-117. PRU_ICSSG PWM Switching Characteristics

see Figure 7-98

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPWM1	$t_{sk(PWM\_A-PWM\_B)}$	Skew, PWM_A to PWM_B		5	ns

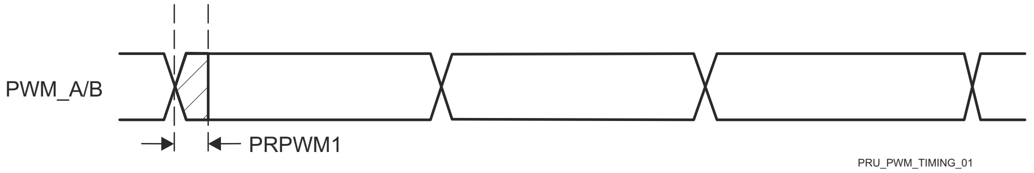


Figure 7-98. PRU_ICSSG PWM Timing

7.10.5.16.3 PRU_ICSSG Industrial Ethernet Peripheral (IEP)

Table 7-118. PRU_ICSSG IEP Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		1	3	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	EDC_SYNC_OUTx EDIO_OUTVALID	2	7	pF
		EDIO_DATA_OUT	3	10	pF

7.10.5.16.3.1 PRU_ICSSG IEP Timing

Table 7-119. PRU_ICSSG IEP Timing Requirements – Input Validated with SYNC

see Figure 7-99

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRIEP1	$t_{w(EDC\_SYNC\_OUTxL)}$	Pulse duration, EDC_SYNC_OUTx low	20P(1) - 2		ns
PRIEP2	$t_{w(EDC\_SYNC\_OUTxH)}$	Pulse duration, EDC_SYNC_OUTx high	20P(1) - 2		ns
PRIEP3	$t_{su(EDIO\_DATA\_IN-EDC\_SYNC\_OUTx)}$	Setup time, EDIO_DATA_IN valid before EDC_SYNC_OUTx active edge	20		ns
PRIEP4	$t_{h(EDC\_SYNC\_OUTx-EDIO\_DATA\_IN)}$	Hold time, EDIO_DATA_IN valid after EDC_SYNC_OUTx active edge	20		ns

(1) P = PRU_ICSSG IEP clock source period in ns.

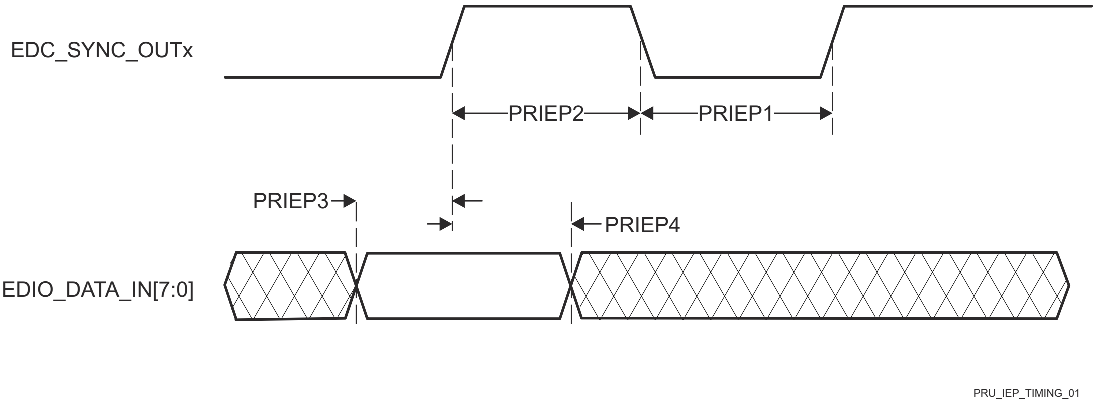


Figure 7-99. PRU_ICSSG IEP SYNC Timing Requirements

Table 7-120. PRU_ICSSG IEP Switching Characteristics – Digital IOs

see Figure 7-100

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
IEPIO1	$t_{w(EDIO\_OUTVALIDL)}$	Pulse duration, EDIO_OUTVALID low	14P(1) - 2		ns
IEPIO2	$t_{w(EDIO\_OUTVALIDH)}$	Pulse duration, EDIO_OUTVALID high	32P(1) - 2		ns
IEPIO3	$t_{d(EDIO\_OUTVALID-EDIO\_DATA\_OUT)}$	Delay time, EDIO_OUTVALID to EDIO_DATA_OUT	0	18P(1)	ns
IEPIO4	$t_{sk(EDIO\_DATA\_OUT)}$	EDIO_DATA_OUT skew		5	ns

(1) P = PRU_ICSSG IEP clock source period in ns.

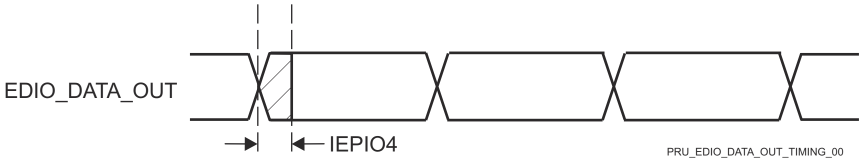


Figure 7-100. PRU_ICSSG IEP Digital IOs Timing Requirements

Table 7-121. PRU_ICSSG IEP Timing Requirements – LATCH_INx

see Figure 7-101

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRLA1	$t_{w(EDC\_LATCH\_INxL)}$	Pulse duration, EDC_LATCH_INx low	3P(1) + 2		ns
PRLA2	$t_{w(EDC\_LATCH\_INxH)}$	Pulse duration, EDC_LATCH_INx high	3P(1) + 2		ns

(1) P = PRU_ICSSG IEP clock source period in ns.

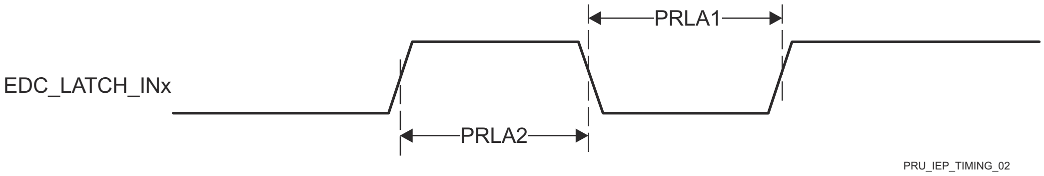


Figure 7-101. PRU_ICSSG IEP LATCH_INx Timing Requirements

7.10.5.16.4 PRU_ICSSG Universal Asynchronous Receiver Transmitter (UART)

Table 7-122. PRU_ICSSG UART Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	30(1)	pF

(1) This value represents an absolute maximum load capacitance. As the UART baud rate increases, it may be necessary to reduce the load capacitance to a value less than this maximum limit to provide enough timing margin for the attached device. The output rise/fall times increase as capacitive load increases, which decreases the time data is valid for the receiver of the attached devices. Therefore, it is important to understand the minimum data valid time required by the attached device at the operating baud rate. Then use the device IBIS models to verify the actual load capacitance on the UART signals does not increase the rise/fall times beyond the point where the minimum data valid time of the attached device is violated.

7.10.5.16.4.1 PRU_ICSSG UART Timing

Table 7-123. PRU_ICSSG UART Timing Requirements

see Figure 7-102

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{w(RXD)}$	Pulse width, receive data bit high or low	0.95U(1) (2)	1.05U(1) (2)	ns
2	$t_{w(RXDS)}$	Pulse width, receive start bit low	0.95U(1) (2)		ns

(1) U = UART baud time in ns = 1/programmed baud rate.
(2) This value defines the data valid time, where the input voltage is required to be above V_{IH} or below V_{IL}.

Table 7-124. PRU_ICSSG UART Switching Characteristics

see Figure 7-102

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	f(baud)	Programmed baud rate		12	Mbps
3	$t_{w(TXD)}$	Pulse width, transmit data bit high or low	U(1) - 2	U(1) + 2	ns
4	$t_{w(TXDS)}$	Pulse width, transmit start bit low	U(1) - 2	U(1) + 2	ns

(1) U = UART baud time in ns = 1/actual baud rate, where the actual baud rate is defined in the UART Baud Rate Settings table of the device TRM.

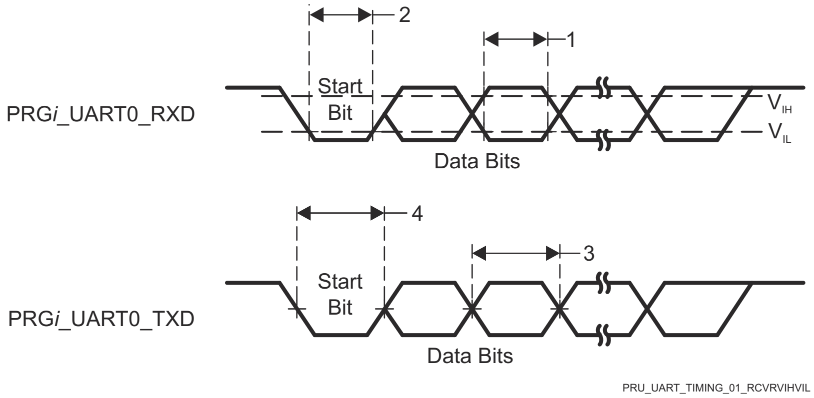


Figure 7-102. PRU_ICSSG UART Timing Requirements and Switching Characteristics

7.10.5.16.5 PRU_ICSSG Enhanced Capture Peripheral (ECAP)

Table 7-125. PRU_ICSSG ECAP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

7.10.5.16.5.1 PRU_ICSSG ECAP Timing

Table 7-126. PRU_ICSSG ECAP Timing Requirements

see Figure 7-103

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PREP1	$t_{w(CAP)}$	Pulse Duration, CAP (asynchronous)	2P(1) + 2		ns
PREP2	$t_{w(SYNCI)}$	Pulse Duration, SYNCI (asynchronous)	2P(1) + 2		ns

(1) P = CORE_CLK period in ns.

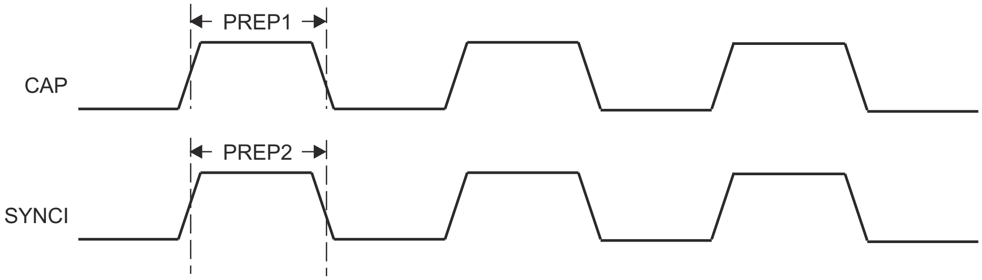


Figure 7-103. PRU_ICSSG ECAP Timing

Table 7-127. PRU_ICSSG ECAP Switching Characteristics

see Figure 7-104

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PREP3	$t_{w(APWM)}$	Pulse Duration, APWM high/low	2P(1) - 2		ns
PREP4	$t_{w(SYNCO)}$	Pulse Duration, SYNCO (asynchronous)	P(1) - 2		ns

(1) P = CORE_CLK period in ns.

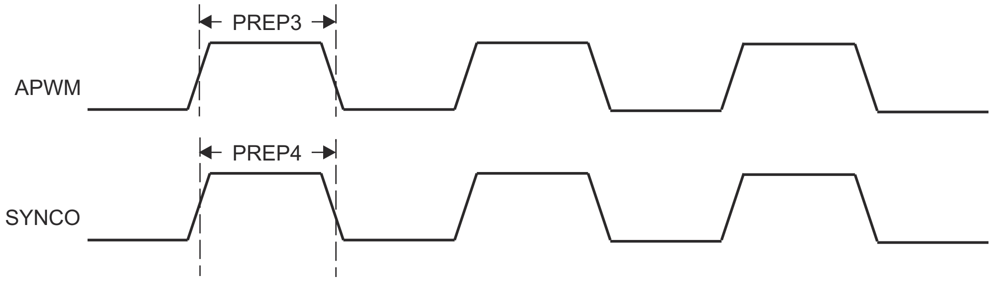


Figure 7-104. PRU_ICSSG ECAP Switching Characteristics

7.10.5.16.6 PRU_ICSSG RGMII, MII_RT, and Switch

For more information, see *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)* section in *Processors and Accelerators* chapter in the device TRM.

7.10.5.16.6.1 PRU_ICSSG MDIO Timing

Table 7-128, Table 7-129, Table 7-130, and Figure 7-105 present timing conditions, requirements, and switching characteristics for PRU_ICSSG MDIO.

Table 7-128. PRU_ICSSG MDIO Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	10	470	pF

Table 7-129. PRU_ICSSG MDIO Timing Requirements

see Figure 7-105

NO.	PARAMETER		MIN	MAX	UNIT
MDIO1	$t_{su(MDIO\_MDC)}$	Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high	90		ns
MDIO2	$t_{h(MDC\_MDIO)}$	Hold time, MDIO[x]_MDIO valid after MDIO[x]_MDC high	0		ns

Table 7-130. PRU_ICSSG MDIO Switching Characteristics

see Figure 7-105

NO.	PARAMETER		MIN	MAX	UNIT
MDIO3	$t_{c(MDC)}$	Cycle time, MDIO[x]_MDC	400		ns
MDIO4	$t_{w(MDCH)}$	Pulse Duration, MDIO[x]_MDC high	160		ns
MDIO5	$t_{w(MDCL)}$	Pulse Duration, MDIO[x]_MDC low	160		ns
MDIO7	$t_{d(MDC\_MDIO)}$	Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid	-150	150	ns

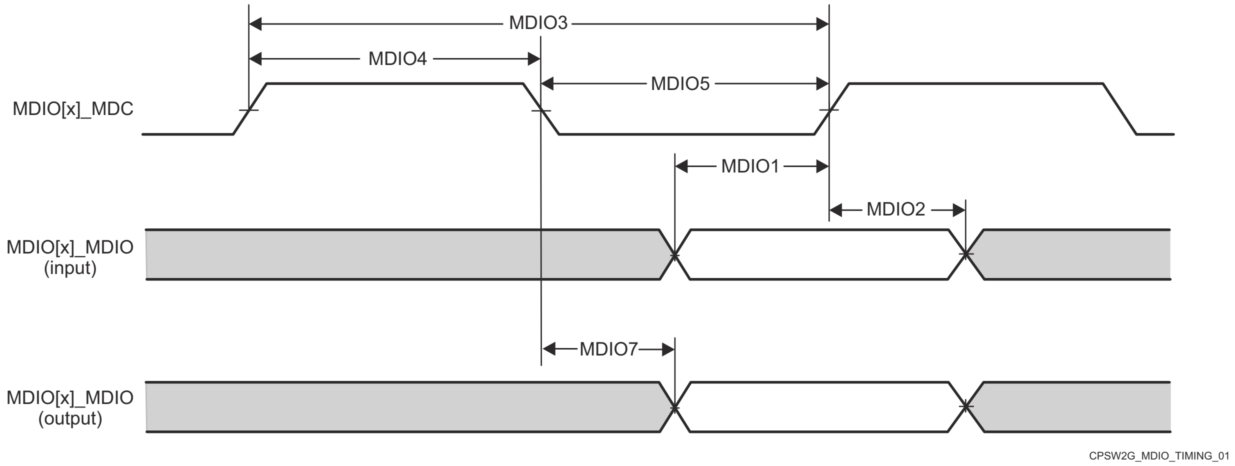


Figure 7-105. PRU_ICSSG MDIO Timing Requirements and Switching Characteristics

7.10.5.16.6.2 PRU_ICSSG MII Timing

Note

In order to ensure the MII_G_RT I/O timing values published in the device data sheet, the PRU_ICSSG ICSSGn_CORE_CLK (where n = 0 to 1) core clock must be configured for 200 MHz, 225 MHz, or 250 MHz and the TX_CLK_DELAYn (where n = 0 or 1) bit field in the ICSSG_TXCFG0/1 register must be set to 0h (default value).

Table 7-131, Table 7-132, Figure 7-106, Table 7-133, Figure 7-107, Table 7-134, Figure 7-108, Table 7-135, and Figure 7-109 present timing conditions, requirements, and switching characteristics for PRU_ICSSG MII.

Table 7-131. PRU_ICSSG MII Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	20	pF

Table 7-132. PRU_ICSSG MII Timing Requirements – MII[x]_RX_CLK

see Figure 7-106

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIR1	$t_{c(RX\_CLK)}$	Cycle time, MII[x]_RX_CLK	10 Mbps	399.96	400.04	ns
			100 Mbps	39.996	40.004	ns
PMIR2	$t_{w(RX\_CLKH)}$	Pulse Duration, MII[x]_RX_CLK High	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
PMIR3	$t_{w(RX\_CLKL)}$	Pulse Duration, MII[x]_RX_CLK Low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns

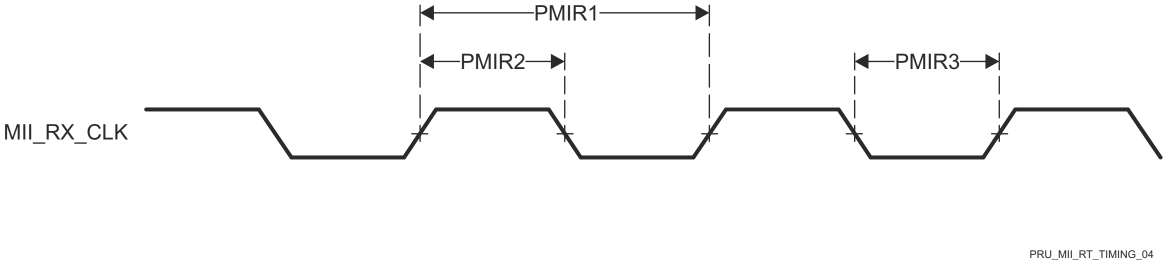


Figure 7-106. PRU_ICSSG MII[x]_RX_CLK Timing

Table 7-133. PRU_ICSSG MII Timing Requirements – MII[x]_RXD[3:0], MII[x]_RX_DV, and MII[x]_RX_ER

see Figure 7-107

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIR4	$t_{su(RXD-RX\_CLK)}$	Setup time, MII[x]_RXD[3:0] valid before MII[x]_RX_CLK	10 Mbps	8		ns
	$t_{su(RX\_DV-RX\_CLK)}$	Setup time, MII[x]_RX_DV valid before MII[x]_RX_CLK		8		ns
	$t_{su(RX\_ER-RX\_CLK)}$	Setup time, MII[x]_RX_ER valid before MII[x]_RX_CLK		8		ns
	$t_{su(RXD-RX\_CLK)}$	Setup time, MII[x]_RXD[3:0] valid before MII[x]_RX_CLK	100 Mbps	8		ns
	$t_{su(RX\_DV-RX\_CLK)}$	Setup time, MII[x]_RX_DV valid before MII[x]_RX_CLK		8		ns
	$t_{su(RX\_ER-RX\_CLK)}$	Setup time, MII[x]_RX_ER valid before MII[x]_RX_CLK		8		ns
PMIR5	$t_{h(RX\_CLK-RXD)}$	Hold time, MII[x]_RXD[3:0] valid after MII[x]_ RX_CLK	10 Mbps	8		ns
	$t_{h(RX\_CLK-RX\_DV)}$	Hold time, MII[x]_RX_DV valid after MII[x]_RX_CLK		8		ns
	$t_{h(RX\_CLK-RX\_ER)}$	Hold time, MII[x]_RX_ER valid after MII[x]_RX_CLK		8		ns
	$t_{h(RX\_CLK-RXD)}$	Hold time, MII[x]_RXD[3:0] valid after MII[x]_ RX_CLK	100 Mbps	8		ns
	$t_{h(RX\_CLK-RX\_DV)}$	Hold time, MII[x]_RX_DV valid after MII[x]_RX_CLK		8		ns
	$t_{h(RX\_CLK-RX\_ER)}$	Hold time, MII[x]_RX_ER valid after MII[x]_RX_CLK		8		ns

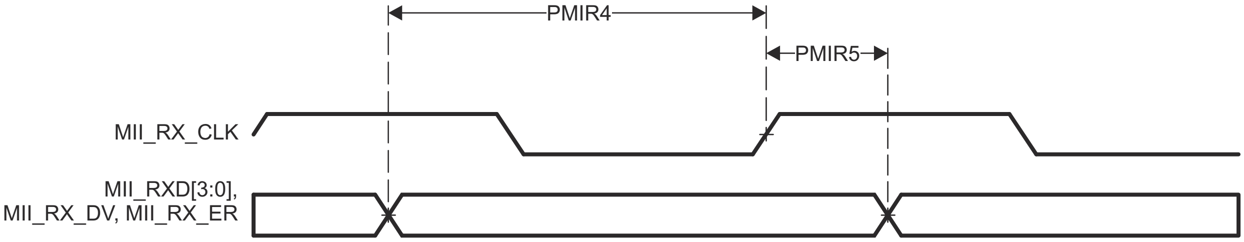


Figure 7-107. PRU_ICSSG MII[x]_RXD[3:0], MII[x]_RX_DV, and MII[x]_RX_ER Timing

Table 7-134. PRU_ICSSG MII Timing Requirements – MII[x]_TX_CLK

see Figure 7-108

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIT1	$t_{c(TX\_CLK)}$	Cycle time, MII[x]_TX_CLK	10 Mbps	399.96	400.04	ns
			100 Mbps	39.996	40.004	ns
PMIT2	$t_{w(TX\_CLKH)}$	Pulse Duration, MII[x]_TX_CLK High	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
PMIT3	$t_{w(TX\_CLKL)}$	Pulse Duration, MII[x]_TX_CLK Low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns

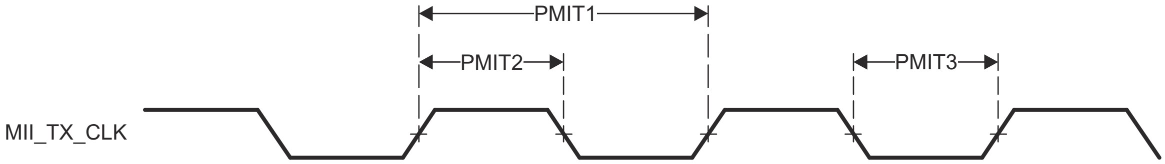


Figure 7-108. PRU_ICSSG MII[x]_TX_CLK Timing

Table 7-135. PRU_ICSSG MII Switching Characteristics – MII[x]_TXD[3:0] and MII[x]_TX_EN

see Figure 7-109

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIT4	$t_{d(TX\_CLK-TXD)}$	Delay time, MII[x]_TX_CLK High to MII[x]_TXD[3:0] valid	10 Mbps	0	25	ns
	$t_{d(TX\_CLK-TX\_EN)}$	Delay time, MII[x]_TX_CLK to MII[x]_TX_EN valid		0	25	ns
	$t_{d(TX\_CLK-TXD)}$	Delay time, MII[x]_TX_CLK High to MII[x]_TXD[3:0] valid	100 Mbps	0	25	ns
	$t_{d(TX\_CLK-TX\_EN)}$	Delay time, MII[x]_TX_CLK to MII[x]_TX_EN valid		0	25	ns

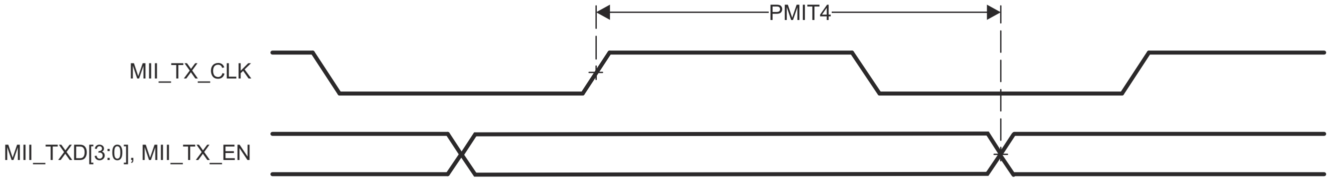


Figure 7-109. PRU_ICSSG MII[x]_TXD[3:0], MII[x]_TX_EN Timing

7.10.5.16.6.3 PRU_ICSSG RGMII Timing

Table 7-136, Table 7-137, Table 7-138, Figure 7-110, Table 7-139, Table 7-140, and Figure 7-111 present timing conditions, requirements, and switching characteristics for PRU_ICSSG RGMII.

Table 7-136. PRU_ICSSG RGMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD = 1.8V	1.44	5	V/ns
		VDD = 3.3V	2.65	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL		50	ps
		RGMII[x]_TXC, RGMII[x]_TD[3:0], RGMII[x]_TX_CTL		50	ps

Table 7-137. PRU_ICSSG RGMII Timing Requirements – RGMII[x]_RXC

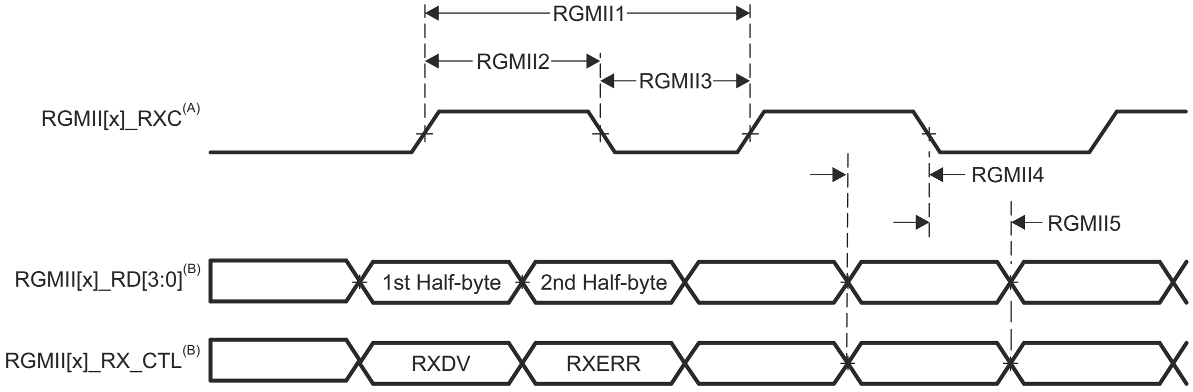
see Figure 7-110

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII1	$t_{c(RXC)}$	Cycle time, RGMII[x]_RXC	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
			1000 Mbps	7.2	8.8	ns
RGMII2	$t_{w(RXCH)}$	Pulse duration, RGMII[x]_RXC high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
RGMII3	$t_{w(RXCL)}$	Pulse duration, RGMII[x]_RXC low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns

Table 7-138. PRU_ICSSG RGMII Timing Requirements – RGMII[x]_RD[3:0] and RGMII[x]_RX_CTL

see Figure 7-110

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII4	$t_{su(RD-RXC)}$	Setup time, RGMII[x]_RD[3:0] valid before RXC high/low	10 Mbps	1		ns
			100 Mbps	1		ns
			1000 Mbps	1		ns
	$t_{su(RX\_CTL-RXC)}$	Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC high/low	10 Mbps	1		ns
			100 Mbps	1		ns
			1000 Mbps	1		ns
RGMII5	$t_{h(RXC-RD)}$	Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC high/low	10 Mbps	1		ns
			100 Mbps	1		ns
			1000 Mbps	1		ns
	$t_{h(RXC-RX\_CTL)}$	Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC high/low	10 Mbps	1		ns
			100 Mbps	1		ns
			1000 Mbps	1		ns



A. RGMII[x]_RXC must be externally delayed relative to the data and control pins.

B. Data and control information is received using both edges of the clocks. RGMII[x]_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_RXC and data bits 7-4 on the falling edge of RGMII[x]_RXC. Similarly, RGMII[x]_RX_CTL carries RXDV on rising edge of RGMII[x]_RXC and RXERR on falling edge of RGMII[x]_RXC.

Figure 7-110. PRU_ICSSG RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL Timing Requirements - RGMII Mode

Table 7-139. PRU_ICSSG RGMII Switching Characteristics – RGMII[x]_TXC

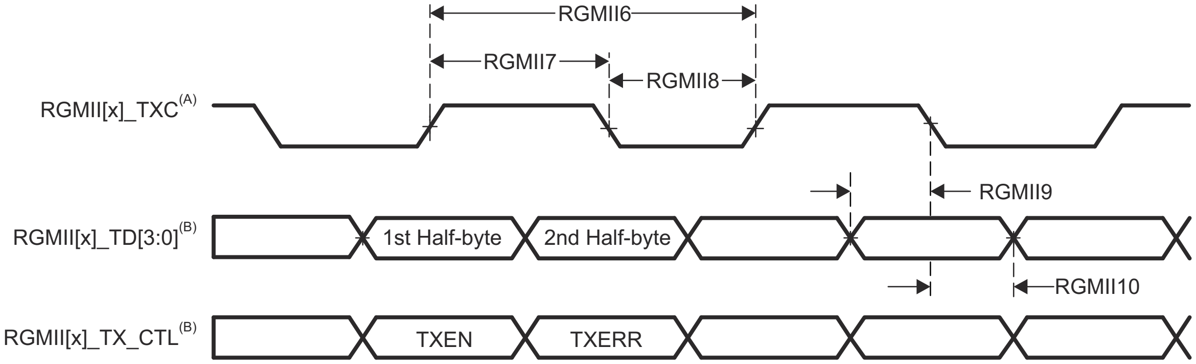
see Figure 7-111

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII6	$t_{c(TXC)}$	Cycle time, RGMII[x]_TXC	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
			1000 Mbps	7.2	8.8	ns
RGMII7	$t_{w(TXCH)}$	Pulse duration, RGMII[x]_TXC high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
RGMII8	$t_{w(TXCL)}$	Pulse duration, RGMII[x]_TXC low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns

Table 7-140. PRU_ICSSG RGMII Switching Characteristics – RGMII[x]_TD[3:0] and RGMII[x]_TX_CTL

see Figure 7-111

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII9	$t_{osu(TD-TXC)}$	Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low	10 Mbps	1.2		ns
			100 Mbps	1.2		ns
			1000 Mbps	1.2		ns
	$t_{osu(TX\_CTL-TXC)}$	Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low	10 Mbps	1.2		ns
			100 Mbps	1.2		ns
			1000 Mbps	1.2		ns
RGMII10	$t_{oh(TXC-TD)}$	Output setup time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low	10 Mbps	1.2		ns
			100 Mbps	1.2		ns
			1000 Mbps	1.2		ns
	$t_{oh(TXC-TX\_CTL)}$	Output setup time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low	10 Mbps	1.2		ns
			100 Mbps	1.2		ns
			1000 Mbps	1.2		ns



A. TXC is delayed internally before being driven to the RGMII[x]_TXC pin. This internal delay is always enabled.

B. Data and control information is received using both edges of the clocks. RGMII[x]_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_TXC and data bits 7-4 on the falling edge of RGMII[x]_TXC. Similarly, RGMII[x]_TX_CTL carries TXEN on rising edge of RGMII[x]_TXC and TXERR on falling edge of RGMII[x]_TXC.

Figure 7-111. PRU_ICSSG RGMII[x]_TXC, RGMII[x]_TD[3:0], and RGMII[x]_TX_CTL Switching Characteristics - RGMII Mode

7.10.5.17 Timers

For more details about features and additional description information on the device Timers, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 7-141. Timer Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	10	pF

Table 7-142. Timer Input Timing Requirements

see Figure 7-112

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T1	$t_{w(TINPH)}$	Pulse duration, high	CAPTURE	2 + 4P(1)		ns
T2	$t_{w(TINPL)}$	Pulse duration, low	CAPTURE	2 + 4P(1)		ns

(1) P = functional clock period in ns.

Table 7-143. Timer Output Switching Characteristics

see Figure 7-112

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T3	$t_{w(TOUTH)}$	Pulse duration, high	PWM	-2 + 4P(1)		ns
T4	$t_{w(TOUTL)}$	Pulse duration, low	PWM	-2 + 4P(1)		ns

(1) P = functional clock period in ns.

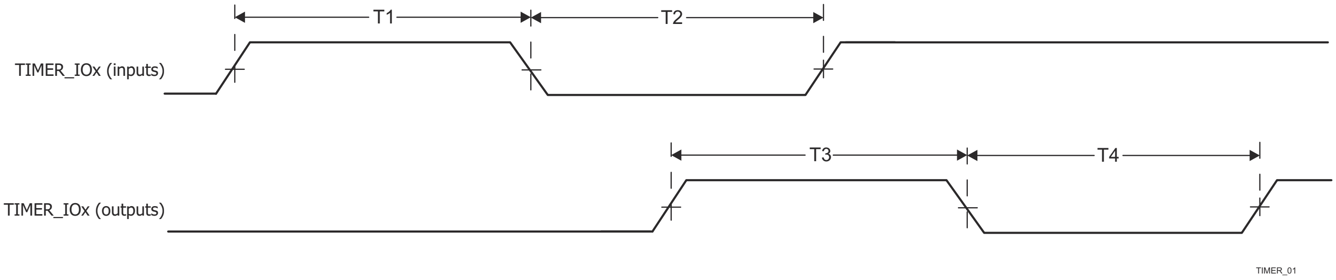


Figure 7-112. Timer Timing Requirements and Switching Characteristics

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

7.10.5.18 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 7-144. UART Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	30(1)	pF

(1) This value represents an absolute maximum load capacitance. As the UART baud rate increases, it may be necessary to reduce the load capacitance to a value less than this maximum limit to provide enough timing margin for the attached device. The output rise/fall times increase as capacitive load increases, which decreases the time data is valid for the receiver of the attached devices. Therefore, it is important to understand the minimum data valid time required by the attached device at the operating baud rate. Then use the device IBIS models to verify the actual load capacitance on the UART signals does not increase the rise/fall times beyond the point where the minimum data valid time of the attached device is violated.

Table 7-145. UART Timing Requirements

see Figure 7-113

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{w(RXD)}$	Pulse width, receive data bit high or low	0.95U(1) (2)	1.05U(1) (2)	ns
2	$t_{w(RXDS)}$	Pulse width, receive start bit low	0.95U(1) (2)		ns

(1) U = UART baud time in ns = 1/programmed baud rate.
(2) This value defines the data valid time, where the input voltage is required to be above V_{IH} or below V_{IL}.

Table 7-146. UART Switching Characteristics

see Figure 7-113

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{(baud)}$	Programmable baud rate for Main Domain UARTs		12	Mbps
		Programmable baud rate for MCU Domain UARTs		3.7	Mbps
3	$t_{w(TXD)}$	Pulse width, transmit data bit high or low	U(1) - 2.2	U(1) + 2.2	ns
4	$t_{w(TXDS)}$	Pulse width, transmit start bit low	U(1) - 2.2		ns

(1) U = UART baud time in ns = 1/programmed baud rate.

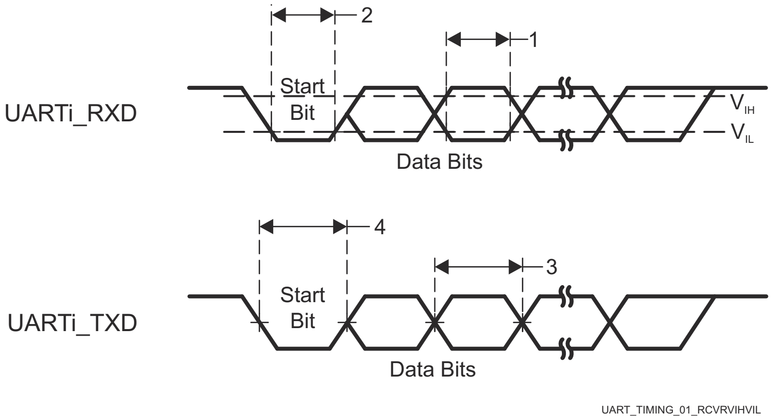


Figure 7-113. UART Timing Requirements and Switching Characteristics

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

7.10.5.19 USB

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

The USB 3.1 GEN1 subsystem is compliant with the Universal Serial Bus (USB) 3.1 Specification, revision 1.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the *SERDES0 Signal Descriptions* and the corresponding subsection within *Detailed Description*.

7.10.6 Emulation and Debug

For more details about features and additional description information on the device Trace and JTAG interfaces, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

7.10.6.1 Trace

Table 7-147. Trace Timing Conditions

PARAMETER			MIN	MAX	UNIT
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	5	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Mismatch)}$	Propagation delay mismatch across all traces	VDDSHV3 = 1.8V		200	ps
		VDDSHV3 =3.3V		100	ps

Table 7-148. Trace Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1.8V Mode					
DBTR1	$t_{c(TRC\_CLK)}$	Cycle time, TRC_CLK	6.50		ns
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	2.50		ns
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	2.50		ns
DBTR4	$t_{osu(TRC\_DATAV-TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	0.81		ns
DBTR5	$t_{oh(TRC\_CLK-TRC\_DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	0.81		ns
DBTR6	$t_{osu(TRC\_CTLV-TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	0.81		ns
DBTR7	$t_{oh(TRC\_CLK-TRC\_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	0.81		ns
3.3V Mode					
DBTR1	$t_{c(TRC\_CLK)}$	Cycle time, TRC_CLK	8.67		ns
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	3.58		ns
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	3.58		ns
DBTR4	$t_{osu(TRC\_DATAV-TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	1.08		ns
DBTR5	$t_{oh(TRC\_CLK-TRC\_DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	1.08		ns
DBTR6	$t_{osu(TRC\_CTLV-TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	1.08		ns
DBTR7	$t_{oh(TRC\_CLK-TRC\_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	1.08		ns

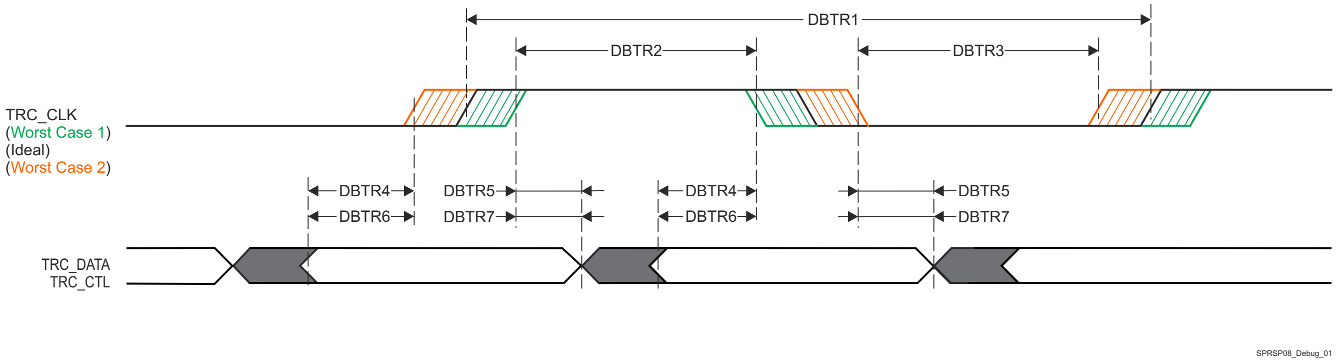


Figure 7-114. Trace Switching Characteristics

7.10.6.2 JTAG

Table 7-149. JTAG Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	2.0	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	5	15	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace Delay)}$	Propagation delay of each trace	83.5	1000(1)	ps
$t_{d(Trace Mismatch Delay)}$	Propagation delay mismatch across all traces		100	ps

(1) Maximum propagation delay associated with the JTAG signal traces has a significant impact on maximum TCK operating frequency. It may be possible to increase the trace delay beyond this value, but the operating frequency of TCK must be reduced to account for the additional trace delay.

Table 7-150. JTAG Timing Requirements

see Figure 7-115

NO.			MIN	MAX	UNIT
J1	$t_{c(TCK)}$	Cycle time minimum, TCK	45.5(1)		ns
J2	$t_{w(TCKH)}$	Pulse width minimum, TCK high	0.4P(2)		ns
J3	$t_{w(TCKL)}$	Pulse width minimum, TCK low	0.4P(2)		ns
J4	$t_{su(TDI-TCK)}$	Input setup time minimum, TDI valid to TCK high	4		ns
	$t_{su(TMS-TCK)}$	Input setup time minimum, TMS valid to TCK high	4		ns
J5	$t_{h(TCK-TDI)}$	Input hold time minimum, TDI valid from TCK high	2		ns
	$t_{h(TCK-TMS)}$	Input hold time minimum, TMS valid from TCK high	2		ns

(1) The maximum TCK operating frequency assumes the following timing requirements and switching characteristics for the attached debugger. The operating frequency of TCK must be reduced to provide appropriate timing margin if the debugger exceeds any of these assumptions.

- Minimum TDO setup time of 2.2 ns relative to the rising edge of TCK
- TDI and TMS output delay in the range of -16.1 ns to 14.1 ns relative to the falling edge of TCK

(2) P = TCK cycle time in ns

Table 7-151. JTAG Switching Characteristics

see Figure 7-115

NO.	PARAMETER		MIN	MAX	UNIT
J6	$t_{d(TCKL-TDOI)}$	Delay time minimum, TCK low to TDO invalid	0		ns
J7	$t_{d(TCKL-TDOV)}$	Delay time maximum, TCK low to TDO valid		14	ns

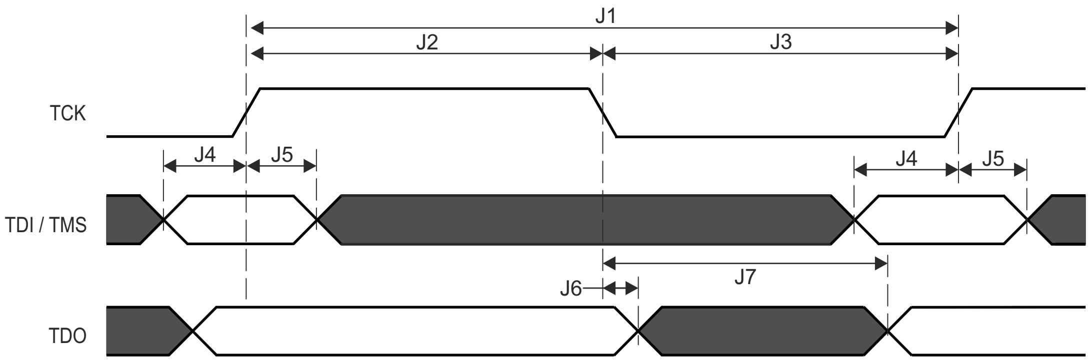


Figure 7-115. JTAG Timing Requirements and Switching Characteristics

8 Detailed Description

8.1 Overview

AM64x is an extension of the Sitara™ industrial-grade family of heterogeneous Arm processors. AM64x is built for industrial applications, such as motor drives and programmable logic controllers (PLCs), which require a unique combination of real-time processing and communications with applications processing. AM64x combines two instances of Sitara's gigabit TSN-enabled PRU-ICSSG, up to two Arm Cortex-A53 cores, up to four Cortex-R5F MCUs, and a Cortex-M4F MCU domain.

AM64x is architected to provide real-time performance through the high-performance R5Fs, Tightly-Coupled Memory banks, configurable SRAM partitioning, and low-latency paths to and from peripherals for rapid data movement in and out of the SoC. This deterministic architecture allows for AM64x to handle the tight control loops found in servo drives, while the peripherals like FSI, GPMC, PWMs, sigma delta decimation filters, and absolute encoder interfaces help enable a number of different architectures found in these systems.

The Cortex-A53s provide the powerful computing elements necessary for Linux applications. Linux, and Real-time (RT) Linux, is provided through TI's Processor SDK Linux which stays updated to the latest Long Term Support (LTS) Linux kernel, bootloader and Yocto file system on an annual basis. AM64x helps bridge the Linux world with the real-time world by enabling isolation between Linux applications and real-time streams through configurable memory partitioning. The Cortex-A53s can be assigned to work strictly out of DDR for Linux, and the internal SRAM can be broken up into various sizes for the Cortex-R5Fs to use together or independently.

The PRU_ICSSG in AM64x provides the flexible industrial communications capability necessary to run gigabit TSN, EtherCAT, PROFINET, EtherNet/IP, and various other protocols. In addition, the PRU_ICSSG also enables additional interfaces in the SoC including sigma delta decimation filter modules and absolute encoder interfaces.

Functional safety features can be enabled through the MCU domain with an integrated Cortex-M4F and dedicated peripheral set which can all be shared or isolated from the rest of the SoC. AM64x also supports secure boot.

Note

For more information on features, subsystems, and architecture of superset device System on Chip (SoC), see the device TRM.

8.2 Processor Subsystems

8.2.1 Arm Cortex-A53 Subsystem

The A53SS module supports the following features:

- Dual Core A53 Cluster
    - Full ARM v8-A Architecture Compliant
- AArch32 and AArch64 Execution States
- All exception levels EL0-3
- A32 Instruction Set (Previously ARM instruction set)
- T32 instruction set (previously Thumb instruction set)
- A64 Instruction Set
    - Advanced SIMD and Floating Point Extensions (NEON)
    - ARMv8 Cryptography Extensions
    - ARMv8 Cryptography Extensions
    - ARM GICv3 architecture
    - In-order pipeline with symmetric dual-issue of most instructions
    - Harvard L1 with system MMU
- 32 KB Instruction Cache
- 32 KB Data Cache
    - 256KB Shared L2 Cache
    - Generic Timer(s)
    - Debug
- 128-Bit VBUSM Initiator Interfaces (for axi_r and axi_r channels)
- 128-Bit VBUSM Target Interface (for Accelerator Coherency Port)
- 64-bit Grey-coded system input time
- 48-bit Grey-coded debug input time
- 32-bit VBUSP Target Interface for Debug
- Integrated PBIST Controller with BISOR

For more information, see *Dual-A53 MPU Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

8.2.2 Arm Cortex-R5F Subsystem (R5FSS)

The R5FSS is a dual-core implementation of the Arm® Cortex®-R5F processor configured for dual/single-core operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various wrappers for protocol conversion and address translation for easy integration into the SoC.

Note

The Cortex®-R5F processor is a Cortex-R5 processor that includes the optional Floating Point Unit (FPU) extension.

For more information, see *Dual-R5F Subsystem (R5FSS)* section in *Processors and Accelerators* chapter in the device TRM.

8.2.3 Arm Cortex-M4F (M4FSS)

The M4FSS module on the AM64x device provides a safety channel (secondary channel - working in conjunction with an external microcontroller)- or- a general purpose MCU.

The M4FSS module supports the following features:

- Cortex M4F With MPU
- ARMv7-M architecture
- Support for Nested Vectored Interrupt Controller (NVIC) with 64 inputs

- Ability to executed code from internal or external memories
- 192 KB of SRAM (I-Code)
- 64 KB of SRAM (D-Code)
- External access to internal memories if allowed
- Debug Support Including:
  - DAP based Debug to the CPU Core
  - Full Debug Features of CPU Core are enabled
  - Standard ITM trace
  - CTM Cross Trigger
  - ETM Trace Support
- Fault Detection and Correction
  - SECDED ECC protection on I-CODE
  - SECDED ECC protection on D-CODE
  - Fault Error Interrupt Output

For more information, see *Arm Cortex M4F Subsystem (M4FSS)* section in *Processors and Accelerators* chapter in the device TRM.

8.3 Accelerators and Coprocessors

8.3.1 Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU_ICSSG)

The PRU_ICSSG module supports the following main features:

- 3x PRUs
  - General-Purpose PRU (PRU)
  - Real-Time PRU(RTU_PRU)
  - Transmit PRU (TX_PRU)
- 2x Ethernet MII_G_RT configurable connection to PRUs
  - Up to 2x RGMII ports
  - Up to 2x MII ports
  - RX Classifier
- 2x Industrial Ethernet Peripheral (IEP) to manage and generate industrial Ethernet functions
- 2x Industrial Ethernet 64-bit timers, each with 10 capture and 16 compare events, along with slow and fast compensation.
- 1x MDIO
- 1x UART, with a dedicated 192-MHz clock input
- Supports up to 4 sets of 3-phased motor control, with 12 primary and 12 complimentary programmable PWM outputs.
- Supports up to 9 safety events with optional external trip I/O per PWM set with hardware glitch filter.
- 1x Enhanced Capture Module (ECAP)
- 1x Interrupt Controller (INTC)
  - 160 input events supported – 96 external, 64 internal
- Flexible power management support
- Integrated switched central resource with programmable priority
- All memories support ECC

For more information, see *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)* section in *Processors and Accelerators* chapter in the device TRM.

8.4 Other Subsystems

8.4.1 PDMA Controller

The Peripheral DMA is a simple DMA which has been architected to specifically meet the data transfer needs of peripherals, which perform data transfers using memory mapped registers accessed via a standard non-coherent bus fabric. The PDMA module is intended to be located close to one or more peripherals which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only statically configured Transfer Request (TR) operations.

The PDMA is only responsible for performing the data movement transactions which interact with the peripherals themselves. Data which is read from a given peripheral is packed by a PDMA source channel into a PSI-L data stream which is then sent to a remote peer UDMA-P destination channel which then performs the movement of the data into memory. Likewise, a remote UDMA-P source channel fetches data from memory and transfers it to a peer PDMA destination channel over PSI-L which then performs the writes to the peripheral.

The PDMA architecture is intentionally heterogeneous (UDMA-P + PDMA) to right size the data transfer complexity at each point in the system to match the requirements of whatever is being transferred to or from. Peripherals are typically FIFO based and do not require multi-dimensional transfers beyond their FIFO dimensioning requirements, so the PDMA transfer engines are kept simple with only a few dimensions (typically for sample size and FIFO depth), hardcoded address maps, and simple triggering capabilities.

Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs round-robin scheduling between channels in order to share the underlying DMA hardware.

There are five PDMA modules in the device.

For more information, see *PDMA Controller* section in *DMA Controllers* chapter in the device TRM.

8.4.2 Peripherals

8.4.2.1 ADC

The analog-to-digital converter (ADC) module is a single-channel general purpose analog-to-digital converter with an 8-input analog multiplexer, which supports 12-bit conversion samples from an analog front end (AFE).

There is one ADC module in the device.

For more information, see *Analog-to-Digital Converter (ADC)* section in *Peripherals* chapter in the device TRM.

8.4.2.2 DCC

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference.

The device has seven instances of DCC modules.

For more information, see *Dual Clock Comparator (DCC)* section in *Peripherals* chapter in the device TRM.

8.4.2.3 Dual Date Rate (DDR) External Memory Interface (DDRSS)

Integrated in MAIN domain: one instance of DDR Subsystem (DDRSS) is used as an interface to external RAM devices which can be utilized for storing program or data. DDRSS provides the following main features:

- Support of DDR4 / LPDDR4 memory types
- 16-bit memory bus interface with in-line ECC
- System bus interface: little Endian only with 128-bit data width
- Configuration bus Interface: little Endian only with 32-bit data width
- Support of dual rank configuration
- Support of automatic idle power saving mode when no or low activity is detected
- Class of Service (CoS) - three latency classes supported
- Prioritized refresh scheduling
- Statistical counters for performance management

For more information, see *DDR Subsystem (DDRSS)* section in *Peripherals* chapter in the device TRM.

8.4.2.4 ECAP

This section describes the Enhanced Capture (ECAP) module for the device.

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

8.4.2.5 EPWM

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The EPWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the EPWM is built up from smaller single channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

In the further description the letter x within a signal or module name is used to indicate a generic EPWM instance on a device. For example, output signals EPWMxA and EPWMxB refer to the output signals from the EPWM_x instance. Thus, EPWM1A and EPWM1B belong to EPWM1, EPWM2A and EPWM2B belong to EPWM2, and so forth.

Additionally, the EPWM integration allows this synchronization scheme to be extended to the capture peripheral modules (ECAP). The number of modules is device-dependent and based on target application needs. Modules can also operate stand-alone.

The device has six instances of EPWM modules.

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

8.4.2.6 ELM

The Error Location Module (ELM) is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. A host processor can then correct the data block by flipping the bits to which the ELM error-location outputs point.

When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller. ELM can be also used to support parallel NOR flash or NAND flash.

The General-Purpose Memory Controller (GPMC) probes data read from an external NAND flash and uses this to compute checksum-like information, called syndrome polynomials, on a per-block basis. Each syndrome polynomial gives a status of the read operations for a full block, including 512 bytes of data, parity bits, and an optional spare-area data field, with a maximum block size of 1023 bytes. Computation is based on a Bose-Chaudhuri-Hocquenghem (BCH) algorithm. The ELM extracts error addresses from these syndrome polynomials.

For more information, see *Error Location Module (ELM)* section in *Peripherals* chapter in the device TRM.

8.4.2.7 ESM

The Error Signaling Module (ESM) aggregates safety-related events and/or errors from throughout the device into one location. The module can signal both low and high priority interrupts to a processor to deal with a safety event and/or manipulate an I/O error pin to signal external hardware that an error has occurred. This allows an external controller to reset the device or keep the system in safe, known state.

For more information, see *Error Signaling Module (ESM)* section in *Peripherals* chapter in the device TRM.

8.4.2.8 GPIO

The general-purpose input/output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, user can write to an internal register to control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce host CPU interrupts and DMA synchronization events in different interrupt/event generation modes.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

8.4.2.9 EQEP

The Enhanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system. The disk of an incremental encoder is patterned with a single track of slots patterns. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is realized with a reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90 degrees out of phase from each other. These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel and vice versa.

The encoder wheel typically makes one revolution for every revolution of the motor or the wheel can be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000 revolutions per minute (rpm) results in a frequency of 166.6 KHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

8.4.2.10 General-Purpose Memory Controller (GPMC)

The General-Purpose Memory Controller is a unified memory controller dedicated for interfacing with external memory devices like:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in non-multiplexed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

For more information, see *General-Purpose Memory Controller* section in *Peripherals* chapter in the device TRM.

8.4.2.11 I2C

The Inter-IC Bus (I2C) interface is implemented using the mshsi2c module. This peripheral implements the multi-controller I2C bus, which allows serial transfer of 8-bit data to and from other I2C controller and target devices, through a two-wire interface.

The I2C module supports the following main features:

- Compliant with Philips I2C specification version 2.1
- Supported Speeds:
  - Standard mode (up to 100 K bits/s)
  - Fast mode (up to 400 K bits/s)
  - High-speed mode (up to 3.4 M bits/s), I2C0 and MCU_I2C0 only
- Multi-controller transmitter and target receiver mode
- Multi-controller receiver and target transmitter mode
- Combined controller transmit/receive and receive/transmit modes
- 7-bit and 10-bit device addressing modes
- Built-in 32-byte FIFO for buffered read or write
- Programmable multi-target channel (responds to 4 separates addresses)
- Programmable clock generation
- Support for asynchronous wake-up
- One interrupt line

For more information, see *Inter-Integrated Circuit (I2C) Interface* section in *Peripherals* chapter in the device TRM.

8.4.2.12 MCAN

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a high level of security. CAN has high immunity to electrical interference and the ability to self-diagnose and repair data errors. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The device supports 2 MCAN modules

For more information, see *Modular Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

8.4.2.13 MCRC Controller

VBUSM CRC controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of a memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a pre-determined good signature value. MCRC controller provides four channels to perform CRC calculation on multiple memories in parallel and can be used on any memory system. Channel 1 can also be put into data trace mode, where MCRC controller compresses each data being read through CPU read data bus.

For more information, see *MCRC Controller* section in *Interprocessor Communication* chapter in the device TRM.

8.4.2.14 MCSPI

The MCSPI module is a multichannel transmit/receive, controller/peripheral synchronous serial bus.

There are total of seven MCSPI modules in the device.

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

8.4.2.15 MMCSD

There are two Multi-Media Card/Secure Digital (MMCSD) modules inside the device - MMCSD0 and MMCSD1. Each MMCSD module includes one MMCSD Host Controller, where MMCSD0 is associated with MMC0 and MMCSD1 is associated with MMC1.

The MMCSD Host Controller supports:
- One controller with 8-bit wide data bus
- One controller with 4-bit wide data bus
- Support of eMMC5.1 Host Specification (JESD84-B51)
- Support of SD Host Controller Standard Specification - SDIO 3.00
- Integrated DMA controller supporting SD Advanced DMA - ADMA2 and ADMA3
- eMMC Electrical Standard 5.1 (JESD84-B51)
- Multi-Media card features:
  - Backward compatible with earlier eMMC standards
  - Legacy MMC SDR: 1.8 V, 8/4/1-bit bus width, 0-25 MHz, 25/12.5/3.125 MB/s
  - High Speed SDR: 1.8 V, 8/4/1-bit bus width, 0-50 MHz, 50/25/6.25 MB/s
  - High Speed DDR: 1.8 V, 8/4-bit bus width, 0-50 MHz, 100/50 MB/s
  - HS200 SDR: 1.8 V, 0-200 MHz, 8/4-bit bus width, 200/100 MB/s
- SD card support: SDIO, SDR12, SDR25, SDR50, DDR50
- System bus interface: CBA 4.0 VBUSM initiator port with 64-bit data width and 64-bit address, little Endian only
- Configuration bus interface: CBA 4.0 VBUSM with 32-bit data width, 32-bit aligned accesses only, linear incrementing addressing mode, little Endian only

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

8.4.2.16 OSPI

The Octal Serial Peripheral Interface (OSPI) module is a kind of Serial Peripheral Interface (SPI) module which allows single, dual, quad or octal read and write access to external flash devices. This module has a memory mapped register interface, which provides a direct memory interface for accessing data from external flash devices, simplifying software requirements.

The OSPI module is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signaling its completion via interrupts or status registers. For indirect operations, data is transferred between system memory and external flash memory via an internal SRAM which is loaded for writes and unloaded for reads by a device controller at low latency system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM should be accessed using user programmable configuration registers.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

8.4.2.17 Peripheral Component Interconnect Express (PCIe)

The PCIe subsystem supports the following main features:

- Dual mode – root port (RP) or end point (EP) modes.
- 1-lane configuration with up to 5.0GT/lane.
- 62.5/125 MHz operation on PIPE interface for Gen1/Gen2 respectively
- Constant 32-bit PIPE width for Gen1/Gen2 modes
- Maximum outbound payload size of 128 bytes
- Maximum inbound payload size of 128 bytes
- Maximum remote read request size of 4K bytes
- Maximum number of nonposted outstanding transactions: 8 on each VBUSM interface.
- Four virtual channels (4VC)
- Resizable BAR capability
- SRIS support
- Power Management
  - L1 Power Management Substate support
  - D1 support
  - L1 Power Shutoff support
- Legacy, MSI, and MSI-X interrupt support
- 32 outbound address translation regions
- Precision time measurement (PTM)

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter in the device TRM.

8.4.2.18 Serializer/Deserializer (SerDes) PHY

Integrated in the MAIN domain is one instance of high-speed differential interface implemented with Serializer/Deserializer (SerDes) Multi-protocol Multi-link PHY with the following main blocks:

- Single-lane SerDes PHY with common module for peripheral and Tx clocking handling
- Physical coding sub-block for data translation from/to the parallel interface, as well as data encoding/decoding and symbol alignment
- MUX module for device interface multiplexing into a single SerDes lane (Tx and Rx)
- A wrapper for sending control and reporting status signals from the SerDes and muxes

For more information, see *Serializer/Deserializer (SerDes)* section in *Peripherals* chapter in the device TRM.

8.4.2.19 Real Time Interrupt (RTI/WWDT)

This section describes the Real Time Interrupt (RTI) modules with Windowed Watchdog Timer (WWDT) functionality for the device.

For more information, see *Real Time Interrupt (RTI/WWDT) Module* section in *Peripherals* chapter of the device TRM.

8.4.2.20 Dual Mode Timer (DMTIMER)

The Dual Mode Timer (DMTIMER) module supports the following main features:

- Interrupts generated on overflow, compare, and capture events
- Free running 32-bit upward counter
- Supported operating modes:
  - Compare and capture modes
  - Auto-reload mode
  - Start-stop mode
- Programmable divider clock source (2n with n=[0:8])
- Dedicated input trigger for capture mode, and dedicated output trigger/PWM (pulse width modulation) signal
- On the fly read/write register (while counting)
- Generate 1-ms tick with 32768-Hz functional clock

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

8.4.2.21 UART

The UART module supports the following main features:

- 16C750 compatibility
- Baud rate from 300 bps up to 12 Mbps (MCU_UART0 and MCU_UART1 limited to 3.7 Mbps)
- Auto-baud between 1200 bps and 115.2 Kbps
- Software/hardware flow control
  - Programmable Xon/Xoff characters
  - Programmable Auto-RTS and Auto CTS
- Programmable serial interface characteristics
  - 5-, 6-, 7-, 8-bit characters
  - Even, odd, mark (always 1), space (always 0), or no parity (non-parity bit frame) bit generation and detection
  - 1-, 1.5-, or 2-stop bit generation
- Optional multi-drop transmission
- Configurable time-guard feature
- False start bit detection
- Line break generation and detection
- Modem control functions on UART0 (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully prioritized interrupt system controls
- Internal test and loopback capabilities
- RS-485 External transceiver auto flow control support

For more information, see *Universal Synchronous/Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

8.4.2.22 Universal Serial Bus Subsystem (USBSS)

The Universal Serial Bus Subsystem (USBSS) module supports the following main features:

General USB interface:

- Compliant with USB 3.1 specification
- Compliant with xHCI 1.1 specification
- Port configurable as:
  - USB host:
    - SuperSpeed Gen 1 (5 Gbps)
    - High-speed (480 Mbps)

    - Full-speed (12 Mbps)
    - Low-speed (1.5 Mbps)
  - USB device/peripheral:
    - High-speed (480 Mbps)
    - Full-speed (12Mbps)
  - USB Dual-Role device

USB Host mode features:

- 64 slots
- Up to 96 periodic simultaneous endpoints
- 256 primary streams
- MSI
- Root hub

For more information, see *Universal Serial Bus (USB) Subsystem* section in *Peripherals* chapter in the device TRM.

9 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Device Connection and Layout Fundamentals

9.1.1 Power Supply

9.1.1.1 Power Supply Designs

The **TPS65220** or **TPS65219** Power Management IC (PMIC) is recommended for an integrated power solution. This cost and space optimized solution is designed to power the device and its principal peripherals. For the full application note and related operational details, refer to *Powering the AM64x with the TPS65220 or TPS65219 PMIC*.

- Full device performance entitlement of TPS6522053 as validated on TI Evaluation boards
- Factory programmed configurations support power rail load steps, supply voltage accuracies and maximum load currents with margins
- Factory programmed configurations support LPDDR4 and DDR4 memory
- Meets all power supply sequencing requirements, refer to *Power Supply Sequencing*

Note

AM64x also supports discrete power supply topologies and customized power designs to meet various system requirements.

9.1.1.2 Power Distribution Network Implementation Guidance

The Sitara Processor Power Distribution Networks: Implementation and Analysis provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI *only* supports designs that follow the board design guidelines contained in the application report.

9.1.2 External Oscillator

For more information about External Oscillators, see the *Clock Specifications* section.

9.1.3 JTAG, EMU, and TRACE

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the XDS Target Connection Guide.

For recommendations on JTAG, EMU, and TRACE routing, see the Emulation and Trace Headers Technical Reference Manual

9.1.4 Unused Pins

For more information about Unused Pins, see the *Pin Connectivity Requirements* section.

9.2 Peripheral- and Interface-Specific Design Information

9.2.1 DDR Board Design and Layout Guidelines

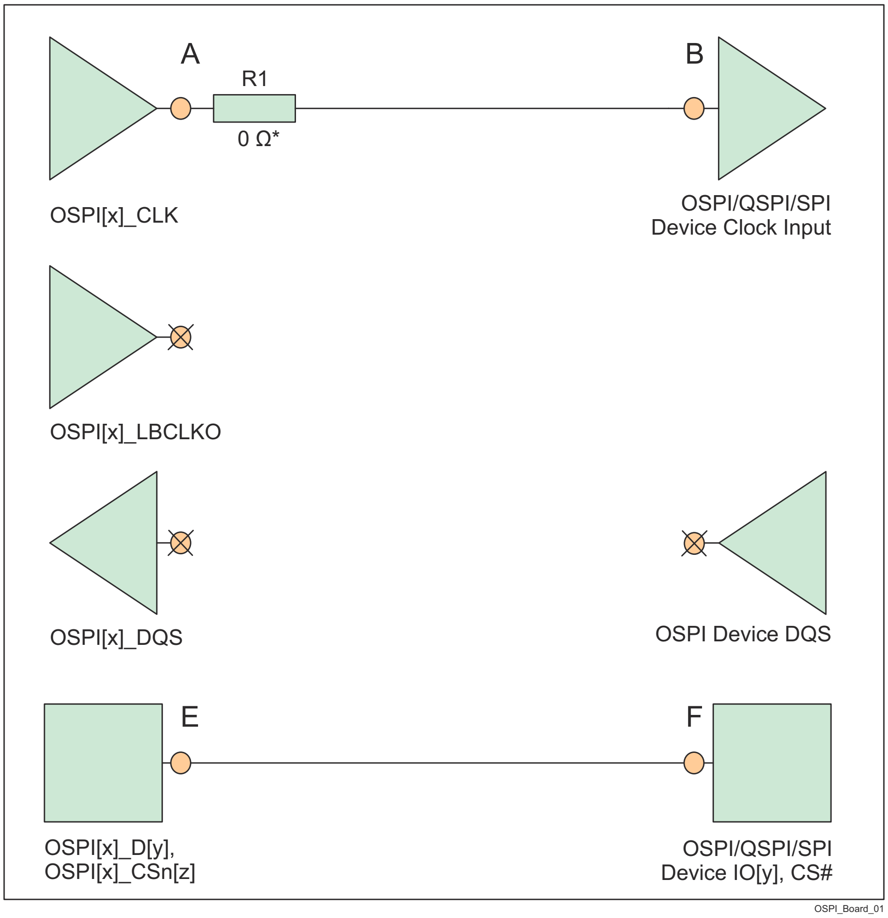
The goal of the AM64x\AM243x DDR Board Design and Layout Guidelines is to make the DDR system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using DDR4 or LPDDR4 memories that follow the guidelines in this document.

9.2.2 OSPI/QSPI/SPI Board Design and Layout Guidelines

The following section details the PCB routing guidelines that must be observed when connecting OSPI, QSPI, or SPI devices.

9.2.2.1 No Loopback, Internal PHY Loopback, and Internal Pad Loopback

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B) must be ≤ 450 ps (~7cm as stripline or ~8cm as microstrip)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 9-1
- Propagation delays and matching:
  - (A to B) ≤ 450 ps
  - (E to F, or F to E) = ((A to B) ± 60 ps)



* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK pin, is placeholder for fine tuning, if needed.

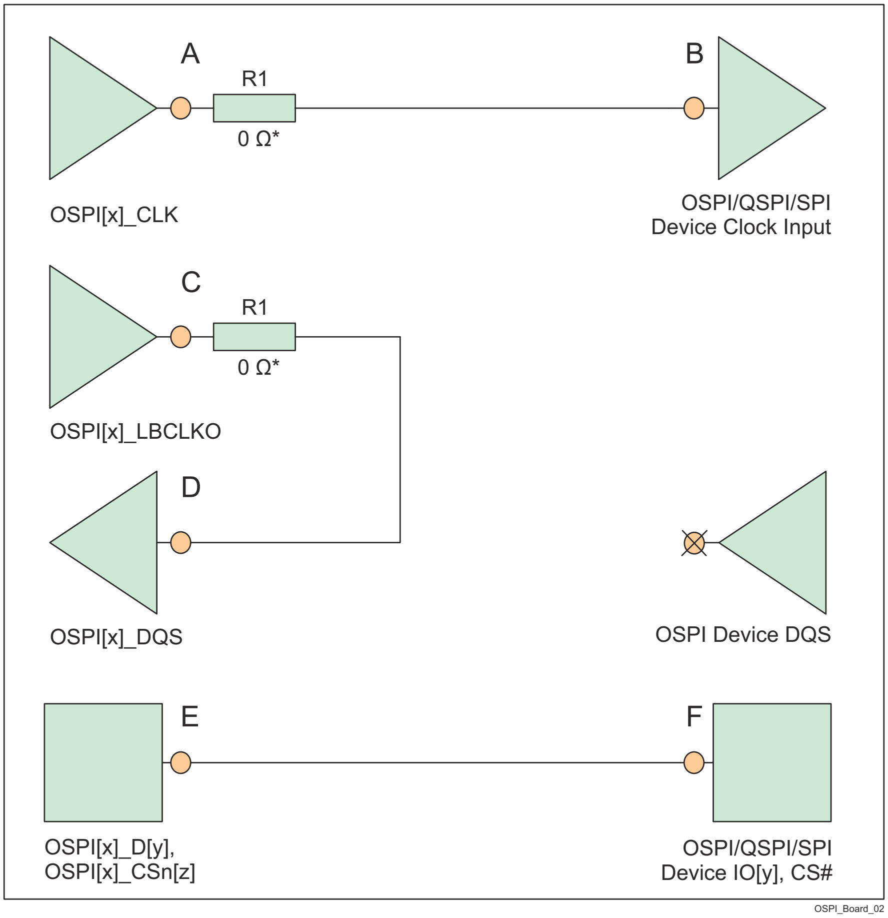
Figure 9-1. OSPI Connectivity Schematic for No Loopback, Internal PHY Loopback, and Internal Pad Loopback

9.2.2.2 External Board Loopback

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The OSPI[x]_LBCLKO output pin must be looped back to the OSPI[x]_DQS input pin
- The signal propagation delay of the OSPI[x]_LBCLKO pin to the OSPI[x]_DQS pin (C to D) must be approximately twice the propagation delay of the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 9-2
- Propagation delays and matching:
  - (C to D) = 2 x ((A to B) ± 30 ps), see the exception note below.
  - (E to F, or F to E) = ((A to B) ± 60 ps)

Note

The External Board Loopback hold time requirement (defined by parameter number O16 in Table 7-101, *OSPI0 Timing Requirements - PHY DDR Mode*) may be larger than the hold time provided by a typical OSPI/QSPI/SPI device. In this case, the propagation delay of OPSI[x]_LBCLKO pin to the OSPI[x]_DQS pin (C to D) can be reduced to provide additional hold time.

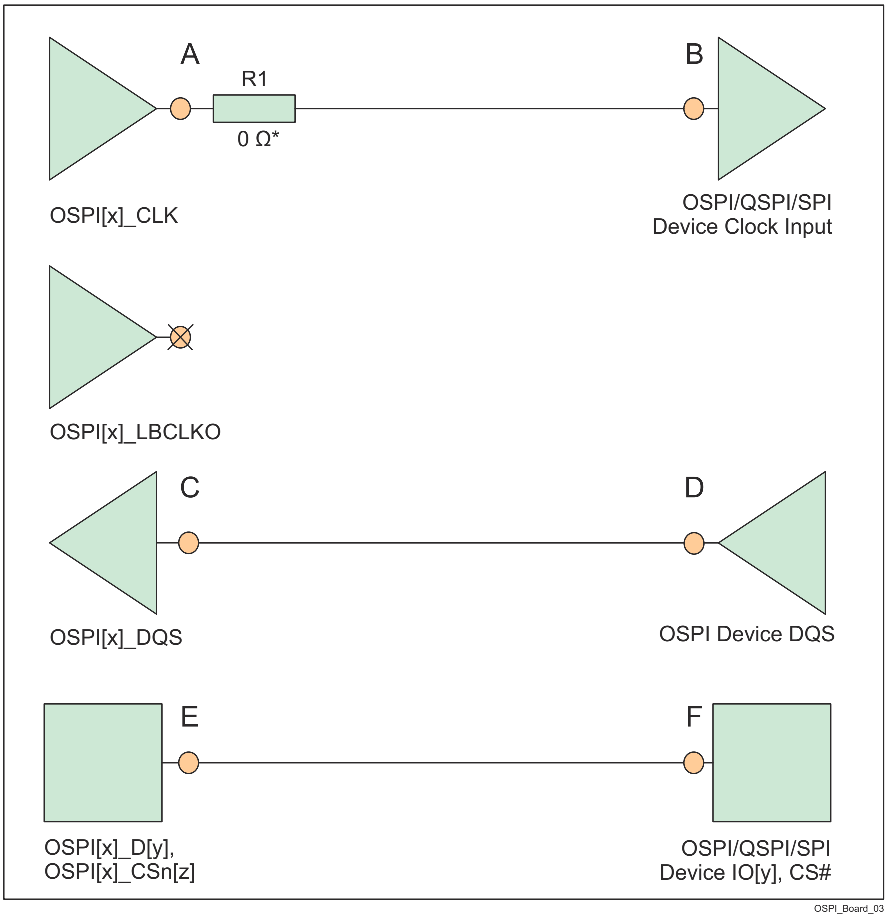


* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK and OSPI[x]_LBCLKO pins, is a placeholder for fine tuning, if needed.

Figure 9-2. OSPI Connectivity Schematic for External Board Loopback

9.2.2.3 DQS (only available in Octal SPI devices)

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The DQS pin of the attached OSPI/QSPI/SPI device must be connected to OSPI[x]_DQS pin
- The signal propagation delay from the attached OSPI/QSPI/SPI device DQS pin to the OSPI[x]_DQS pin (D to C) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in Figure 9-3
- Propagation delays and matching:
  - (D to C) = ((A to B) ± 30 ps)
  - (E to F, or F to E) = ((A to B) ± 60 ps)



* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK pin, is a placeholder for fine tuning, if needed.

Figure 9-3. OSPI Connectivity Schematic for DQS

9.2.3 USB VBUS Design Guidelines

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5 V for normal operation, and as high as 20 V when the Power Delivery addendum is supported. Some automotive applications require a max voltage to be 30 V.

The device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the Figure 9-4), which limits the voltage applied to the actual device pin (USB0_VBUS). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of Zener diode at 5 V should be less than 100 nA.

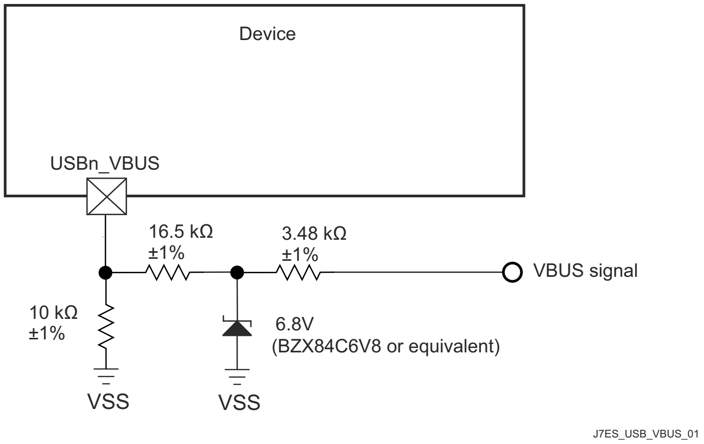


Figure 9-4. USB VBUS Detect Voltage Divider / Clamp Circuit

The USB0_VBUS pin can be considered to be fail-safe because the external circuit in Figure 9-4 limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

9.2.4 System Power Supply Monitor Design Guidelines

The VMON_VSYS pin provides a way to monitor a system power supply. This system power supply is typically a single pre-regulated power source for the entire system and can be connected to the VMON_VSYS pin via and external resistor divider circuit. This system supply is monitored by comparing the external voltage divider output voltage to an internal voltage reference, where a power fail event is triggered when the voltage applied to VMON_VSYS drops below the internal reference voltage. The actual system power supply voltage trip point is determined by the system designer when selecting component values used to implement the external resistor voltage divider circuit.

When building the resistor divider circuit the designer must understand various factors which contribute to variability in the system power supply monitor trip point. The first thing to consider is the initial accuracy of the VMON_VSYS input threshold which has a nominal value of 0.45 V, with a variation of ±3%. Precision 1% resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider. This minimizes variability contributed by resistor value tolerances. Input leakage current associated with VMON_VSYS must also be considered since any current flowing into the pin creates a loading error on the voltage divider output. The VMON_VSYS input leakage current can be in the range of 10 nA to 2.5 µA when applying 0.45 V.

Note

The resistor voltage divider shall be designed such that the output voltage never exceeds the maximum value defined in the *Recommended Operating Conditions* section, during normal operating conditions.

Figure 9-5 presents an example, where the system power supply is nominally 5 V and the maximum trigger threshold is 5 V - 10%, or 4.5 V.

For this example, the designer must understand which variables effect the maximum trigger threshold when selecting resistor values. A device which has a VMON_VSYS input threshold of 0.45 V + 3% needs to be considered when trying to design a voltage divider that doesn't trip until the system supply drops 10%. The effect of resistor tolerance and input leakage also needs to be considered, but the contribution to the maximum trigger point is not obvious. When selecting component values which produce a maximum trigger voltage, the system designer must consider a condition where the value of R1 is 1% low and the value of R2 is 1% high combined with a condition where input leakage current for the VMON_VSYS pin is 2.5 µA. When implementing a resistor divider where R1 = 4.81 KΩ and R2 = 40.2 KΩ, the result is a maximum trigger threshold of 4.517 V.

Once component values have been selected to satisfy the maximum trigger voltage as described above, the system designer can determine the minimum trigger voltage by calculating the applied voltage that produces an output voltage of 0.45 V - 3% when the value of R1 is 1% high and the value of R2 is 1% low, and the input leakage current is 10 nA, or zero. Using an input leakage of zero with the resistor values given above, the result is a minimum trigger threshold of 4.013 V.

This example demonstrates a system power supply voltage trip point that ranges from 4.013 V to 4.517 V. Approximately 250 mV of this range is introduced by VMON_VSYS input threshold accuracy of ±3%, approximately 150 mV of this range is introduced by resistor tolerance of ±1%, and approximately 100 mV of this range is introduced by loading error when VMON_VSYS input leakage current is 2.5 µA.

The resistor values selected in this example produces approximately 100 µA of bias current through the resistor divider when the system supply is 4.5 V. The 100 mV of loading error mentioned above can be reduced to about 10 mV by increasing the bias current through the resistor divider to approximately 1 mA. So resistor divider bias current vs loading error is something the system designer needs to consider when selecting component values.

The system designer must also consider implementing a noise filter on the voltage divider output since VMON_VSYS has minimum hysteresis and a high-bandwidth response to transients. This can be done by installing a capacitor across R1 as shown in Figure 9-5. However, the system designer must determine the response time of this filter based on system supply noise and expected response to transient events.

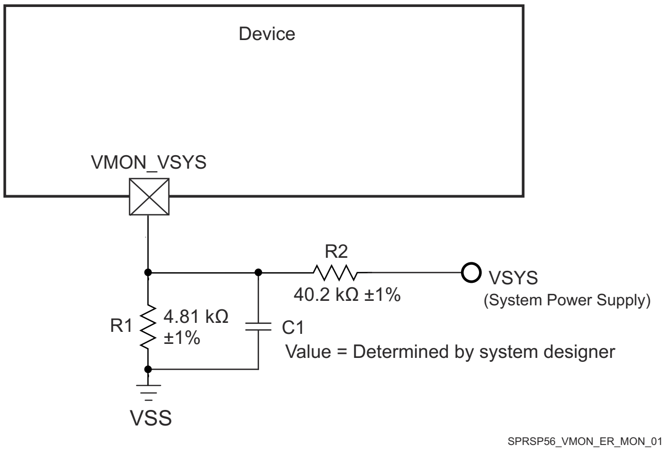


Figure 9-5. System Supply Monitor Voltage Divider Circuit

VMON_1P8_MCU and VMON_1P8_SOC pins provide a way to monitor external 1.8 V power supplies. These pins must be connected directly to their respective power source. An internal resistor divider with software control is implemented inside the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

VMON_3P3_MCU and VMON_3P3_SOC pins provide a way to monitor external 3.3 V power supplies. These pins must be connected directly to their respective power source. An internal resistor divider with software control is implemented inside the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

9.2.5 High Speed Differential Signal Routing Guidance

The High Speed Interface Layout Guidelines provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application note.

9.2.6 Thermal Solution Guidance

The Thermal Design Guide for DSP and ARM Application Processors provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application note.

9.3 Clock Routing Guidelines

9.3.1 Oscillator Routing

When designing the printed-circuit board:

- Place all crystal circuit components as close as possible to the respective device pins.
- Route the crystal circuit traces on the outer layer of the PCB and minimize trace lengths to reduce parasitic capacitance and minimize crosstalk from other signals.
- Place a continuous ground plane on the adjacent layer of the PCB such that it is under all crystal circuit components and crystal circuit traces.
- Route a ground guard around the crystal circuit components to shield it from any adjacent signals routed on the same layer as the crystal circuit traces. Insert multiple vias to stitch down the ground guard such that it does not have any unterminated stubs.
- Route a ground guard between the MCU_OSC0_XI and MCU_OSC0_XO signals to shield the MCU_OSC0_XI signal from the MCU_OSC0_X0 signal. Insert multiple vias to stitch down the ground guard such that it does not have any unterminated stubs.
- Connect all crystal circuit ground connections and ground guard connections directly to the adjacent layer ground plane, and the device VSS ground plane if they are implemented separately on different layers of the PCB.

Note

Implementing a ground guard between the MCU_OSC0_XI and MCU_OSC0_XO signals is critical to minimize shunt capacitance between the two signals. Routing these two signals adjacent to each other without a ground guard between them will effectively reduce the gain of the oscillator amplifier, which reduces its ability to start oscillation.

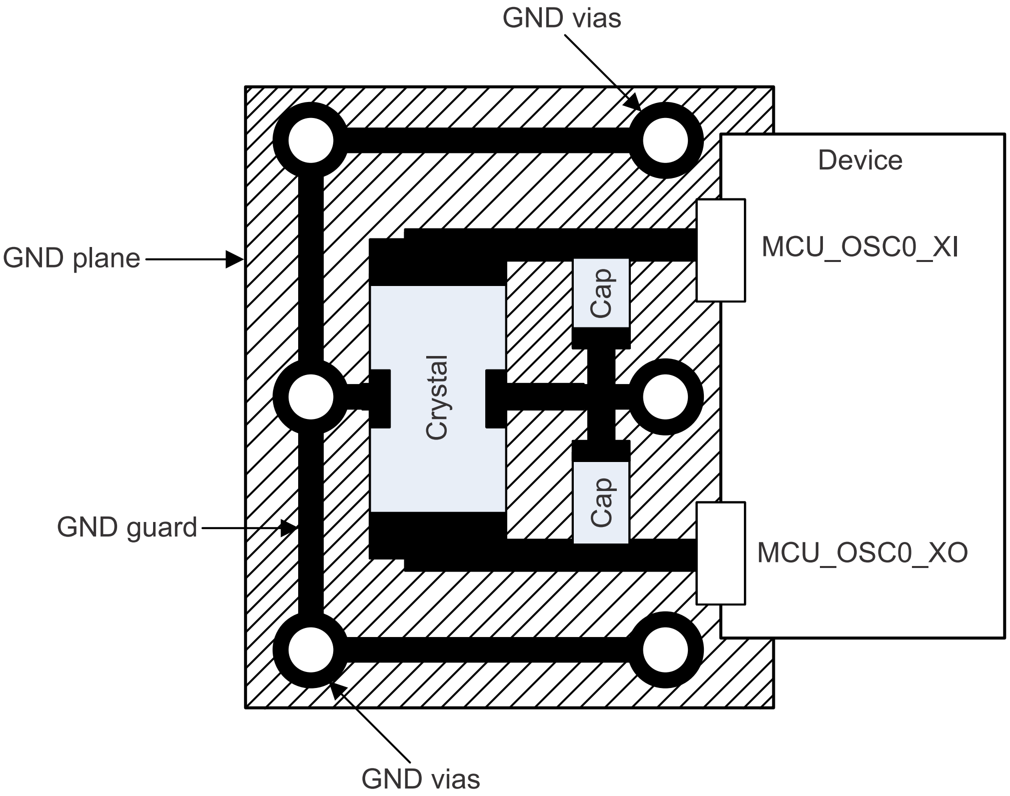


Figure 9-6. MCU_OSC0 PCB requirements

10 Device and Documentation Support

10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all embedded processor devices and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, AM6442BSFFHAALV). Texas Instruments recommends two of three possible prefix designators for related support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X	Experimental device that is not necessarily representative of the device's final electrical specifications and may not use production assembly flow.
P	Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
null (BLANK)	Production version of the silicon die that is fully qualified and meets final electrical specifications.

Support tool development evolutionary flow:

TMDX	Development-support product that has not yet completed Texas Instruments internal qualification testing.
TMDS	Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM64x devices in the ALV package type, see the Package Option Addendum at the end of this document, the TI website (ti.com), or contact your TI sales representative.

10.1.1 Standard Package Symbolization

Note

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

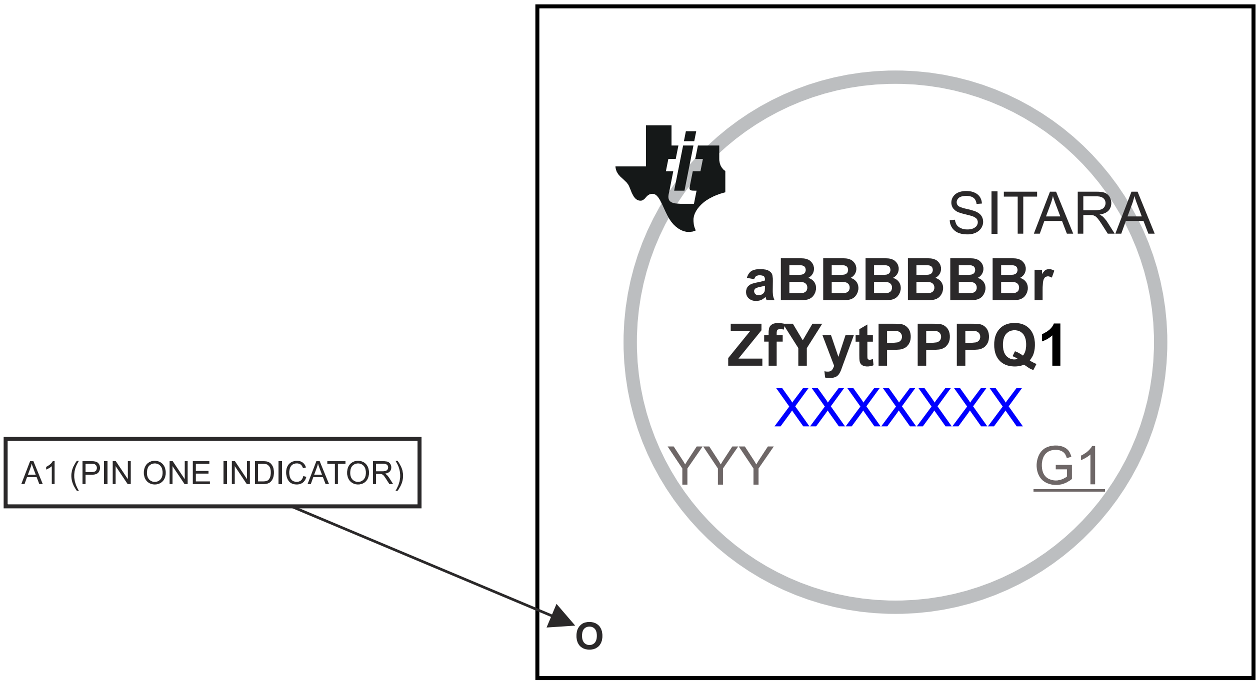


Figure 10-1. Printed Device Reference

10.1.2 Device Naming Convention

Table 10-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
a	Device evolution stage	X	Prototype
		P	Preproduction (production test flow, no reliability data)
		BLANK	Production
BBBBBB	Base production part number	AM6442	See Table 5-1, *Device Comparison*
		AM6441	
		AM6422	
		AM6421	
		AM6412	
		AM6411	
r	Device revision	A	Silicon Revision (SR) 1.0
		B	SR 2.0
Z	Device Speed Grades	S	See Table 7-1, *Speed Grade Maximum Frequency*
		K	
f	Features (see Table 5-1)	C	All PRU_ICSSG features are enabled except for industrial communication support. PRU_ICSSG industrial communication interfaces include Ethernet networking (MII/RGMII, MDIO), Sigma-Delta (SD) decimation, and three channel peripheral interface (EnDat 2.2 and BiSS)
		D	Features supported by C, plus PRU_ICSSG industrial communication is enabled
		E	Features supported by D, plus EtherCAT HW Accelerator and CAN-FD are enabled
		F	Features supported by E, plus Pre-integrated Stacks are enabled
Y	Functional Safety	G	Non-Functional Safety
		F	Functional Safety
y	Security	G	Non-Secure
		H	Secure
t	Temperature (1)	A	–40°C to 105°C - Extended Industrial (see Section 7.4, *Recommended Operating Conditions*)
		I	–40°C to 125°C - Automotive (see Section 7.4, *Recommended Operation Conditions*)
PPP	Package Designator	ALV	ALV FCBGA-N441 (17.2 mm × 17.2 mm) Package
Q1	Automotive Designator	Q1	Automotive Qualified (AEC - Q100)
		BLANK	Standard
XXXXXXX			Lot Trace Code (LTC)
YYY			Production Code; For TI use only
O			Pin one designator
G1			ECAT—Green package designator

(1) Applies to device max junction temperature.

Note

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

10.2 Tools and Software

The following Development Tools support development for TI's Embedded Processing platforms:

Development Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. The tool includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

SysConfig-PinMux Tool The SysConfig-PinMux Tool is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI Embedded Processor devices. The tool can be used to automatically calculate the optimal pinmux configuration to satisfy entered system requirements. The tool generates output C header/code files that can be imported into software development kits (SDKs) and used to configure customer's software to meet custom hardware requirements. The **Cloud-based SysConfig-PinMux Tool** is also available.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

10.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the AM64x devices.

Technical Reference Manual

AM64x/AM243x Processors Silicon Revision 1.0 Technical Reference Manual Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM64x family of devices.

Errata

AM64x/AM243x Processors Silicon Revision 1.0 Silicon Errata Describes the known exceptions to the functional specifications for the device.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM6411BKCGHAALV	ACTIVE	FCBGA	ALV	441	84	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6411B KCGHAALV 709	Samples
AM6411BSCGHAALV	ACTIVE	FCBGA	ALV	441	84	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6411B SCGHAALV 709	Samples
AM6412BKCGHAALVR	ACTIVE	FCBGA	ALV	441	500	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6412B KCGHAALV 709	Samples
AM6412BSCGHAALV	ACTIVE	FCBGA	ALV	441	84	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6412B SCGHAALV 709	Samples
AM6421BSDGHAALVR	ACTIVE	FCBGA	ALV	441	500	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6421B SDGHAALV 709	Samples
AM6421BSEFHAALVR	ACTIVE	FCBGA	ALV	441	500	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6421B SEFHAALV 709	Samples
AM6421BSFFHAALV	ACTIVE	FCBGA	ALV	441	84	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6421B SFFHAALV 709	Samples
AM6421BSFGHAALV	ACTIVE	FCBGA	ALV	441	84	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6421B SFGHAALV 709	Samples
AM6422BSDFHAALVR	ACTIVE	FCBGA	ALV	441	500	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6422B SDFHAALV 709	Samples
AM6422BSDGHAALV	ACTIVE	FCBGA	ALV	441	84	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6422B SDGHAALV 709	Samples
AM6441BSEFHAALV	ACTIVE	FCBGA	ALV	441	84	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6441B SEFHAALV 709	Samples
AM6441BSEGHAALVR	ACTIVE	FCBGA	ALV	441	500	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6441B SEGHAALV	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										709	
AM6441BSFFHAALV	ACTIVE	FCBGA	ALV	441	84	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6441B SFFHAALV 709	Samples
AM6442BSDGHAALV	ACTIVE	FCBGA	ALV	441	84	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6442B SDGHAALV 709	Samples
AM6442BSEFHAALV	ACTIVE	FCBGA	ALV	441	84	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6442B SEFHAALV 709	Samples
AM6442BSEGHAALV	ACTIVE	FCBGA	ALV	441	84	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6442B SEGHAALV 709	Samples
AM6442BSFFHAALV	ACTIVE	FCBGA	ALV	441	84	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6442B SFFHAALV 709	Samples
AM6442BSFGHAALV	ACTIVE	FCBGA	ALV	441	84	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6442B SFGHAALV 709	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

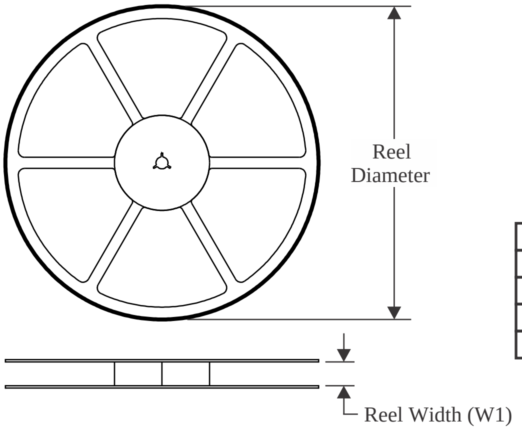
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

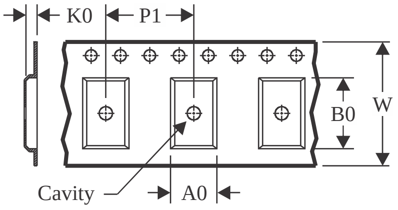
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

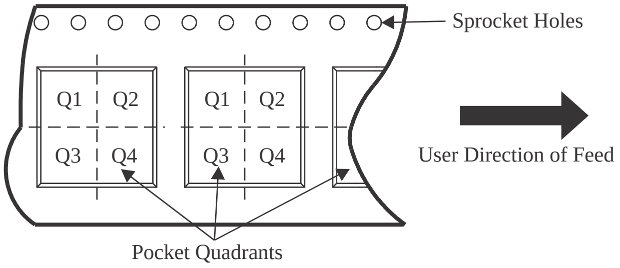


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

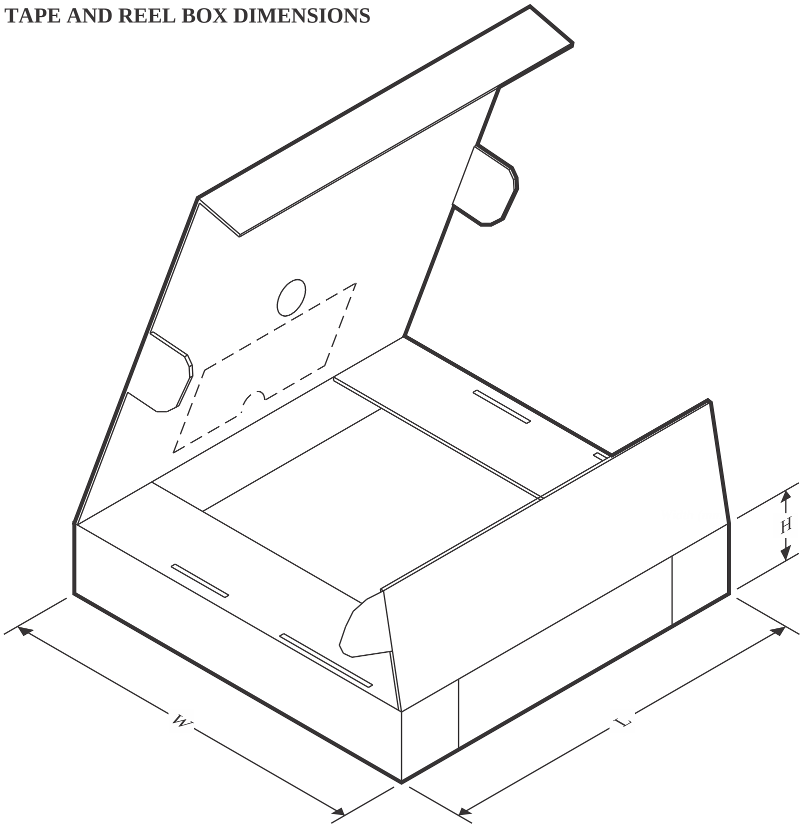
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM6412BKCGHAALVR	FCBGA	ALV	441	500	330.0	32.4	17.6	17.6	3.74	24.0	32.0	Q1
AM6421BSDGHAALVR	FCBGA	ALV	441	500	330.0	32.4	17.6	17.6	3.74	24.0	32.0	Q1
AM6421BSEFHAALVR	FCBGA	ALV	441	500	330.0	32.4	17.6	17.6	3.74	24.0	32.0	Q1
AM6422BSDFHAALVR	FCBGA	ALV	441	500	330.0	32.4	17.6	17.6	3.74	24.0	32.0	Q1
AM6441BSEGHAALVR	FCBGA	ALV	441	500	330.0	32.4	17.6	17.6	3.74	24.0	32.0	Q1

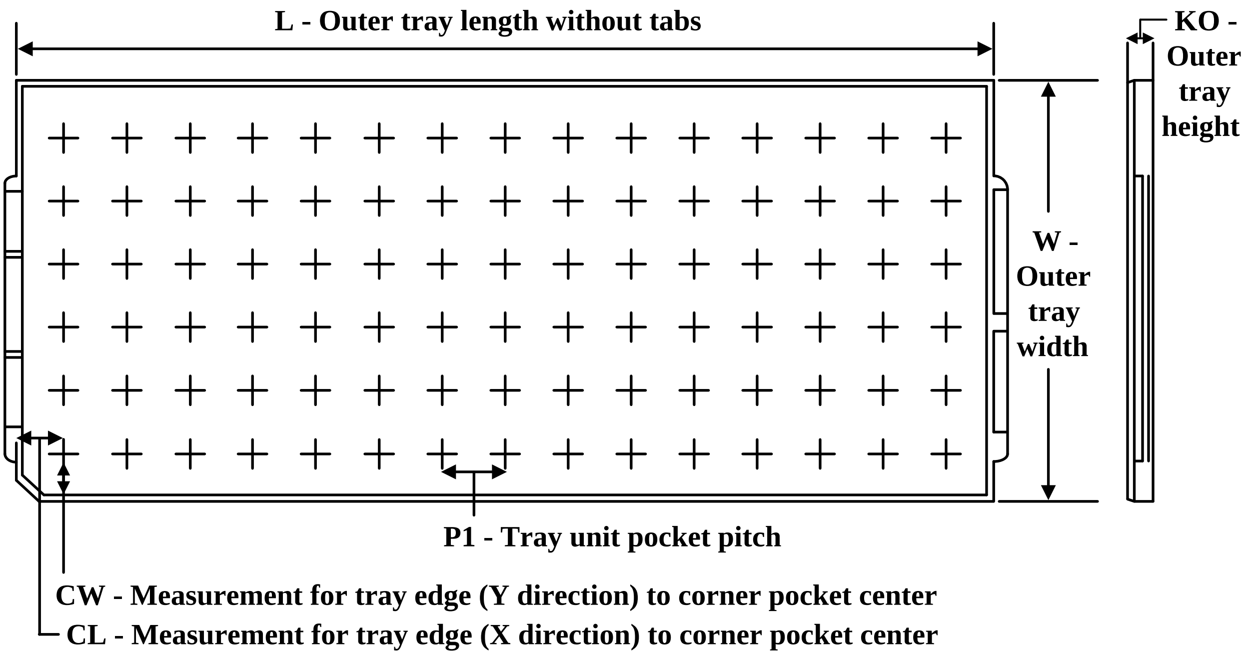
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM6412BKCGHAALVR	FCBGA	ALV	441	500	336.6	336.6	41.3
AM6421BSDGHAALVR	FCBGA	ALV	441	500	336.6	336.6	41.3
AM6421BSEFHAALVR	FCBGA	ALV	441	500	336.6	336.6	41.3
AM6422BSDFHAALVR	FCBGA	ALV	441	500	336.6	336.6	41.3
AM6441BSEGHAALVR	FCBGA	ALV	441	500	336.6	336.6	41.3

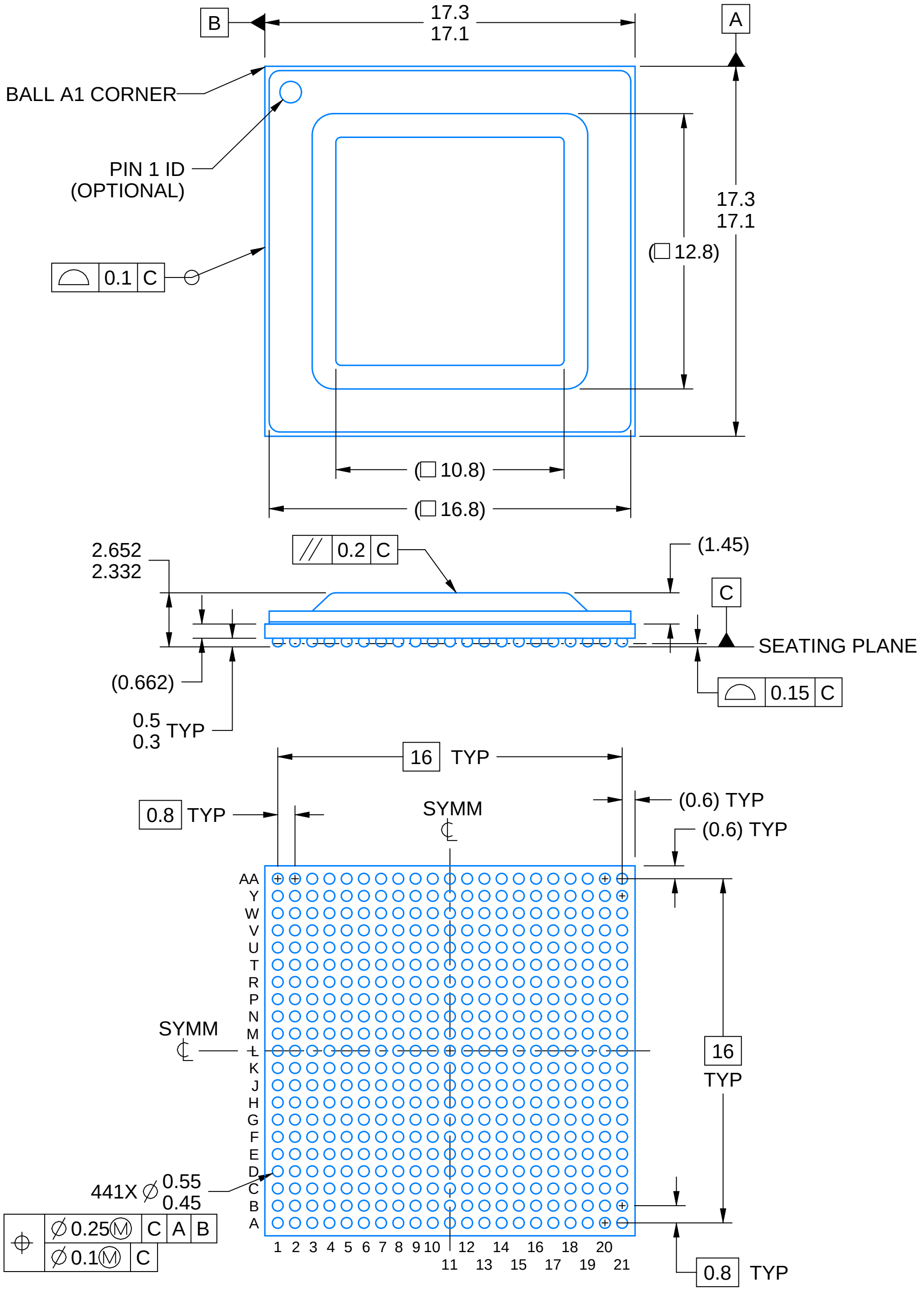
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AM6411BKCGHAALV	ALV	FCBGA	441	84	6 x 14	150	315	135.9	7620	22	14.5	14.55
AM6411BSCGHAALV	ALV	FCBGA	441	84	6 x 14	150	315	135.9	7620	22	14.5	14.55
AM6412BSCGHAALV	ALV	FCBGA	441	84	6 x 14	150	315	135.9	7620	22	14.5	14.55
AM6421BSFFHAALV	ALV	FCBGA	441	84	6 x 14	150	315	135.9	7620	22	14.5	14.55
AM6421BSFGHAALV	ALV	FCBGA	441	84	6 x 14	150	315	135.9	7620	22	14.5	14.55
AM6422BSDGHAALV	ALV	FCBGA	441	84	6 x 14	150	315	135.9	7620	22	14.5	14.55
AM6441BSEFHAALV	ALV	FCBGA	441	84	6 x 14	150	315	135.9	7620	22	14.5	14.55
AM6441BSFFHAALV	ALV	FCBGA	441	84	6 x 14	150	315	135.9	7620	22	14.5	14.55
AM6442BSDGHAALV	ALV	FCBGA	441	84	6 x 14	150	315	135.9	7620	22	14.5	14.55
AM6442BSEFHAALV	ALV	FCBGA	441	84	6 x 14	150	315	135.9	7620	22	14.5	14.55
AM6442BSEGHAALV	ALV	FCBGA	441	84	6 x 14	150	315	135.9	7620	22	14.5	14.55
AM6442BSFFHAALV	ALV	FCBGA	441	84	6 x 14	150	315	135.9	7620	22	14.5	14.55
AM6442BSFGHAALV	ALV	FCBGA	441	84	6 x 14	150	315	135.9	7620	22	14.5	14.55

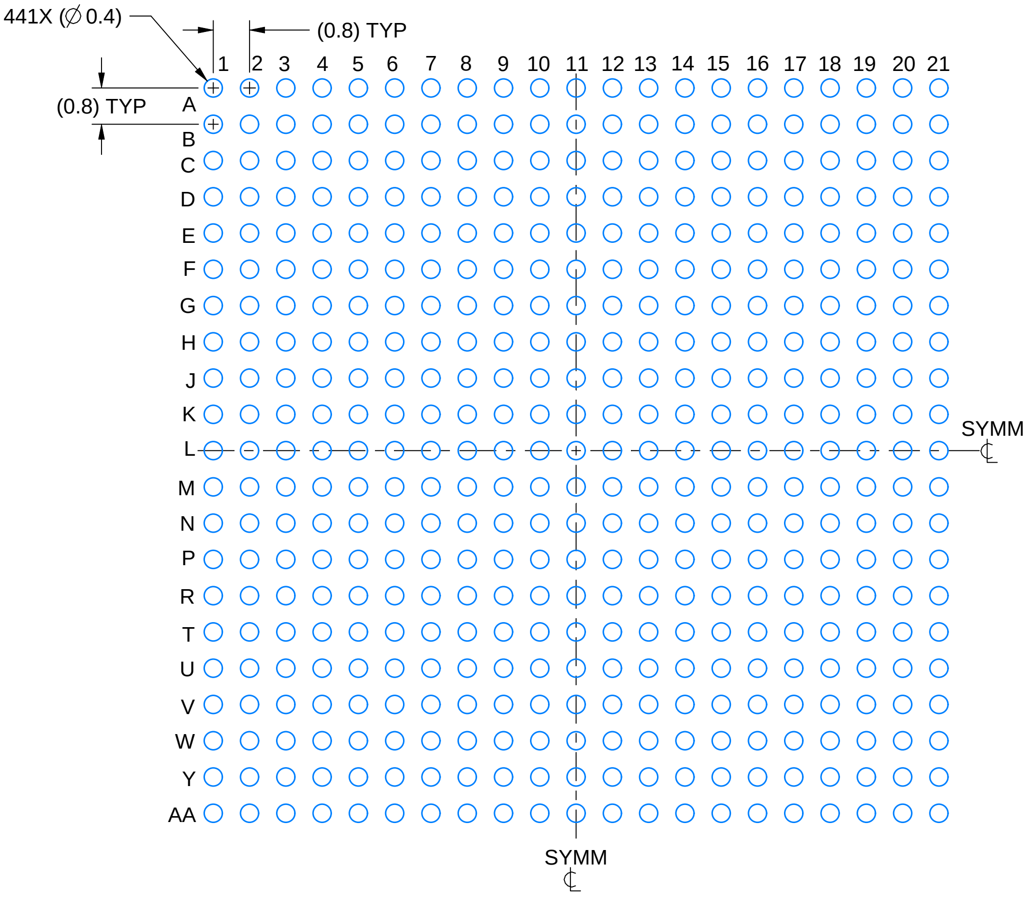


4225999/A 06/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SNOWN
SCALE:6X

NON-SOLDER MASK
DEFINED
(PREFERRED)

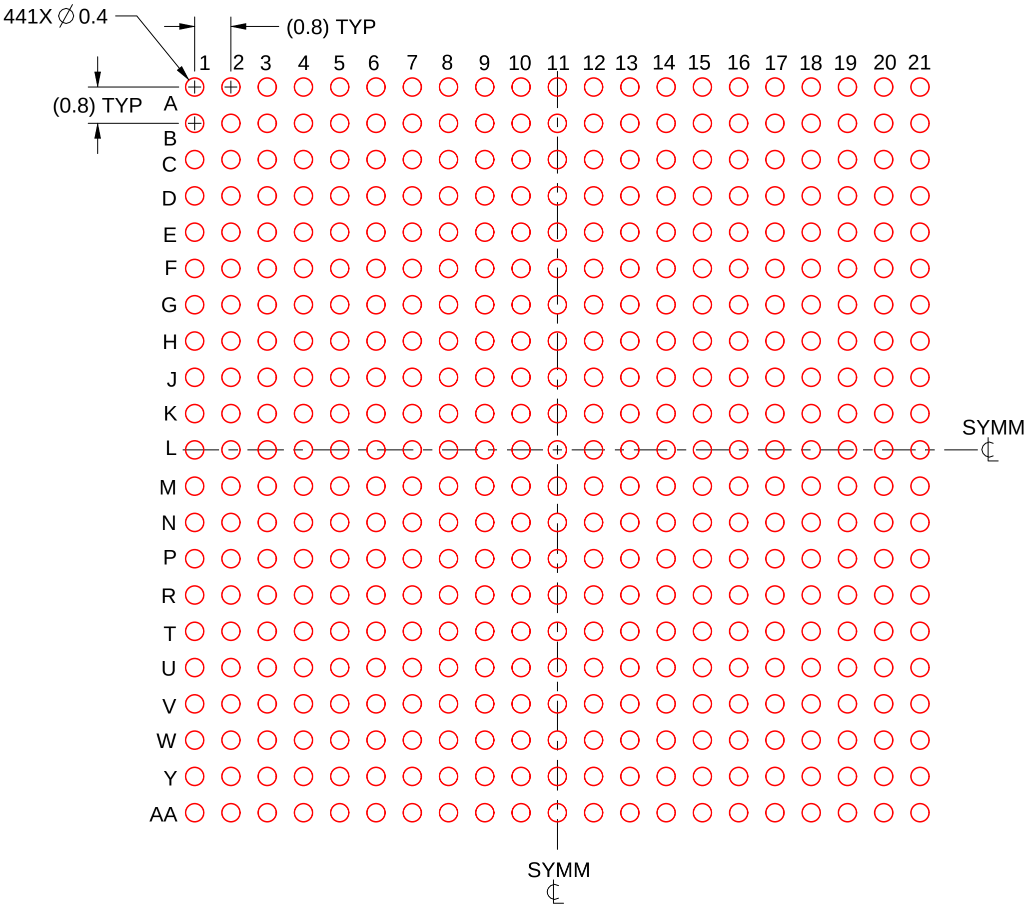
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4225999/A 06/2020

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE: 6X

4225999/A 06/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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