

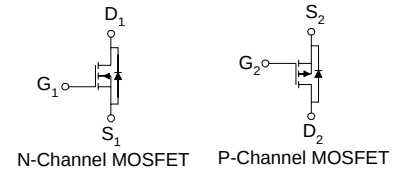
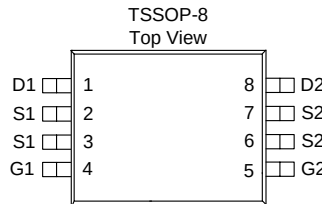
P & N-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	32 @ $V_{GS} = 10V$	4.3
	46 @ $V_{GS} = 4.5V$	3.7
-30	52 @ $V_{GS} = -10V$	-3.8
	80 @ $V_{GS} = -4.5V$	-2.8

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSSOP-8 saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	± 20	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	4.3	-3.8	A
	$T_A = 70^\circ\text{C}$		3.5	-3.0	
Pulsed Drain Current ^b		I_{DM}	20	-20	
Continuous Source Current (Diode Conduction) ^a		I_S	1.0	-1.0	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	1.14	1.14	W
	$T_A = 70^\circ\text{C}$		0.73	0.73	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typ	Max	
Maximum Junction-to-Ambient ^a	$t \leq 10 \text{ sec}$	R_{thJA}	88	110	$^\circ\text{C/W}$
	Steady State		120	150	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25° C UNLESS OTHERWISE NOTED)								
Parameter	Symbol	Test Conditions	Limits				Unit	
			Ch	Min	Typ	Max		
Static								
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 uA	N	1.0			V	
		V _{GS} = V _{DS} , I _D = -250 uA	P	-1.0				
Gate-Body Leakage	I _{GSS}	V _{GS} = 20 V, V _{DS} = 0 V	N			±100	nA	
		V _{GS} = -20 V, V _{DS} = 0 V	P			±100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V	N			1	uA	
		V _{DS} = -16 V, V _{GS} = 0 V	P			-1		
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N	20			A	
		V _{DS} = -5 V, V _{GS} = -10 V	P	-20				
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.3 A	N			32	mΩ	
		V _{GS} = 4.5 V, I _D = 3.7 A				46		
		V _{GS} = -10 V, I _D = -3.8 A	P			52		
		V _{GS} = -4.5 V, I _D = -2.8 A				80		
Forward Tranconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 4.3 A	N		11		S	
		V _{DS} = -15 V, I _D = -3.8 A	P		11			
Dynamic								
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, V _{GS} =4.5V, I _D =4.3A P-Channel V _{DS} =-15V, V _{GS} =-4.5V, I _D =-3.8A	N		4.7		nC	
Gate-Source Charge	Q _{gs}		P		8.0			
		Gate-Drain Charge	Q _{gd}	N		1.8		
P				2.3				
Turn-On Delay Time	t _{d(on)}	N-Chaneeel V _{DD} =15V, V _{GS} =4.5V, I _D =1A , R _{GEN} =6Ω, P-Channel V _{DD} =-15V, V _{GS} =-4.5V, I _D =-1A R _{GEN} =6Ω	N		13		nS	
			P		14			
Rise Time	t _r		N		14			
			P		14			
Turn-Off Delay Time	t _{d(off)}		N		30			
			P		40			
Fall-Time	t _f		N		30			
			P		30			

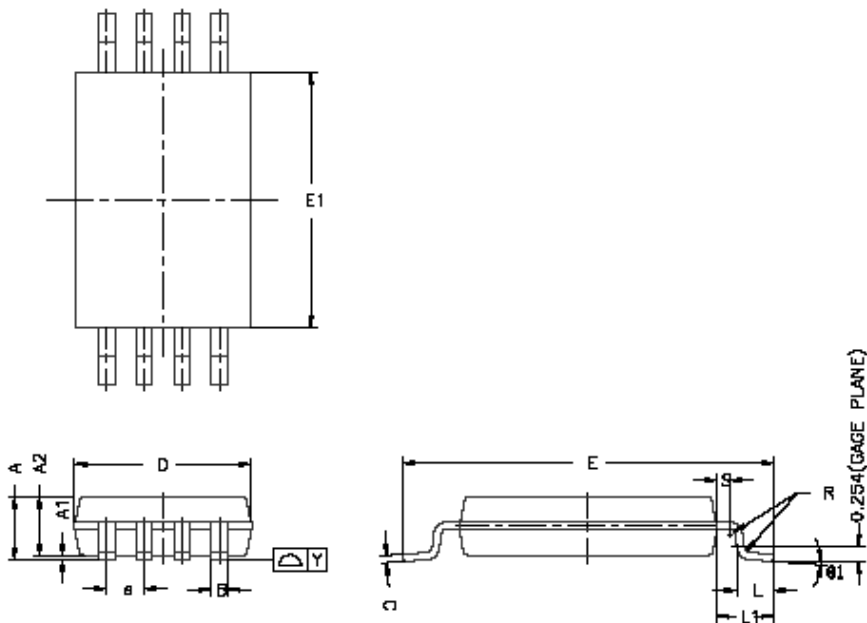
Notes

- Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

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Package Information

TSSOP-8: 8LEAD



DIM.	MILLIMETERS		
	MIN.	NDM.	MAX.
A	1.05	1.10	1.20
A(1)	0.05	0.10	0.15
A(2)	0.99	1.02	1.05
B	0.19	0.25	0.30
C	---	0.127	---
D	2.90	3.00	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
a	0.635SC		
L	0.45	0.60	0.75
L1	0.90	1.00	1.10
Y	---	---	0.10
Ø1	Ø	Ø	Ø
R	0.09	---	---
S	0.20	---	---