Final

Am685

Voltage Comparator

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

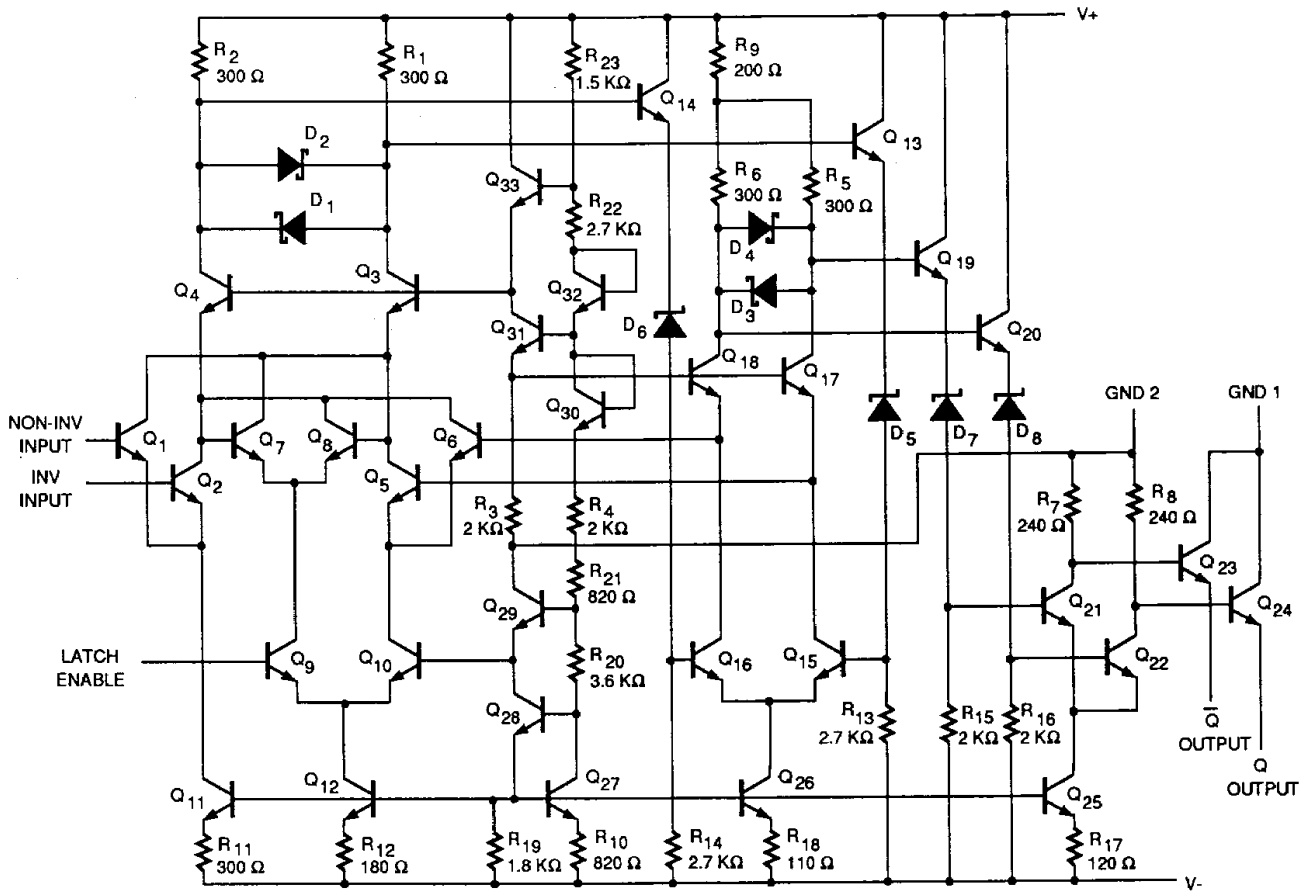
- 6.5 ns Maximum Propagation Delay at 5 mV Overdrive
- 3.0 ns Latch Setup Time
- Complementary ECL Outputs
- 50 Ω Line Driving Capability

GENERAL DESCRIPTION

The Am685 is a fast voltage comparator manufactured with an advanced bipolar-NPN, Schottky-diode high-frequency process that ensures very short propagation delays (6.5 ns) without sacrificing the excellent matching characteristics hitherto associated only with slow, high-performance linear ICs. The circuit has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output-current capability is adequate for driving terminated 50 Ω transmission lines. The low input offset and high resolution make this comparator especially suitable for high-speed precision analog-to-digital processing.

A latch function is provided so that the comparator can be used in a sample-hold mode. If the Latch Enable input is HIGH, the comparator functions normally. If the Latch Enable is driven LOW, the comparator outputs are locked in their existing logic states. If the latch function is not used, the Latch Enable must be connected to ground.

CIRCUIT DIAGRAM



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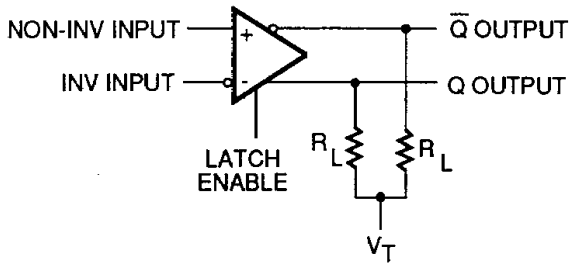
FUNCTIONAL DIAGRAM



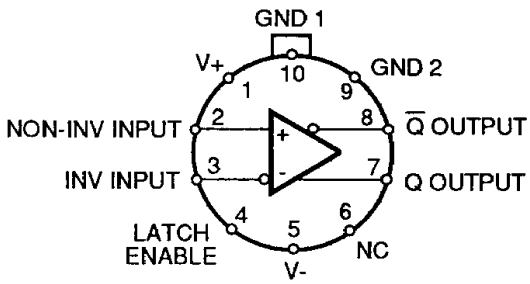
03937C-001

The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50-200 Ω connected to -2.0 V, or 200-2000 Ω connected to -5.2 V.

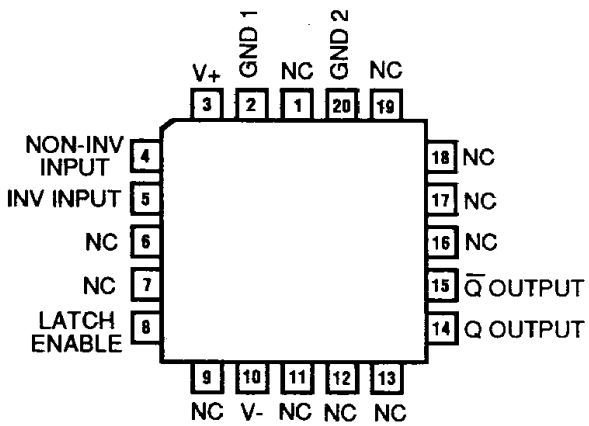
03937-001

CONNECTION DIAGRAMS
Top View

Metal Can
H-10-1

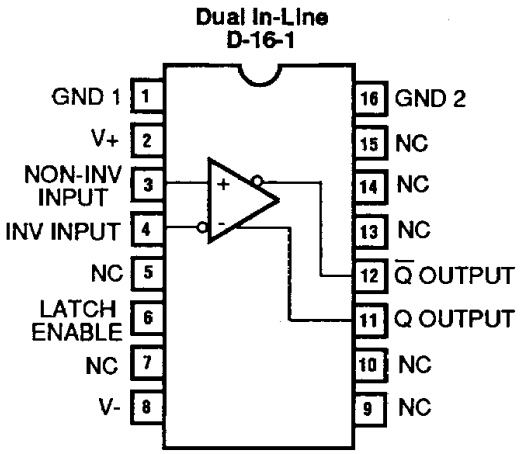


Leadless Chip-Pak
L-20-1



Note 1 On metal package, pin 5 is connected to case.
On DIP, pin 8 is connected to case.

Dual In-Line
D-16-1



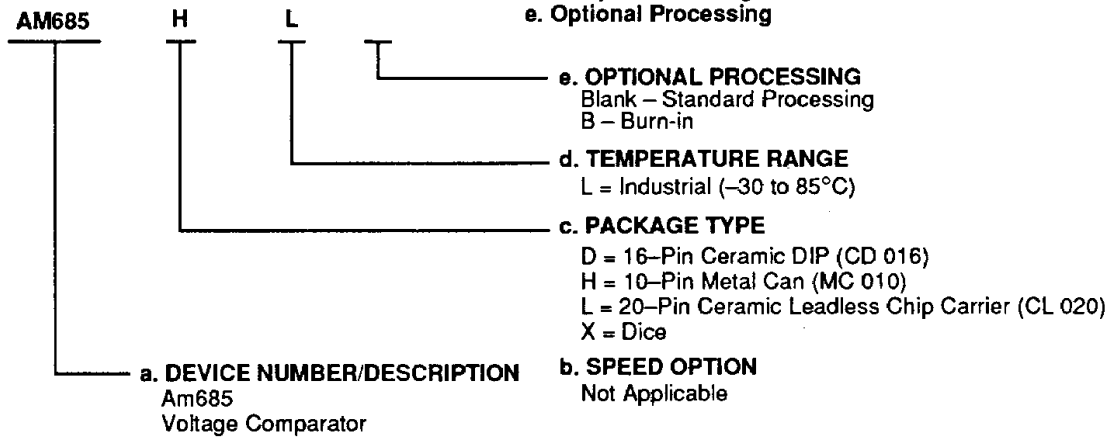
03937-003

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM685	HL, DL, LMB, XL, XM

Valid Combinations

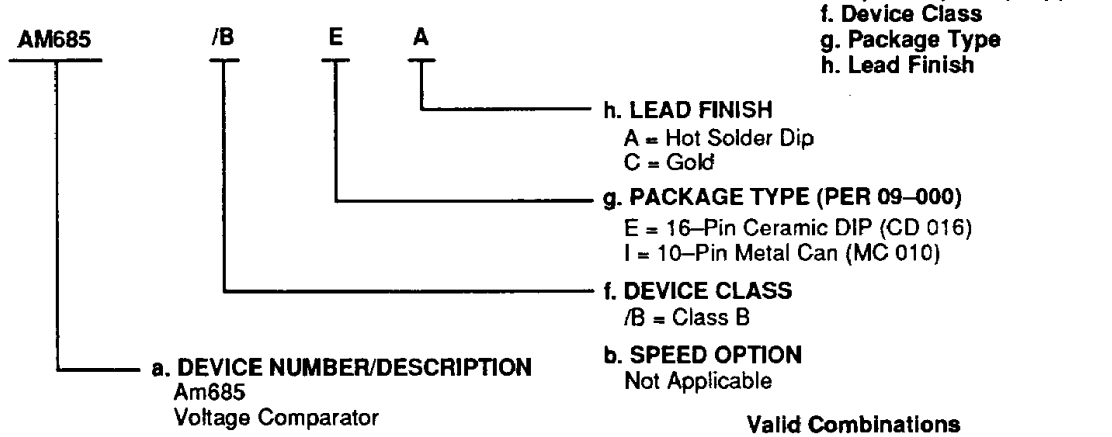
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List products are fully compliant with MIL–M–38510 and MIL–STD–883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
f. Device Class
g. Package Type
h. Lead Finish



Valid Combinations	
AM685	/BEA /BIC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

Group A Tests

Group A Tests consist of sub-groups 1, 2, 3, 4, 5, 6, 9

MAXIMUM RATINGS

Positive Supply Voltage	+7 V
Negative Supply Voltage	–7 V
Input Voltage	±4 V
Differential Input Voltage	±6 V
Minimum Operating Voltage (V+ to V–)	9.7 V
Output Current	30 mA
Power Dissipation (Note 2)	500 mW
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

** To duplicate high power steady state operation, parts are pulse tested at these correlated temperatures: 685 L = –10°C to +105°C, 685 M = –35C to +145°C*

Operating Temperature Range

Am685–L*	–30°C to +85°C
Am685–M*	–55°C to +125°C
Die Size	.032" x .054"

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Over the operating temperature ranges (unless otherwise specified)

DC Characteristics (Included in Group A, Subgroup 1,2,3,4,5,6, unless noted)

Parameter Symbol	Parameter Description	Test Conditions	Am685–L		Am685–M		Unit
			Min.	Max.	Min.	Max.	
V_{OS}	Input Offset Voltage	R_S = 100 Ω, T_A = 25°C R_S = 100 Ω	–2.0 –2.5	+2.0 +2.5	–2.0 –3.0	+2.0 +3.0	mV mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	R_S = 100 Ω (Note 6)	–10	+10	–10	+10	µV/°C
I_{OS}	Input Offset Current	T_A = 25°C	–1.0 –1.3	+1.0 +1.3	–1.0 –1.6	+1.0 +1.6	µA µA
I_B	Input Bias Current	T_A = 25°C		10 13		10 16	µA µA
R_{IN}	Input Resistance	T_A = 25°C (Note 5)	6.0		6.0		kΩ
C_{IN}	Input Capacitance (Note 1)	T_A = 25°C		3.0		3.0	pF
V_{CM}	Input Voltage Range		–3.3	+3.3	–3.3	+3.3	V
CMMR	Common Mode Rejection Ratio	R_S = 100 Ω, –3.3<V_{CM}<+3.3 V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	R_S = 100 Ω, ΔVs = ±5	60		60		dB
V_{OH}	Output HIGH Voltage	$T_A = T_{A(min)}$ $T_A = T_{A(max)}$ T_A = 25°C	–1.060 –0.890 –0.960	–0.890 –0.700 –0.810	–1.100 –0.850 –0.960	–0.920 –0.620 –0.810	V V V
V_{OL}	Output LOW Voltage	$T_A = T_{A(min)}$ $T_A = T_{A(max)}$ T_A = 25°C	–1.890 –1.825 –1.850	–1.675 –1.625 –1.650	–1.910 –1.810 –1.850	–1.690 –1.575 –1.650	V V V
I+	Positive Supply Current			22		22	m
I–	Negative Supply Current			26		26	mA
P_{DISS}	Power Dissipation			300		300	mW

Switching Characteristics (V_{in} = 100 mV, V_{od} = 5 mV) Included in Group A subgroup unless noted.

Parameter Symbol	Parameter Description	Test Conditions	Am685–L		Am685–M		Unit
			Min.	Max.	Min.	Max.	
t_{pd+}	Input to Output HIGH (Note 6)	$T_{A(min)} < T_A < 25°C$ $T_A = T_{A(max)}$	4.5 5.0	6.5 9.5	4.5 5.5	6.5 12	ns ns
t_{pd-}	Input to Output LOW (Note 6)	$T_{A(min)} < T_A < 25°C$ $T_A = T_{A(max)}$	4.5 5.0	6.5 9.5	4.5 5.5	6.5 12	ns ns
t_{pd+} (E)	Latch Enable to Output HIGH (Note 4)	$T_{A(min)} < T_A < 25°C$ $T_A = T_{A(max)}$	4.5 5.0	6.5 9.5	4.5 5.5	6.5 12	ns ns
t_{pd-} (E)	Latch Enable to Output LOW (Note 4)	$T_{A(min)} < T_A < 25°C$ $T_A = T_{A(max)}$	4.5 5.0	6.5 9.5	4.5 5.5	6.5 12	ns ns
t_s	Minimum Set–up Time (Note 4)	$T_{A(min)} < T_A < 25°C$ $T_A = T_{A(max)}$		3.0 4.0		3.0 6.0	ns ns
t_h	Minimum Hold Time (Note 4)	$T_{A(min)} < T_A < T_{A(max)}$		1.0		1.0	ns
t_{pw} (E)	Minimum Latch Enable Pulse Width (Note 4)	$T_{A(min)} < T_A < 25°C$ $T_A = T_{A(max)}$		3.0 4.0		3.0 5.0	ns ns

Notes:

1) For MC only; CERDIP = 7 pF.

2) For the metal can package, derate at 6.8 mW/°C for operation at ambient temperatures above +100°C; for the dual in-line package, derate at 9 mW/°C for operation at ambient temperatures above +105°C.

3) Unless otherwise specified V+ = 6.0 V, V⁻ = –5.2 V, V_T = –2.0 V, and R_L = 50 Ω; all switching characteristics are for a 100 mV input step with 5 mV overdrive. The specifications given for V_{OS}, I_{OS}, I_B, CMMR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5 supply voltages. The Am685 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

4) Owing to the difficult and critical nature of switching measurements involving the latch, these parameters cannot be tested in production. Engineering data indicates that at least 95% of the units will meet specifications given.

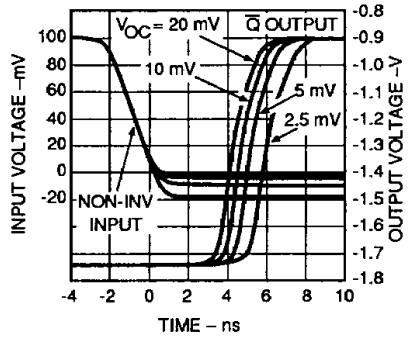
5) Guaranteed, not tested.

6) Not 100% tested. Group A only.

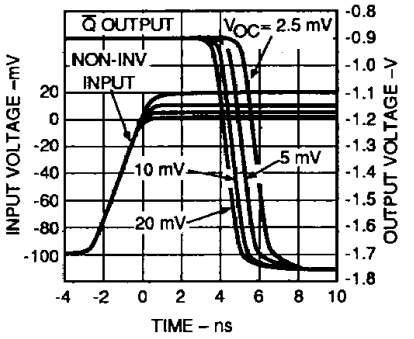
PERFORMANCE CURVES

(Unless otherwise specified, standard conditions for all curves are T_A = 25°C, V+ = 6.0 V, V- = -5.2 V, V_T = -2.0 V, R_L = 50Ω, and switching characteristics are for V_{IN} = 100 mV, V_{od} = 5 mV.)

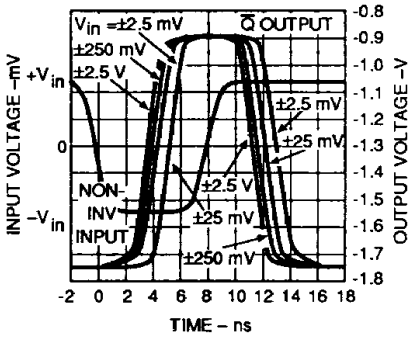
Response for Various Input Overdrives



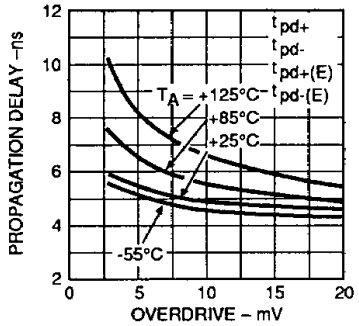
Response for Various Input Overdrives



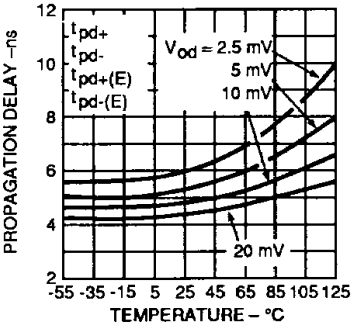
Response for Various Input Signal Levels



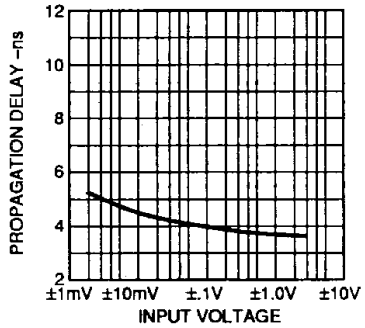
Propagation Delays as a Function of Input Overdrive



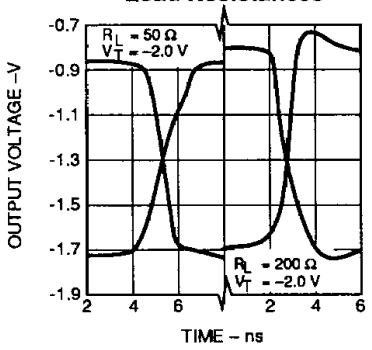
Propagation Delays as a Function of Temperature



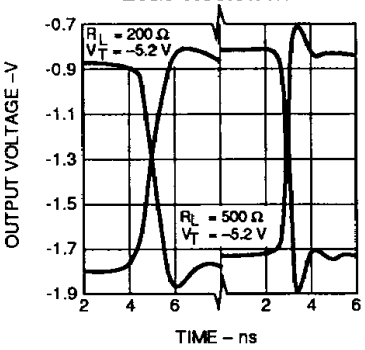
Propagation Delay as a Function of Input Signal Level



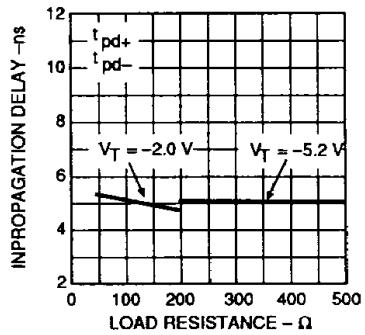
Response for Various Load Resistances



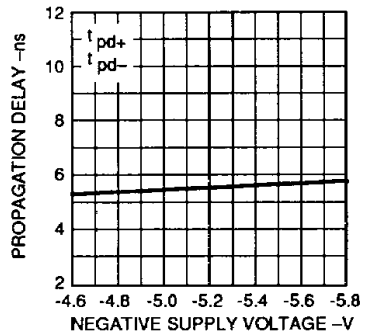
Response for Various Load Resistances



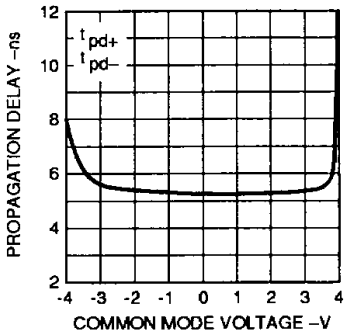
Propagation Delays as a Function of Load Resistance



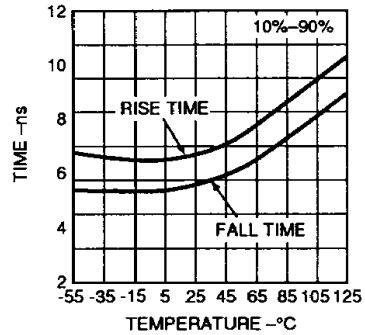
Propagation Delays as a Function of Negative Supply Voltage



Propagation Delays as a Function of Common Mode Voltage



Output Rise and Fall Times as a Function of Temperature



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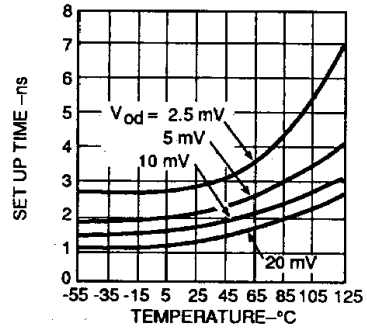
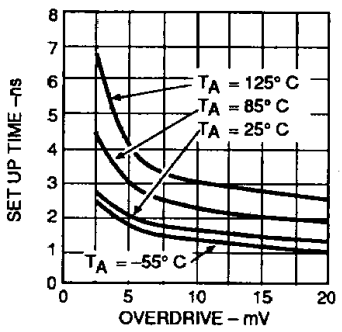
PERFORMANCE CURVES, (Continued)

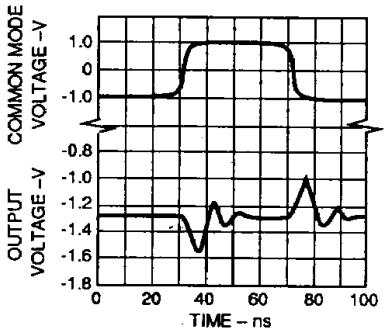
Set-up Time as a Function of Temperature



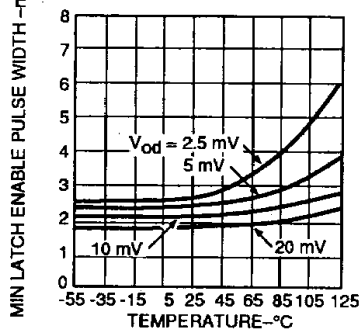
Set-up Time as a Function of Input Overdrive



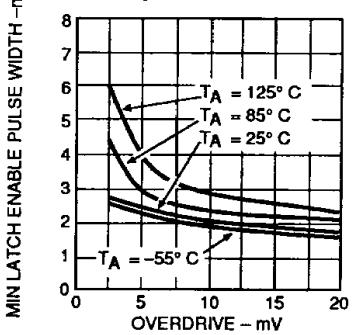
Common Mode Pulse Response



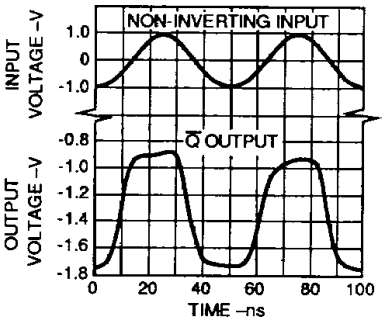
Min. Latch Enable Pulse Width as a Function of Temperature



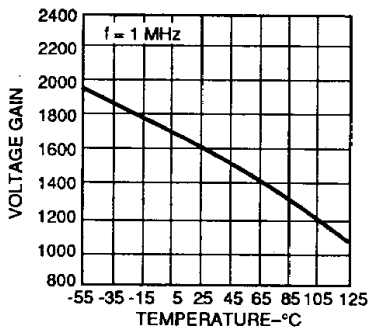
Min. Latch Enable Pulse Width as a Function of Input Overdrive



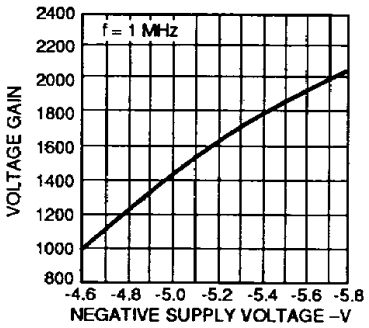
Response to 100 MHz Sine Wave



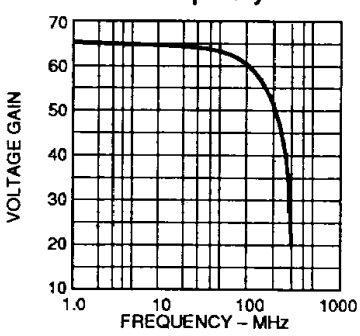
Voltage Gain as a Function of Temperature



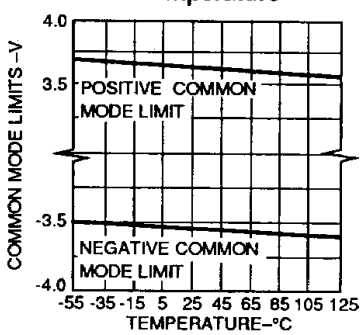
Voltage Gain as a Function of Negative Supply Voltage



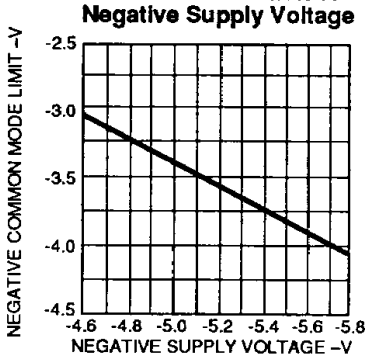
Voltage Gain as a Function of Frequency



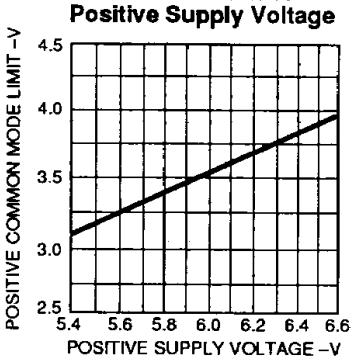
Common Mode Limits as a Function of Temperature



Negative Common Mode Limit as a Function of Negative Supply Voltage



Positive Common Mode Limit as a Function of Positive Supply Voltage



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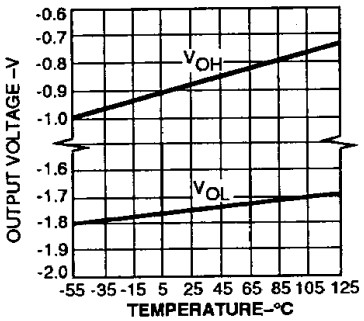
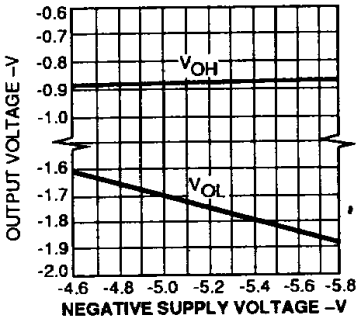
PERFORMANCE CURVES, (Continued)

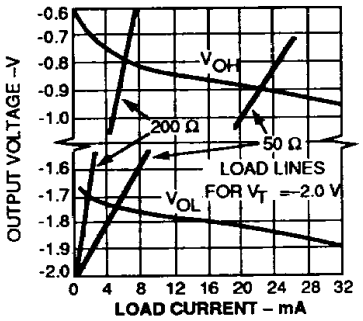
Output Levels as a Function of Temperature



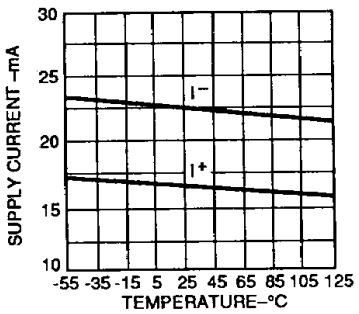
Output Levels as a Function of Negative Supply Voltage



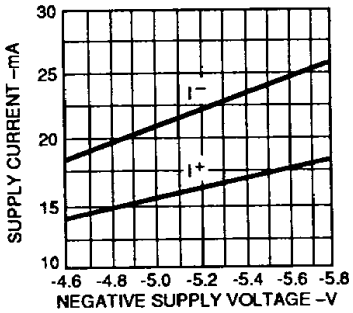
Output Levels as a Function of DC Loading



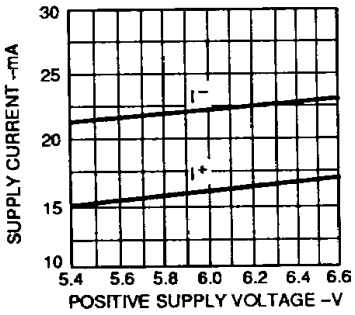
Supply Currents as a Function of Temperature



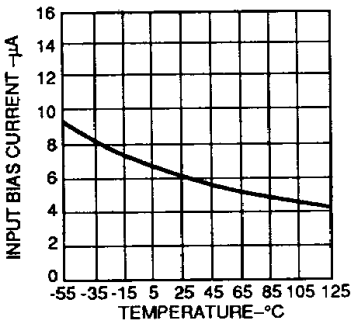
Supply Currents as a Function of Negative Supply Voltage



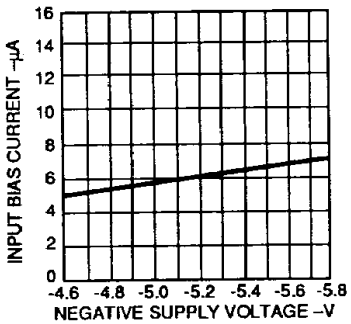
Supply Currents as a Function of Positive Supply Voltage



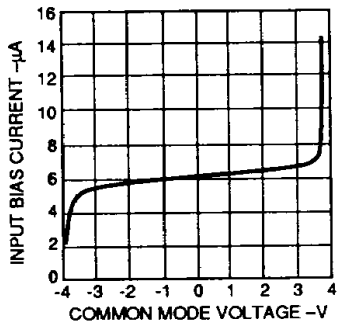
Input Bias Current as a Function of Temperature



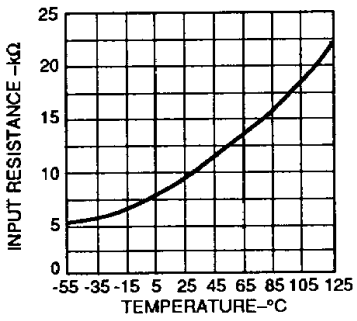
Input Bias Current as a Function of Negative Supply Voltage



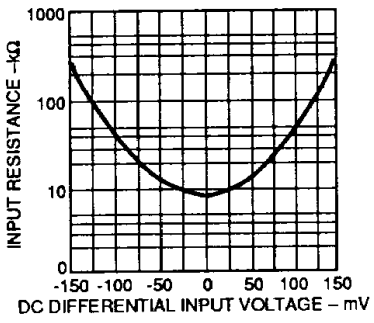
Input Bias Current as a Function of Common Mode Voltage



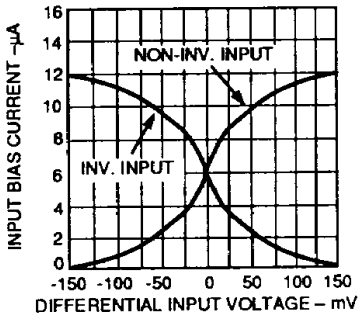
Input Resistance as a Function of Temperature



Input Resistance as a Function of DC Differential Input Voltage



Input Current as a Function of Differential Input Voltage



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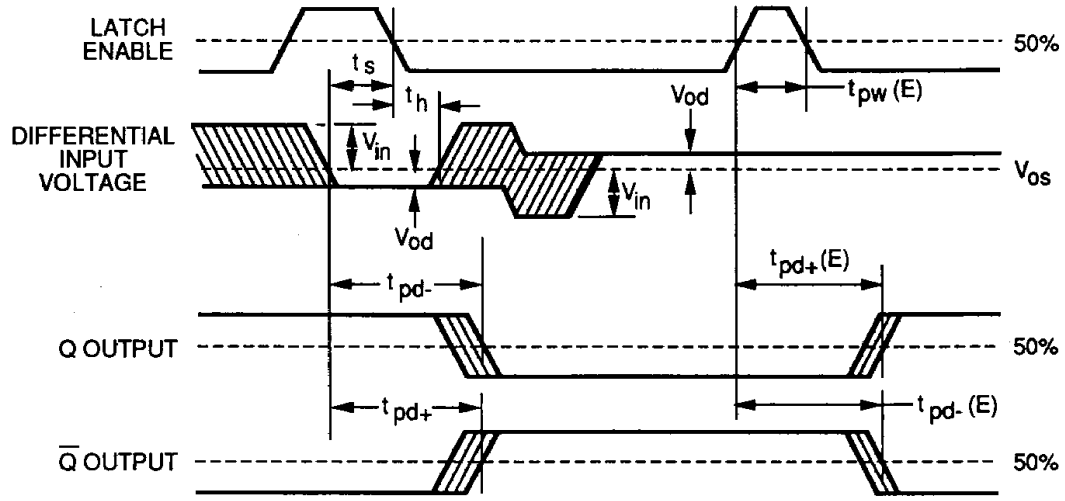
TIMING DIAGRAMS



WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▩	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN

03937-008

Figure 1.

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_s will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may or may not be detected.

DEFINITION OF TERMS

V_{OS} **INPUT OFFSET VOLTAGE** — That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.

$\Delta V_{OS}/\Delta T$ **AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE** — The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

I_{OS} **INPUT OFFSET CURRENT** — The difference between the currents into the two input terminals when there is zero voltage between the two outputs.

I_B **INPUT BIAS CURRENT** — The average of the two input currents.

R_{IN} **INPUT RESISTANCE** — The resistance looking into either input terminal with the other grounded.

C_{IN} **INPUT CAPACITANCE** — The capacitance looking into either input terminal with the other grounded.

V_{CM} **INPUT VOLTAGE RANGE** — The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

CMRR **COMMON MODE REJECTION RATIO** — The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

SVRR **SUPPLY VOLTAGE REJECTION RATIO** — The ratio of the change in input offset voltage to the change in power supply voltages producing it.

V_{OH} **OUTPUT HIGH VOLTAGE** — The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} **OUTPUT LOW VOLTAGE** — The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

I_+ **POSITIVE SUPPLY CURRENT** — The current required from the positive supply to operate the comparator.

I_- **NEGATIVE SUPPLY CURRENT** — The current required from the negative supply to operate the comparator.

P_{DISS} **POWER DISSIPATION** — The power dissipated by the comparator with both outputs terminated in 50 Ω to –2.0 V.

Switching Terms (refer to Figure 1)

t_{pd+} **INPUT TO OUTPUT HIGH DELAY** — The propagation delay measured from the time the input signal crosses the input offset voltage to the 50 point of an output LOW to HIGH transition.

t_{pd-} **INPUT TO OUTPUT LOW DELAY** — The propagation delay measured from the time the input signal crosses the input offset voltage to the 50 point of an output HIGH to LOW transition.

$t_{pd+}(E)$ **LATCH ENABLE TO OUTPUT HIGH DELAY** — The propagation delay measured from the 50 point of the Latch Enable signal LOW to HIGH transition to the 50 point of an output LOW to HIGH transition.

$t_{pd-}(E)$ **LATCH ENABLE TO OUTPUT LOW DELAY** — The propagation delay measured from the 50 point of the Latch Enable signal LOW to HIGH transition to the 50 point of an output HIGH to LOW transition.

t_s **MINIMUM SET-UP TIME** — The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h **MINIMUM HOLD TIME** — The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw}(E)$ **MINIMUM LATCH ENABLE PULSE WIDTH** — The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

Other Symbols

T_A **Ambient temperature**

R_S **Input source resistance**

V_S **Supply voltages**

$V+$ **Positive supply voltage**

$V-$ **Negative supply voltage**

V_T **Output load terminating voltage**

R_L **Output load resistance**

V_{in} **Input pulse amplitude**

V_{od} **Input overdrive**

f **Frequency**

Measurement Of Propagation Delay

A voltage comparator must be able to respond to input signal levels ranging from a few millivolts to several volts, ideally with little variation in propagation delay. The most difficult condition is where the comparator has been driven hard into one state by a large signal, and the next input signal is just barely enough to make it switch to the other state. This forces the input stage of the circuit to swing from a full off (or on) state to a point somewhere near the center of its linear range, thus exercising both its large and small signal responses. If the comparator is fast for this condition, it should be as fast or faster for almost any other condition. The unofficial industry standard input signal is a 100 mV step with an overdrive of 5 mV (the overdrive is the voltage in excess of that needed to bring the output to the center of its dynamic range). The 100 mV is more than enough to fully turn on the input stage, but not so large to make measurement a problem. Large pulses would require exceptionally good control on waveform purity, since only a few tenths of a percent of overshoot or ripple would be enough to affect the value of the overdrive and, for sensitive comparators, result in false switching. The propagation delay is measured from the time the input signal crosses the input threshold voltage (i.e., the offset voltage) to the 50 point of either output. This definition ensures that each unit is measured under equal conditions, and also makes the measurement relatively independent of the input rise and fall times.

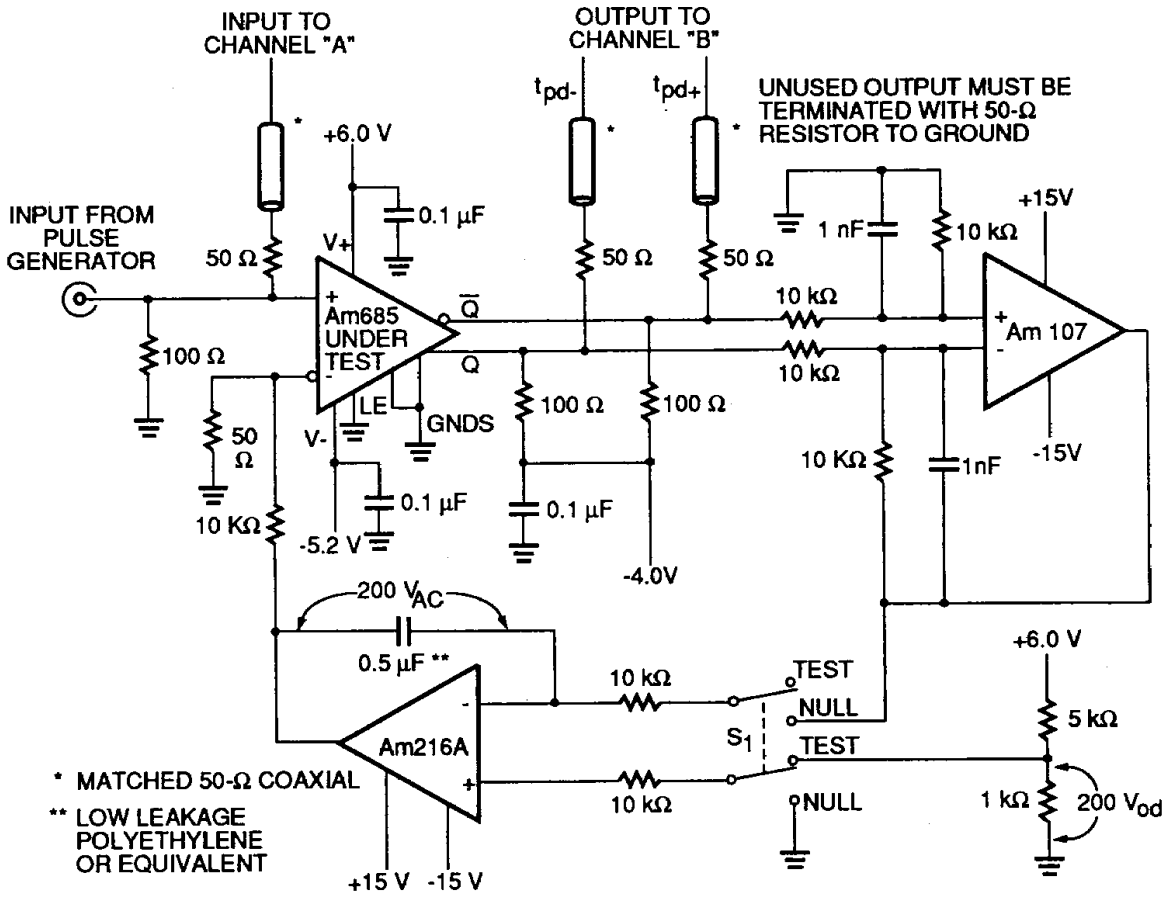
The test circuit of Figure 2 provides a means of automatically nulling out the offset voltage and applying the overdrive. With S1 in the "NULL" position, the feedback loop around the Am685 via the two operational amplifiers corrects for the offset of the circuit including any dc shift in the ground level of the input signal. When switched to "TEST", the offset is held on the storage capacitor of the Am216A and the overdrive is added at the Am216A non-inverting input. The duty cycle of the signal is made low so that the presence of the input pulse during nulling will not disturb the offset. A solid ground plane is used for the test jig, and capacitors bypass the supply voltages. All power and signal leads are kept as short as possible. The Am685 input and output run directly into the 50 Ω inputs of the sampling scope via equal lengths of 50 Ω coaxial cable. For the conditions shown in the figure, t_{pd_+} is measured at the $\overline{Q}$ output and t_{pd_-} at the Q output. If it is desired to measure to opposite output polarities, the polarities of the input signal and overdrive must be reversed.

Thermal Considerations

To achieve the high speed of the Am685, a certain amount of power must be dissipated as heat. This increases the temperature of the die relative to the ambient temperature. In order to be compatible with ECL III and ECL 10,000, which normally use air flow as a means of package cooling, the Am685 characteristics are specified when the device has an air flow across the package of 500 linear feet per minute or greater. Thus, even though different ECL circuits on a printed circuit board may have different power dissipations, all will have the same input and output levels, etc., provided each sees the same air flow and air temperature. This eases design, since the only change in characteristics between devices is due to the increase in ambient temperature of the air passing over the devices. If the Am685 is operated without air flow, the change in electrical characteristics due to the increased die temperature must be taken into account.

Interconnection Techniques

All high-speed ECL circuits require that special precautions be taken for optimum system performance. The Am685 is particularly critical because it features very high gain (60 dB) at very high frequencies (100 MHz). A ground plane must be provided for a good, low inductance, ground current return path. The impedance at the inputs should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch, since severe ringing occurs beyond this length. For longer lengths, the printed-circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150 Ω. Reflections will occur unless the line is terminated in its characteristic impedance. The termination resistors normally go to –2.0 V, but a Thevenin equivalent to V– can be used at some increase in power. Best results are usually obtained with the terminating resistor at the end of the driven line. The lower impedance lines are more suitable for driving capacitance loads. The supply voltages should be well decoupled with RF capacitors connected to the ground plane as close to the device supply pins as possible.



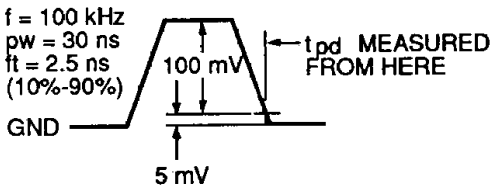


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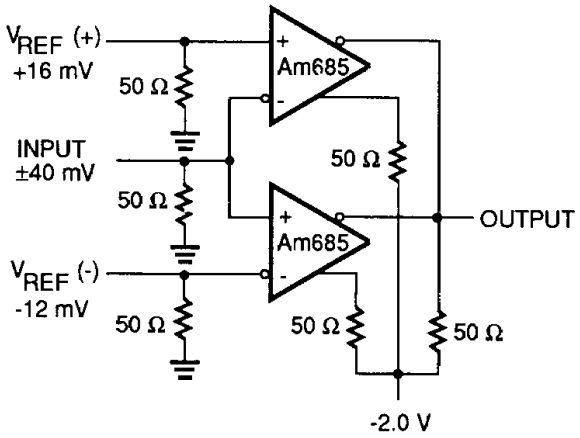
Figure 2.

TYPICAL APPLICATIONS



Typical Applications
High-Speed Window Detector

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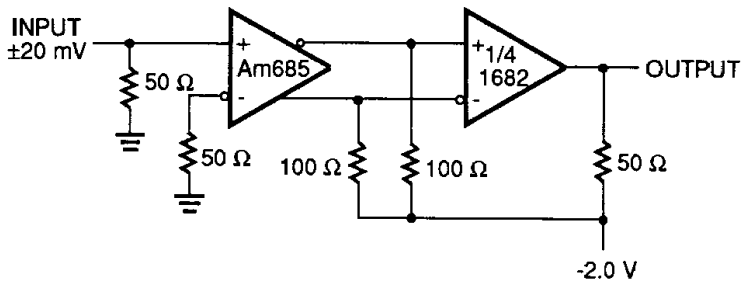
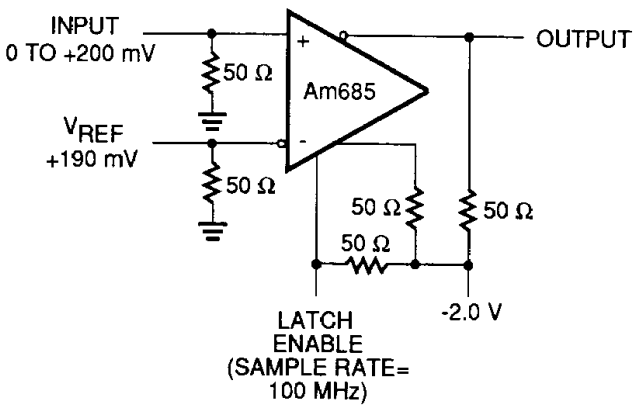


Typical Applications
300 MHz Line Receiver

03937–011

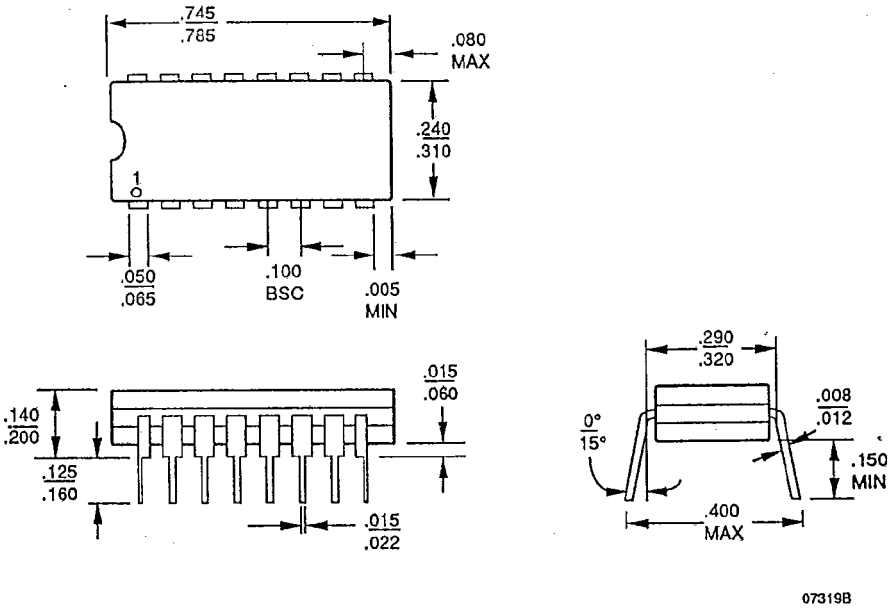


Typical Applications
High-Speed Sampling

03937–012

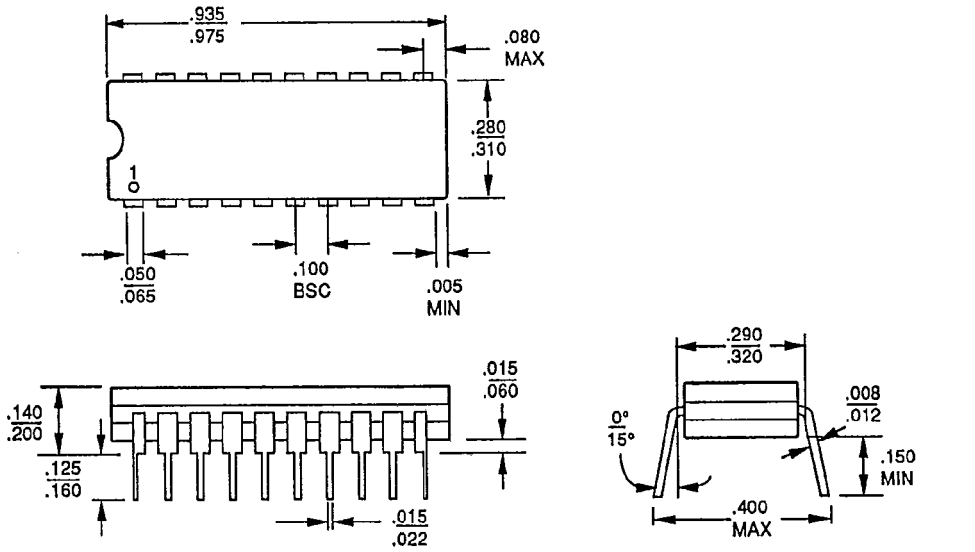
T-90-20

PHYSICAL DIMENSIONS
CD 016



07319B

CD 020



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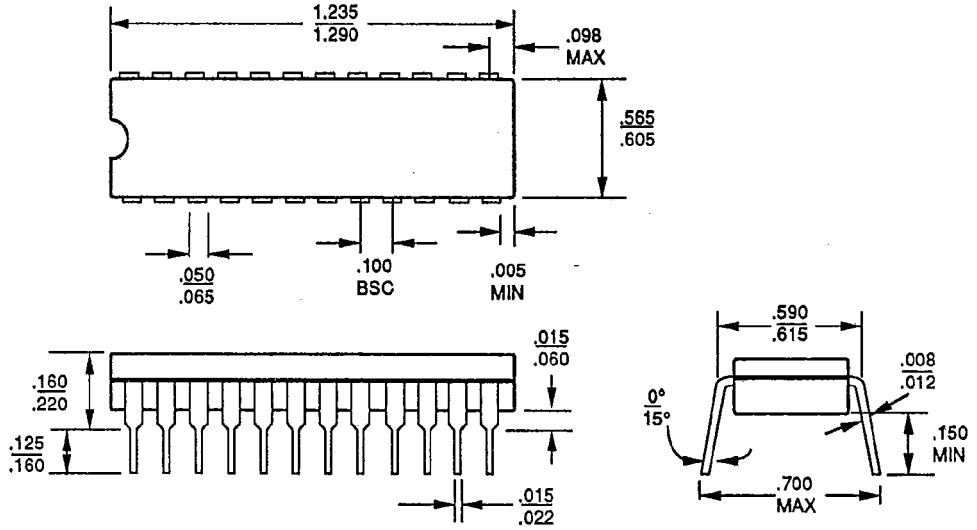
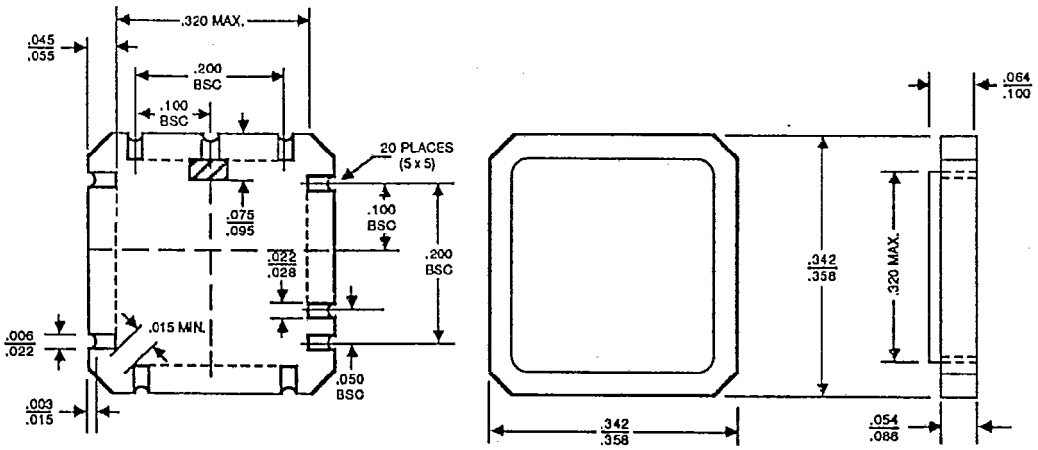
T-90-20

PHYSICAL DIMENSIONS (continued)
CD 024



03067-008A

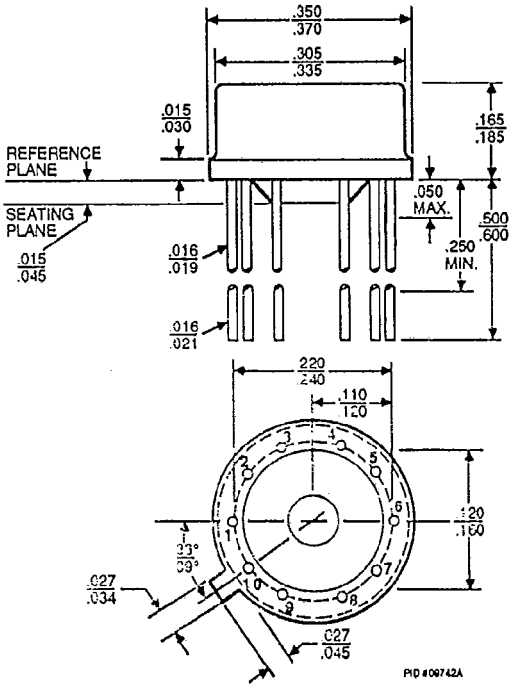
CL 020



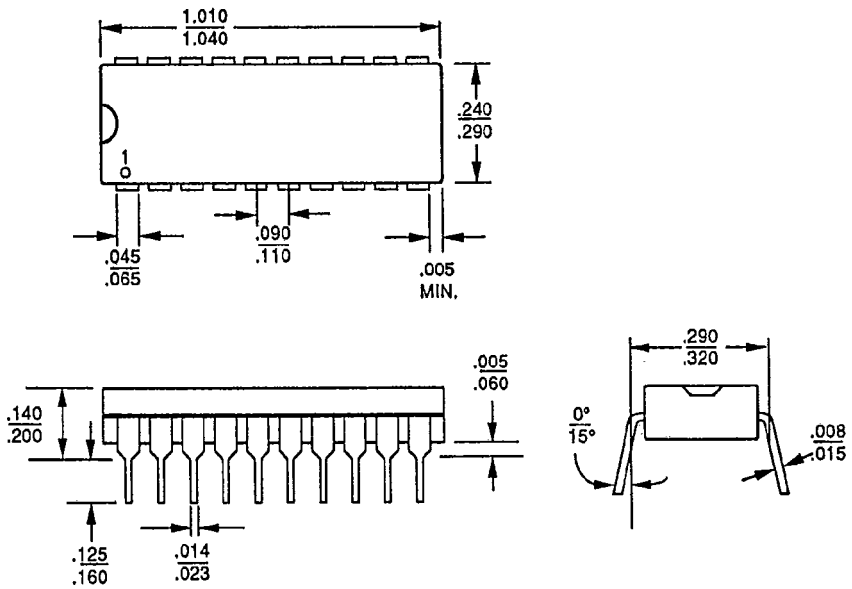
PID #07318C

PHYSICAL DIMENSIONS (continued)

MC 010



PD 020



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