# **Dual N-Channel 12-V (D-S) MOSFET**

### **Key Features:**

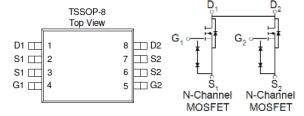
- Low r<sub>DS(on)</sub> trench technology
- · Low thermal impedance
- · Fast switching speed

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	$r_{DS(on)}(m\Omega)$	I□ (A)	
16	11 @ V <sub>GS</sub> = 4.5V	9.6	
10	13 @ $V_{GS} = 2.5V$	8.8	

## **Typical Applications:**

- Power Routing
- · Li Ion Battery Packs
- · Level Shifting and Driver Circuits







ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Limit	Units	
Drain-Source Voltage			16	V	
Gate-Source Voltage	$V_{GS}$	±8	V		
Continuous Dunin Current®	T <sub>A</sub> =25°C		9.6		
Continuous Drain Current <sup>a</sup>	T <sub>A</sub> =70°C	l <sub>D</sub>	7.8	Α	
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	40			
Continuous Source Current (Diode Conduction) a	I <sub>S</sub>	2.2	Α		
Device Dissipation 8	T <sub>A</sub> =25°C	P <sub>D</sub>	1.5	W	
Power Dissipation <sup>a</sup>	T <sub>A</sub> =70°C	] 'D	1	VV	
Operating Junction and Storage Temperature Range	$T_J$ , $T_{stg}$	-55 to 150	°C		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
Maximum Junction-to-Ambient <sup>a</sup>	t <= 10 sec	$R_{\theta JA}$	83	°C/W	
Maximum Junction-to-Ambient	Steady State	IXOJA	120	C/VV	

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#### Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

### **Electrical Characteristics**

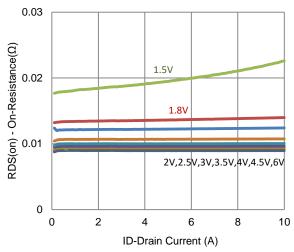
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \text{ uA}$	0.4			V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			±10	uA	
Zoro Coto Voltogo Droin Correct	1	$V_{DS} = 12.8V, V_{GS} = 0 V$			1	uA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 12.8 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			10	T uA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	14			Α	
Drain Cauras On Basistanas a	r	$V_{GS} = 4.5 \text{ V}, I_D = 4.8 \text{ A}$			11	mΩ	
Drain-Source On-Resistance <sup>a</sup>	r <sub>DS(on)</sub>	$V_{GS} = 2.5 \text{ V}, I_D = 4.4 \text{ A}$			13	11122	
Forward Transconductance a	g <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_{D} = 4.8 \text{ A}$		54		S	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 1.1 \text{ A}, V_{GS} = 0 \text{ V}$		0.65		V	
		Dynamic <sup>b</sup>					
Total Gate Charge	$Q_g$	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V},$		21			
Gate-Source Charge	$Q_{gs}$	$I_{DS} = 10 \text{ V}, \text{ V}_{GS} = 4.3 \text{ V},$ $I_{D} = 4.8 \text{ A}$		1.7		nC	
Gate-Drain Charge	$Q_{gd}$	1B = 4.0 A		6.0			
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DS} = 10 \text{ V}, R_{L} = 2.1 \Omega,$		273			
Rise Time	t <sub>r</sub>	$V_{DS} = 10 \text{ V}, \text{ K}_{L} - 2.1 \Omega,$ $I_{D} = 4.8 \text{ A},$		890		ne	
Turn-Off Delay Time	$t_{d(off)}$	$V_{GEN} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$		4870		ns	
Fall Time	t <sub>f</sub>	VGEN - 4.5 V, NGEN - 0 12		3110			
Input Capacitance	C <sub>iss</sub>			1257			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ Mhz}$		257		pF	
Reverse Transfer Capacitance	$C_{rss}$			234			

#### Notes

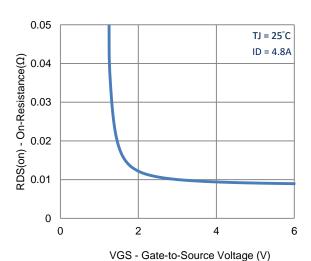
- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.

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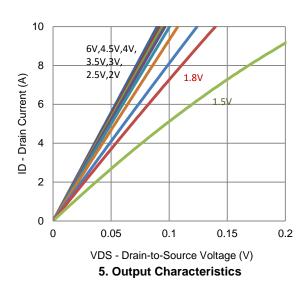
## **Typical Electrical Characteristics**



#### 1. On-Resistance vs. Drain Current



3. On-Resistance vs. Gate-to-Source Voltage



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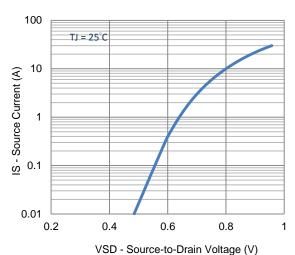
TJ = 25°C

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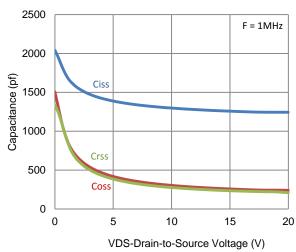
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2. Transfer Characteristics

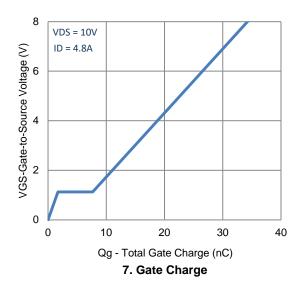


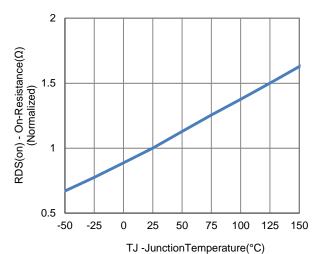
4. Drain-to-Source Forward Voltage



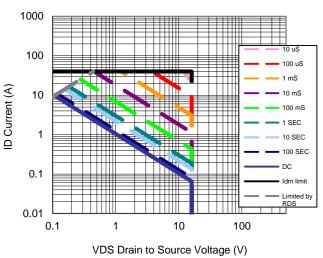
6. Capacitance

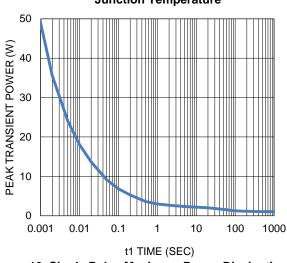
## **Typical Electrical Characteristics**



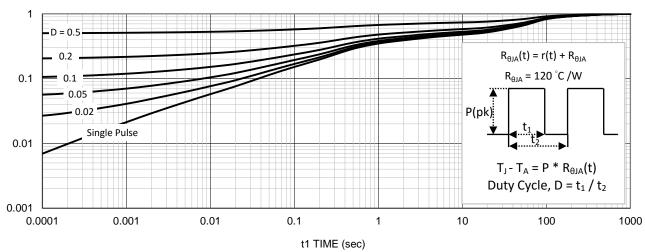


8. Normalized On-Resistance Vs Junction Temperature



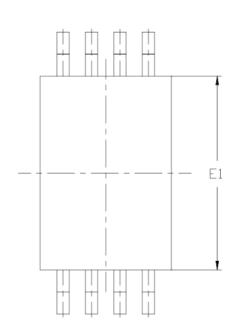


9. Safe Operating Area 10. Single Pulse Maximum Power Dissipation

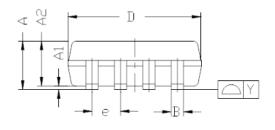


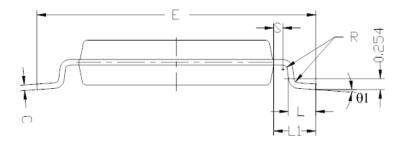
11. Normalized Thermal Transient Junction to Ambient

### **Package Information**



DIM	MILLIMETERS			
DIM.	MIN.	N□M.	MAX.	
Α	1.05	1.10	1.20	
A(1)	0.05	0.10	0.15	
A(2)	0.99	1.02	1.05	
В	0.19	0.25	0,30	
С		0.127		
D	2.90	3.00	3.10	
E	6.20	6.40	6.60	
E1	4.30	4.40	4.50	
9	0.65BSC			
L	0.45	0.60	0.75	
L1	0.90	1.00	1.10	
Υ			0.10	
θ1	0°	4°	8°	
R	0.09			
S	0.20			





#### Note:

- 1. All Dimension Are In mm.
- 2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- 3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
- 4. The Package Top May Be Smaller Than The Package Bottom.
- Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess
  Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The
  Foot.