

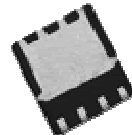
P-Channel 100-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

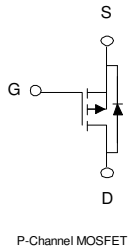
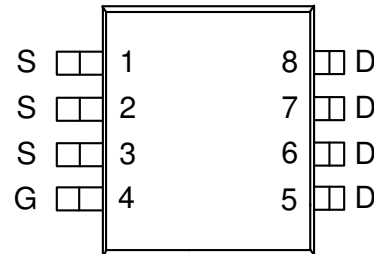
- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN3x3-8PP saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
-100	269 @ $V_{GS} = -10V$	-3
	289 @ $V_{GS} = -5.5V$	-2.9



DFN3x3-8PP
Top View



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Maximum	Units	
Drain-Source Voltage	V_{DS}	-100	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ^a	I_D	$T_A=25^\circ C$	-3	A
		$T_A=70^\circ C$	-2.5	
Pulsed Drain Current ^b	I_{DM}	± 50		
Continuous Source Current (Diode Conduction) ^a	I_S	-2.1	A	
Power Dissipation ^a	P_D	$T_A=25^\circ C$	3.5	W
		$T_A=70^\circ C$	2.0	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	t \leq 10 sec	35
		Steady State	81

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

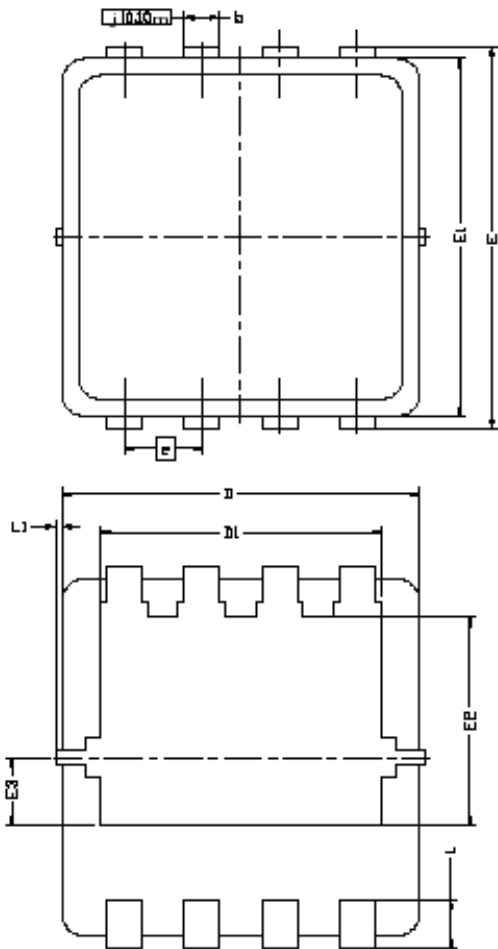
SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 10	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -80 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μA
		$V_{DS} = -80 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-5	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-50			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = -10 \text{ V}, I_D = -1 \text{ A}$			269	m Ω
		$V_{GS} = -5.5 \text{ V}, I_D = -1 \text{ A}$			289	
Forward Transconductance ^A	g_{fs}	$V_{DS} = -15 \text{ V}, I_D = -1 \text{ A}$		29		S
Diode Forward Voltage	V_{SD}	$I_S = 2.5 \text{ A}, V_{GS} = 0 \text{ V}$		-0.8		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15 \text{ V}, V_{GS} = -5.5 \text{ V}, I_D = -1 \text{ A}$		8		nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			3		
Input Capacitance	C_{iss}	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1300		pF
Output Capacitance	C_{oss}			130		
Reverse Transfer Capacitance	C_{rss}			70		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15 \text{ V}, R_L = 6 \Omega, I_D = -1 \text{ A}, V_{GEN} = -10 \text{ V}$		5		nS
Rise Time	t_r			4		
Turn-Off Delay Time	$t_{d(off)}$			60		
Fall-Time	t_f			40		

Notes

- Pulse test: $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information



DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
θ1	0°	10°	12°	0°	10°	12°