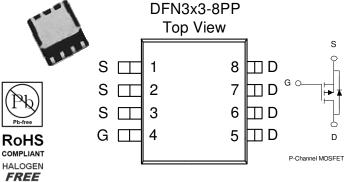
### P-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

•	Low $r_{DS(on)}$ provides higher efficiency and
	extends battery life

- Low thermal impedance copper leadframe DFN3x3-8PP saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$r_{DS(on)} m(\Omega)$	$I_{D}(A)$			
20	$14 @ V_{GS} = -4.5V$	-13			
-20	19 @ V <sub>GS</sub> = -2.5V	-12			



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter			Maximum	Units		
Drain-Source Voltage			-20	V		
Gate-Source Voltage	$V_{GS}$	±8	V			
Continuous Drain Current <sup>a</sup>	$T_A=25^{\circ}C$	Τ_	-13			
Continuous Drain Current	$T_A=25$ °C $T_A=70$ °C	ъ	-11	A		
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	±50				
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	-2.1	A		
D D: : .: a	$T_A=25^{\circ}C$	$P_{\mathrm{D}}$	3.5	W		
Power Dissipation <sup>a</sup>	$\begin{array}{c c} T_A=25^{\circ}C \\ \hline T_A=70^{\circ}C \end{array} P_D$		2.0	l vv		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C			

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Maximum	Units		
a	t <= 10 sec	ъ	35	°C/W		
Maximum Junction-to-Ambient <sup>a</sup>	Steady State	Reja	81	°C/W		

1

#### Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

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SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)							
Parameter	Cymbol	•	Limits			Unit	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static	-						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = -250 \text{ uA}$	-1			V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V$ , $V_{GS} = \pm 8 V$			±100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uA	
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$ $V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-50		-5	Α	
Drain-Source On-Resistance <sup>A</sup>	r <sub>DS(on)</sub>	$V_{GS} = -4.5 \text{ V}, I_D = -11.5 \text{ A}$ $V_{GS} = -2.5 \text{ V}, I_D = -9.3 \text{ A}$			14 19	mΩ	
Forward Tranconductance <sup>A</sup>	g <sub>fs</sub>	$V_{GS} = -15 \text{ V}, I_D = -11.5 \text{ A}$		29	19	S	
Diode Forward Voltage	$V_{SD}$	$I_{S} = 2.5 \text{ A}, V_{GS} = 0 \text{ V}$		-0.8		V	
Dynamic <sup>b</sup>							
Total Gate Charge	$Q_{g}$	V 45.V.V 4.5.V		25		nC	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V},$ $I_{D} = -11.5 \text{ A}$		11			
Gate-Drain Charge	$Q_{gd}$	ID = -11.3 A		17			
Input Capacitance	C <sub>iss</sub>			2300			
Output Capacitance	ut Capacitance C <sub>oss</sub> V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz			600		рF	
Reverse Transfer Capacitance	$C_{rss}$			300			
Turn-On Delay Time	$t_{d(on)}$			15			
Rise Time	t <sub>r</sub>	$V_{DD} = -15 \text{ V}, \text{ R}_L = 6 \Omega ,$ $I_D = -1 \text{ A}, V_{GEN} = -10 \text{ V}$		13		nS	
Turn-Off Delay Time	$t_{d(off)}$			100			
Fall-Time	t <sub>f</sub>			54			

#### Notes

a. Pulse test:  $PW \le 300$ us duty cycle  $\le 2\%$ .

b. Guaranteed by design, not subject to production testing.

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## Typical Electrical Characteristics (P-Channel)

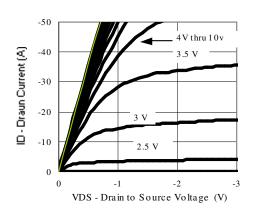


Figure 1. On-Region Characteristics

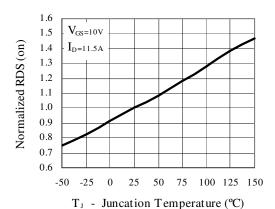
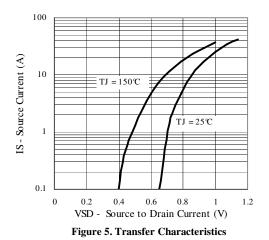


Figure 3. On-Resistance Variation with Temperature



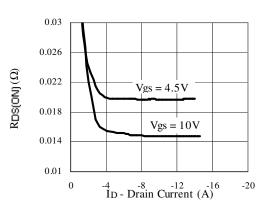


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

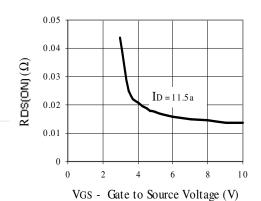


Figure 4. On-Resistance with Gate to Source Voltage

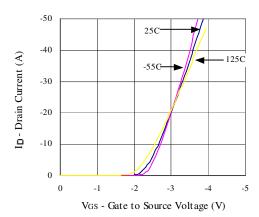


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

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## Typical Electrical Characteristics (P-Channel)

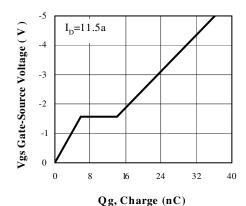


Figure 7. Gate Charge Characteristics

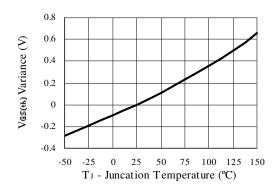


Figure 9. Maximum Safe Operating Area

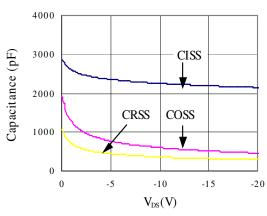


Figure 8. Capacitance Characteristics

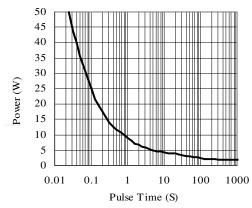


Figure 10. Single Pulse Maximum Power Dissipation

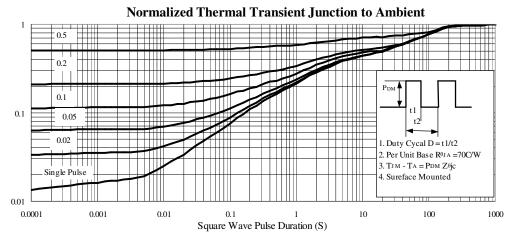
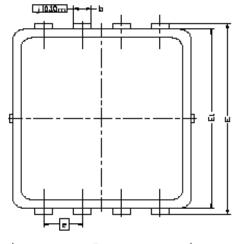
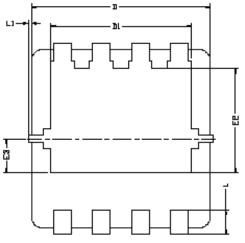
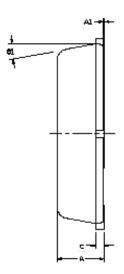


Figure 11. Transient Thermal Response Curve

# Package Information







птм	MILLIMETERS			INCHES			
DIM.	MIN	NDM	MAX	MIN	NDM	MAX	
Α	0,700	0'80	0.900	0.0276	0.0315	0.0354	
A1	0.00		0.05	0.000		0.002	
la	0.24	0.30	0.35	0.009	0.012	0.014	
C	0.10	0.152	0.25	0,004	0.006	0,010	
ם	3.00 BSC			0.118 BSC			
D1	5	2£ 25.	:C	0.093 BSC			
Ε	3,20 BSC			0.126 BSC			
E1	3.00 BSC			0.118 BSC			
E5	1.75 BSC			0.069 BSC			
E3	0.575 BSC			0.	023 BS	3C	
6	Ů	0.65 BSC			0.026 BSC		
L	0,30	0,40	0,50	0.0118	0.0157	0.0197	
L1			0.100	0		0.004	
<b>Q1</b>	0°	10*	12*	0*	10°	12*	