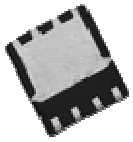
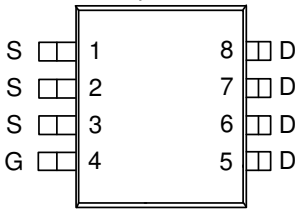
N-Channel 80-V (D-S) MOSFET

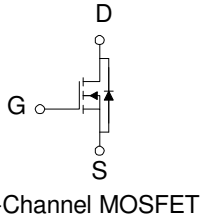
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
80	35 @ V_{GS} = 10V	9
	40 @ V_{GS} = 4.5V	8



DFN3x3-8PP
Top View





N-Channel MOSFET

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN3x3-8PP saves board space
- Fast switching speed
- High performance trench technology

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Limit**	**Units**
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[a]	T_A=25°C	I_D	±9	A
	T_A=70°C		±7	
Pulsed Drain Current[b]		I_{DM}	±75	
Continuous Source Current (Diode Conduction)[a]		I_S	16	A
Power Dissipation[a]	T_A=25°C	P_D	3.5	W
	T_A=70°C		2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Case[a]	t <= 5 sec	$R_{\theta JC}$	25	°C/W
Maximum Junction-to-Ambient[a]	t <= 5 sec	$R_{\theta JA}$	50	°C/W

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

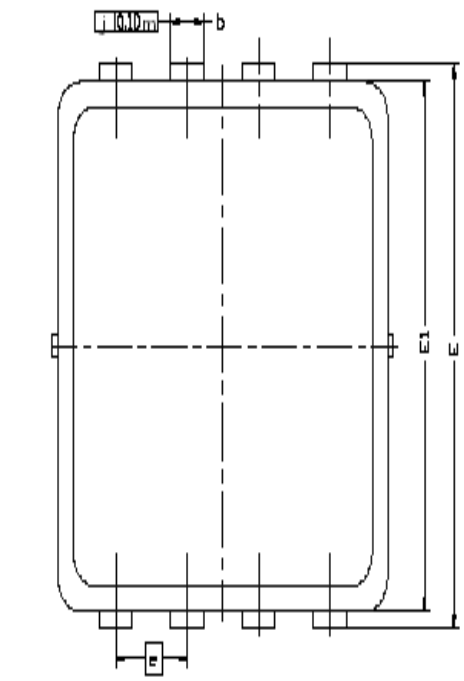
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 uA	1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 64 V, V_{GS} = 0 V			1	uA
		V_{DS} = 64 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	20			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 1 A			35	mΩ
		V_{GS} = 4.5 V, I_D = 1 A			40	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 15 V, I_D = 9 A		40		S
Diode Forward Voltage	V_{SD}	I_S = 2.3 A, V_{GS} = 0 V		0.7		V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 9 A		28		nC
Gate-Source Charge	Q_{gs}			13		
Gate-Drain Charge	Q_{gd}			6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 25 V, R_L = 25 Ω , I_D = 1 A, V_{GEN} = 10 V		6		nS
Rise Time	t_r			2		
Turn-Off Delay Time	$t_{d(off)}$			24		
Fall-Time	t_f			2		

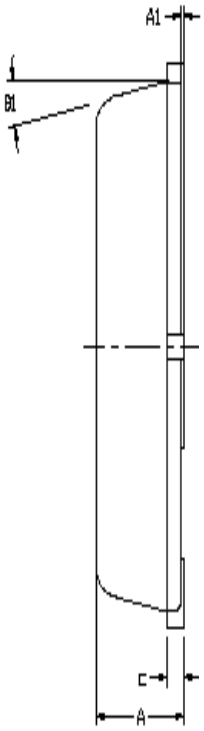
Notes

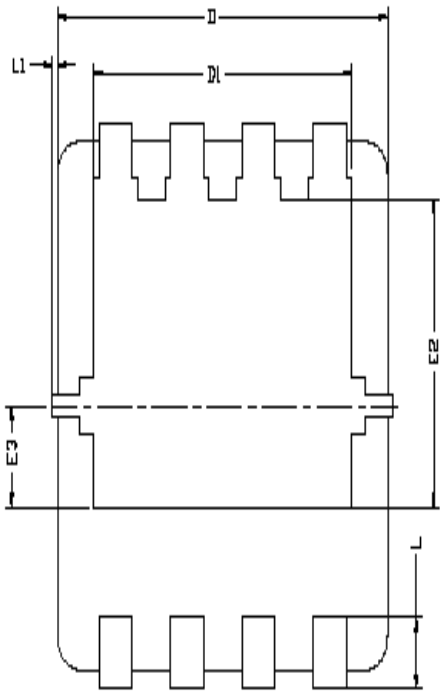
a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information







DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
θ1	0°	10°	12°	0°	10°	12°