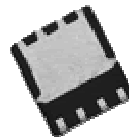


N-Channel 30-V (D-S) MOSFET

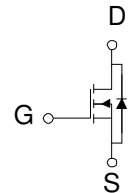
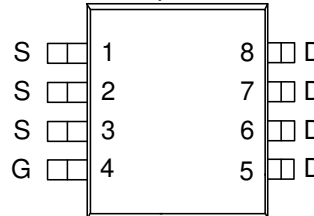
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8PP saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	7.5 @ $V_{GS} = 10V$	22
	11.5 @ $V_{GS} = 4.5V$	18

SOIC-8PP
Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	20	
Continuous Drain Current ^a	I_D	$T_A=25^\circ C$	22
		$T_A=70^\circ C$	18
Pulsed Drain Current ^b	I_{DM}	50	A
Continuous Source Current (Diode Conduction) ^a	I_S	2.3	A
Power Dissipation ^a	P_D	$T_A=25^\circ C$	5
		$T_A=70^\circ C$	2.2
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Maximum	Units	
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	25	$^\circ C/W$	
	Steady State	65	$^\circ C/W$	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

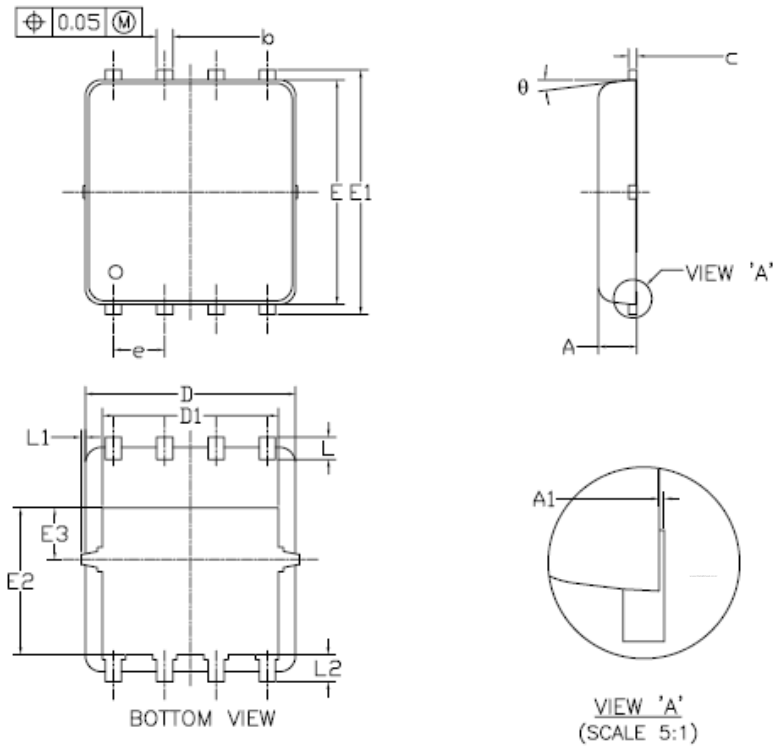
SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
		$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$			7.5	mΩ
		$V_{GS} = 4.5 \text{ V}, I_D = 2 \text{ A}$			11.5	
Forward Transconductance ^A	g_s	$V_{DS} = 15 \text{ V}, I_D = 2 \text{ A}$		40		S
Diode Forward Voltage	V_{SD}	$I_S = 2 \text{ A}, V_{GS} = 0 \text{ V}$		0.7		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 10 \text{ A}$		16		nC
Gate-Source Charge	Q_{gs}			5		
Gate-Drain Charge	Q_{gd}			6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15 \text{ V}, R_L = 6 \Omega, I_D = 1 \text{ A},$ $V_{GEN} = 10 \text{ V}$		5		nS
Rise Time	t_r			4		
Turn-Off Delay Time	$t_{d(off)}$			23		
Fall-Time	t_f			9		

Notes

- Pulse test: $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	—	0.05	0.000	—	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.20 BSC			0.205 BSC		
D1	4.35 BSC			0.171 BSC		
E	5.55 BSC			0.219 BSC		
E1	6.05 BSC			0.238 BSC		
E2	3.625 BSC			0.143 BSC		
E3	1.275 BSC			0.050 BSC		
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	—	0.15	0	—	0.006
L2	0.68 REF			0.027 REF		
theta	0°	—	10°	0°	—	10°