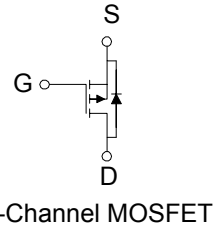
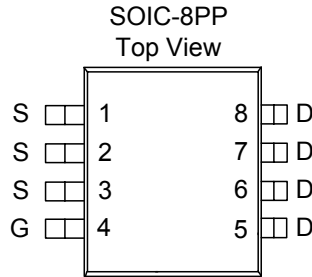
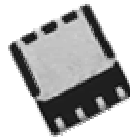


### P-Channel 60-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low  $r_{DS(on)}$  provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8PP saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
-60	45 @ $V_{GS} = -10V$	-10
	60 @ $V_{GS} = -4.5V$	-8



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$I_D$	$T_A = 25^\circ C$	-10
		$T_A = 70^\circ C$	-8
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	$\pm 50$	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	-2.1	A
Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ C$	5.0
		$T_A = 70^\circ C$	3.2
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	t $\leq$ 10 sec	25
		Steady State	65

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

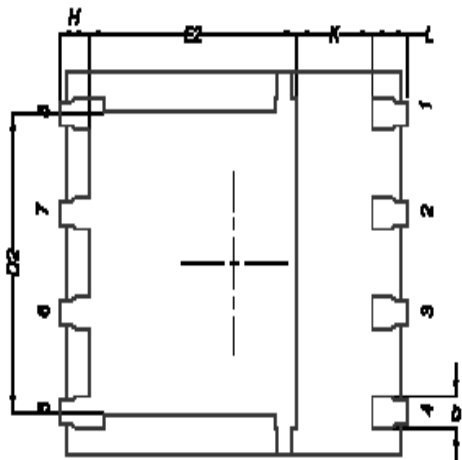
SPECIFICATIONS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
<b>Static</b>						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-1			
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -48 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uA
		$V_{DS} = -48 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-5	
On-State Drain Current <sup>A</sup>	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-50			A
Drain-Source On-Resistance <sup>A</sup>	$r_{DS(on)}$	$V_{GS} = -10 \text{ V}, I_D = -9.0 \text{ A}$			45	m $\Omega$
		$V_{GS} = -4.5 \text{ V}, I_D = -7.2 \text{ A}$			60	
Forward Transconductance <sup>A</sup>	$g_s$	$V_{DS} = -15 \text{ V}, I_D = -9.0 \text{ A}$		31		S
Diode Forward Voltage	$V_{SD}$	$I_S = -2.1 \text{ A}, V_{GS} = 0 \text{ V}$		-0.7		V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V},$ $I_D = -9.0 \text{ A}$		15.3		nC
Gate-Source Charge	$Q_{gs}$			5.2		
Gate-Drain Charge	$Q_{gd}$			5.8		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15 \text{ V}, R_L = 15 \Omega, I_D = -1 \text{ A},$ $V_{GEN} = -10 \text{ V}, R_G = 6\Omega$		15		nS
Rise Time	$t_r$			12		
Turn-Off Delay Time	$t_{d(off)}$			62		
Fall-Time	$t_f$			46		

## Notes

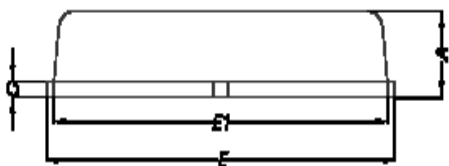
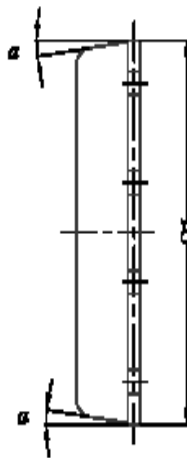
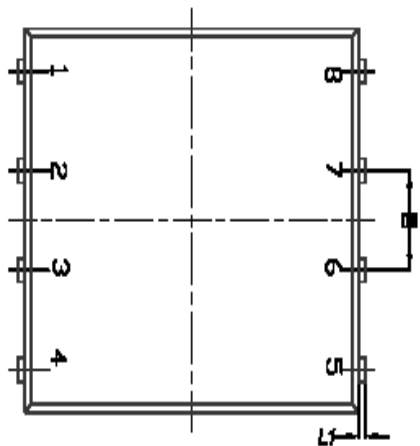
- Pulse test:  $PW \leq 300 \mu\text{s}$  duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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# Package Information



**BACKSIDE VIEW**



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.90	4.90	5.00
D2	3.81	3.81	3.98
E	5.00	6.00	6.10
E1	5.70	6.75	5.00
E2	3.38	3.58	3.78
Ø	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.08	0.13	0.20
α	0°	-	12°