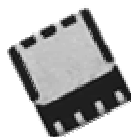


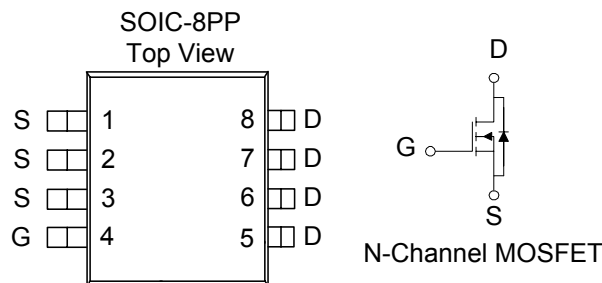
### N-Channel 60-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low  $r_{DS(on)}$  provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8PP saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ m( $\Omega$ )	$I_D$ (A)
60	82 @ $V_{GS} = 10V$	6.4
	115 @ $V_{GS} = 4.5V$	5.4



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	20	
Continuous Drain Current <sup>a</sup>	$I_D$	$T_A = 25^\circ C$	6.4
		$T_A = 70^\circ C$	5.3
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	20	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	2.3	A
Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ C$	5.0
		$T_A = 70^\circ C$	3.2
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	$t \leq 10$ sec	25
		Steady State	65

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

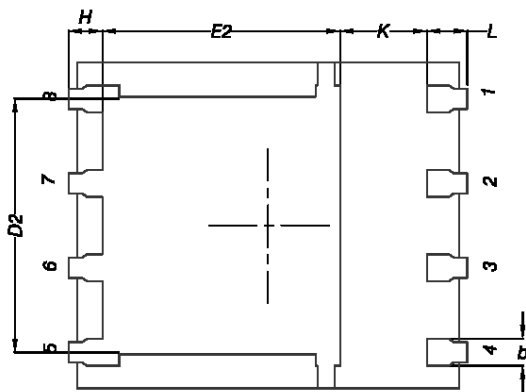
SPECIFICATIONS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
<b>Static</b>						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\ \text{V}, V_{GS} = 12\ \text{V}$			100	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 48\ \text{V}, V_{GS} = 0\ \text{V}$			1	uA
		$V_{DS} = 48\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current <sup>A</sup>	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 10\ \text{V}$	40			A
Drain-Source On-Resistance <sup>A</sup>	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 2\ \text{A}$			82	m $\Omega$
		$V_{GS} = 4.5\ \text{V}, I_D = 2\ \text{A}$			115	
Forward Transconductance <sup>A</sup>	$g_{fs}$	$V_{DS} = 15\ \text{V}, I_D = 6\ \text{A}$		40		S
Diode Forward Voltage	$V_{SD}$	$I_S = 2.3\ \text{A}, V_{GS} = 0\ \text{V}$		0.7		V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 15\ \text{V}, V_{GS} = 4.5\ \text{V},$ $I_D = 6\ \text{A}$		15		nC
Gate-Source Charge	$Q_{gs}$			3		
Gate-Drain Charge	$Q_{gd}$			5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}, R_L = 6\ \Omega, I_D = 1\ \text{A},$ $V_{GEN} = 10\ \text{V}$		15		nS
Rise Time	$t_r$			10		
Turn-Off Delay Time	$t_{d(off)}$			54		
Fall-Time	$t_f$			26		

## Notes

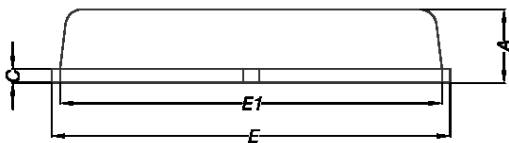
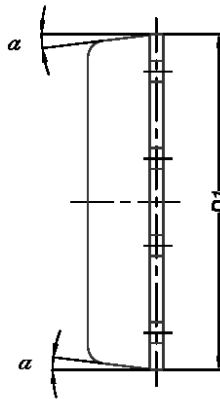
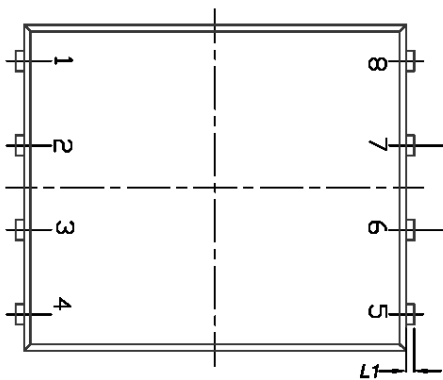
- Pulse test:  $PW \leq 300\ \mu\text{s}$  duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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# Package Information



BACKSIDE VIEW



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
$\phi$	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
$\alpha$	0°	-	12°