Am25LS192 • Am25LS193
Am54LS/74LS192 • Am54LS/74LS193

Decimal and Hexadecimal Up/Down Counters

DISTINCTIVE CHARACTERISTICS

- Separate up and down clocks
- Asynchronous parallel load
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL} at I_{OL} = 8mA
  - Twice the fan-out over military range
  - 440μA source current at HIGH output
- 100% product assurance screening to MIL-STD-883 requirements

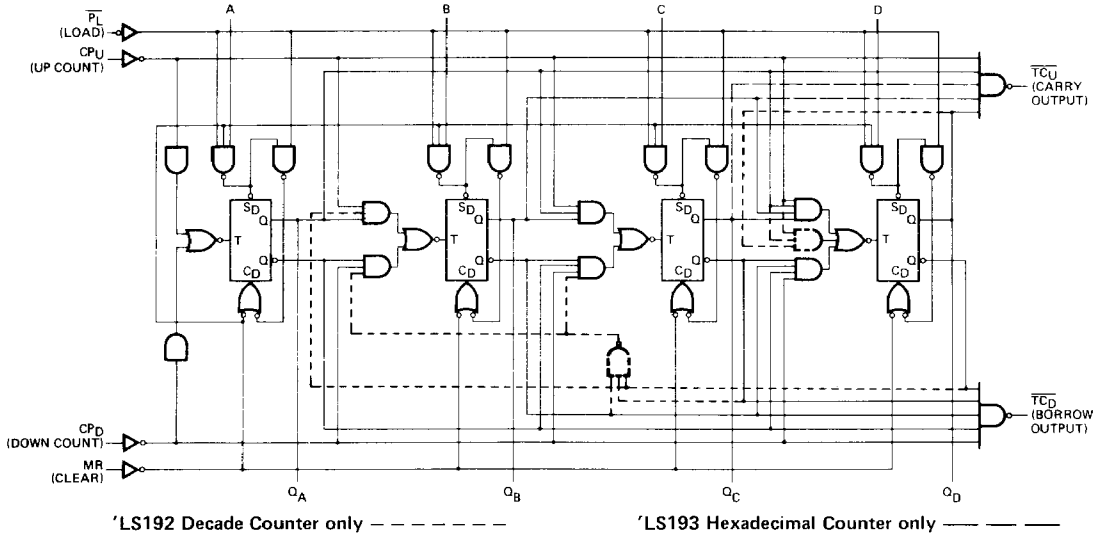
FUNCTIONAL DESCRIPTION

The 'LS192 and 'LS193 are four-bit up/down counters using advanced Low-Power Schottky processing. The 'LS192 counts in the BCD mode and the 'LS193 counts in the binary mode. These counters have separate count-up and count-down clock inputs (CP_U and CP_D, respectively). The Q_i outputs change state synchronously on the LOW-to-HIGH transition on either the up clock input or the down clock input. Only one clock input can be LOW at a time or erroneous counting will result.

Each of the four flip-flops can be preset to a logic HIGH or a logic LOW by means of four parallel inputs (A, B, C, and D). When the parallel load input ($\overline{PL}$) goes LOW, all four flip-flops set to the state of the direct inputs (A, B, C, and D) independent of the clock inputs. An active HIGH master reset (MR) is provided which overrides both the clock and parallel load inputs forcing all Q_i outputs LOW.

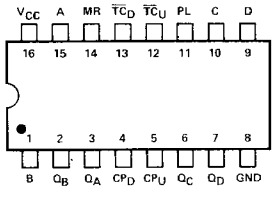
Two terminal count outputs are gated with the clock inputs to provide clock signal to other counters. The TC_D output goes LOW when the counter is in state 0000 and the count down clock goes LOW. The TC_U goes LOW when the count up goes LOW and the counter is in state 1001 ('LS192) or state 1111 ('LS193). The TC_U and TC_D outputs can drive the count up and count down clocks on the next counter in a series. The Q_i outputs of such a connection scheme are not synchronous on cascaded counters in this series.

LOGIC DIAGRAM



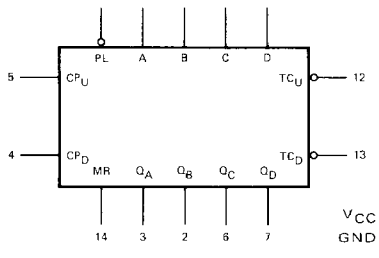
'LS192 Decade Counter only — — — — — — 'LS193 Hexadecimal Counter only ——— ——— ———

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



Am25LS192 • Am25LS193

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25LS192XC/Am25LS193XC	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$ (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am25LS192XM/Am25LS193XM	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$ (MIL)	MIN. = 4.50V	MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$		0.25	0.40	Volts
			$I_{OL} = 8.0mA$		0.35	0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)			19	34	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. ICC is measured with all outputs open; clear and load inputs grounded; and all other inputs at 4.5V

3

Am25LS • Am54LS/74LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am54LS/74LS192 • Am54LS/74LS193

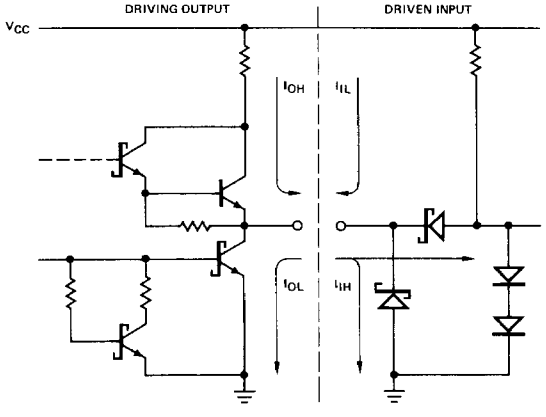
ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74LS192X/74LS193X	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$ (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am54LS192X/54LS193X	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V + 10\%$ (MIL)	MIN. = 4.50V	MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -400\mu A$, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	All, $I_{OL} = 4.0mA$		0.25	0.40	Volts
			74LS only, $I_{OL} = 8.0mA$		0.35	0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)			19	34	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limites are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all outputs open; clear and load inputs grounded; and all other inputs at 4.5V

Am25LS • 54LS/74LS
LOW-POWER SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

SWITCHING CHARACTERISTICS

(T_A = 25°C, V_{CC} = 5.0V)

Parameters	Description		Am25LS Min.	Am25LS Typ.	Am25LS Max.	Am54LS/74LS Min.	Am54LS/74LS Typ.	Am54LS/74LS Max.	Units	Test Conditions
t_{PLH}	CP_U or CP_D to Q_n			24	34		25	38	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				28	39		31	47		
t_{PLH}	CP_U to TC_U			10	15		17	26	ns	
t_{PHL}				10	15		21	33		
t_{PLH}	CP_D to TC_D			10	15		16	24	ns	
t_{PHL}				11	17		21	33		
t_{PLH}	A-D to Q_n Output			13	18			–	ns	
t_{PHL}				27	38			–		
t_{PLH}	A-D to TC_U Output			35	49			–	ns	
t_{PHL}				19	27			–		
t_{PLH}	A-D to TC_D Output			26	36			–	ns	
t_{PHL}				28	39			–		
t_{PHL}	MR Input to Q_n Output			20	29		22	35	ns	
t_{PLH}	MR Input to TC_U Output			25	35			–	ns	
t_{PHL}	MR Input to TC_D Output			16	22			–	ns	
t_{PLH}	P_L Input to Q_n Output			20	29		27	40	ns	
t_{PHL}				25	36		29	40		
t_{PLH}	P_L Input to TC_U Output			31	45			–	ns	
t_{PHL}				30	42			–		
t_{PLH}	P_L Input to TC_D Output			30	42			–	ns	
t_{PHL}				24	34			–		
t_s	Data Set-up Time A-D Input to P_L Input	Load 1	5.0			–			ns	
		Load 0	15			20			ns	
t_s	Set-up Time, P_L Input to CP_U or CP_D		9.0			–			ns	
t_s	Set-up Time, Clear Recovery (In-Active) to CP_U or CP_D		5.0			–			ns	
t_h	Data		0			0			ns	
$t_{pw(0)}$	Pulse Width	CP_U	11			20			ns	
		CP_D	11			20				
		P_L	9.0			20				
$t_{pw(1)}$	Pulse Width	MR	15			20			ns	
f_{max}	Maximum Clock Frequency, Count Up or Down (Note 1)		35	45		25	32		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

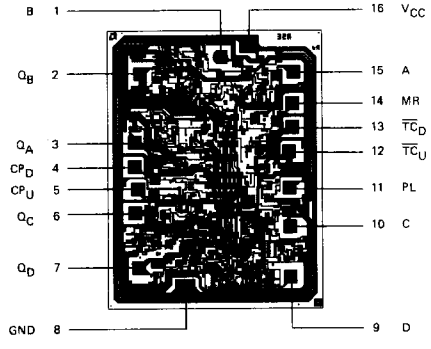
Am25LS192, Am25LS193 ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Min.	Am25LS COM'L Max.	Am25LS MIL $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	CP_U or CP_D to Q_n			44		52	ns	$C_L = 50pF$, $R_L = 2.0k\Omega$
t_{PHL}				54		67		
t_{PLH}	CP_U to TC_U			22		26	ns	
t_{PHL}				23		27		
t_{PLH}	CP_D to TC_D			22		26	ns	
t_{PHL}				23		27		
t_{PLH}	A-D to Q_n Output			26		31	ns	
t_{PHL}				52		63		
t_{PLH}	A-D to TC_U Output			66		80	ns	
t_{PHL}				38		46		
t_{PLH}	A-D to TC_D Output			50		60	ns	
t_{PHL}				54		66		
t_{PHL}	MR Input to Q_n Output			41		50	ns	
t_{PLH}	MR Input to TC_U Output			49		60	ns	
t_{PHL}	MR Input to TC_D Output			32		38	ns	
t_{PLH}	P_L Input to Q_n Output			41		50	ns	
t_{PHL}				53		67		
t_{PLH}	P_L Input to TC_U Output			63		79	ns	
t_{PHL}				60		75		
t_{PLH}	P_L Input to TC_D Output			60		75	ns	
t_{PHL}				48		60		
t_s	Data Set-up Time A-D Input to P_L Input	Load 1	5.0		5.0		ns	
		Load 0	20		23			
t_s	Set-up Time, P_L Input to CP_U or CP_D		13		18		ns	
t_s	Set-up Time, Clear Recovery (In-Active) to CP_U or CP_D		7.0		9.0		ns	
t_h	Data		0		0		ns	
$t_{pw(0)}$	Pulse Width	CP_U	15		17		ns	
		CP_D	15		17			
		P_L	13		17			
$t_{pw(1)}$	Pulse Width	MR	18		21			
f_{max}	Maximum Clock Frequency, Count Up or Down (Note 1)		25		20		MHz	

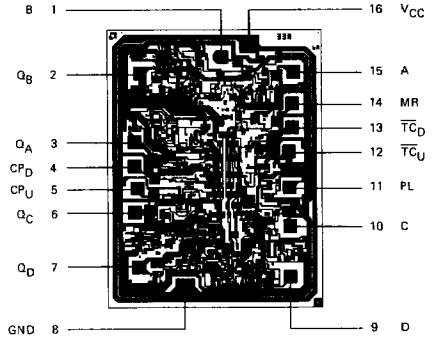
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Metallization and Pad Layout

'LS192



'LS193



DIE SIZE 0.075" X 0.096"

FUNCTION TABLE

INPUTS								OUTPUTS						Conditions
Clock				Data										
Up	Down	Clear	Load	A	B	C	D	Q_A	Q_B	Q_C	Q_D	Borrow	Carry	
X	L	H	X	X	X	X	X	L	L	L	L	L	H	Clear
X	H	H	X	X	X	X	X	L	L	L	L	H	H	
X	X	L	L	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3	X	X	Load
H	↑	L	H	X	X	X	X	Count Down				H	H	Except at borrow
H	L	L	H	X	X	X	X	L	L	L	L	L	H	Borrow
H	H	L	H	X	X	X	X	L	L	L	L	H	H	
↑	H	L	H	X	X	X	X	Count up				H	H	Except at carry
L	H	L	H	X	X	X	X	H	H	H	H	H	L	Carry (193 only)
H	H	L	H	X	X	X	X	H	H	H	H	H	H	
L	H	L	H	X	X	X	X	H	L	L	H	H	L	Carry (192 only)
H	H	L	H	X	X	X	X	H	L	L	H	H	H	

H = HIGH X = Don't care D = A LOW or a HIGH and the respective output
L = LOW ↑ = LOW-to-HIGH transition will assume the same state.

DEFINITION OF FUNCTIONAL TERMS

MR Clear. The clear input to the counter overrides all other inputs. When the clear input is HIGH, the Q outputs are set LOW independent of the other inputs.

$\overline{PL}$ Load. The load input performs asynchronous parallel load of the data on the A, B, C, and D inputs. When the load input is LOW, the Q_i outputs will follow the parallel inputs regardless of the clock inputs.

A, B, C, D The four parallel inputs to the counter flip-flops.

CP_U Count up. A clock input causing the counter to change state in an increasing binary number direction. Counting occurs on the LOW-to-HIGH transition of the clock.

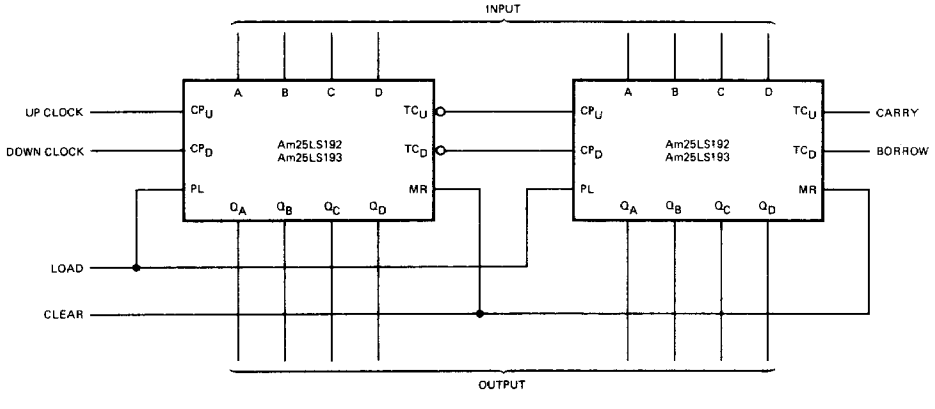
CP_D Count down. A clock input causing the counter to change state in a decreasing binary number direction. The state change occurs on the LOW-to-HIGH transition.

Q_A, Q_B, Q_C, Q_D The four outputs of the counter representing the LSB to MSB, respectively.

$\overline{TC_U}$ Carry output. A clock output that indicates the maximum upper binary number has been reached. For the 'LS192, TC_U indicates that the "9" state has been reached and the up clock is LOW. For the 'LS193, TC_U indicates that the "15" state has been reached and the up clock is LOW.

$\overline{TC_D}$ Borrow output. A clock output indicating that the "0" state has been reached and the down clock is LOW.

APPLICATION



8-Bit Up/Down Counter with Parallel Load