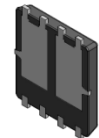
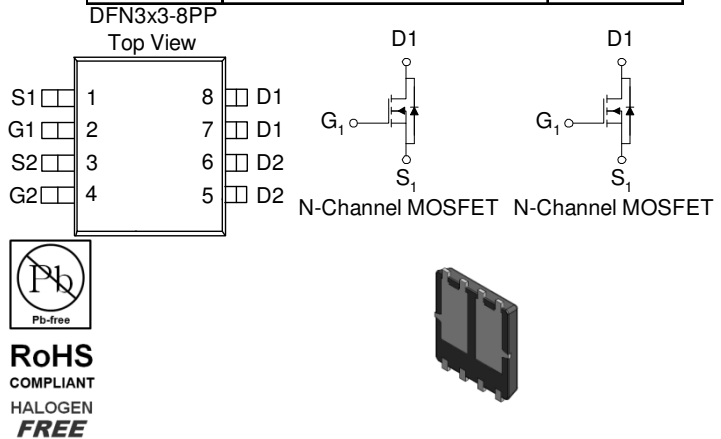


Dual N-Channel 40-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN3x3-8PP saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
40	35 @ $V_{GS} = 10V$	7.0
	46 @ $V_{GS} = 4.5V$	6.1



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	20	
Continuous Drain Current ^a	I_D	$T_A=25^\circ C$	7
		$T_A=70^\circ C$	5.7
Pulsed Drain Current ^b	I_{DM}	± 20	A
Continuous Source Current (Diode Conduction) ^a	I_S	7	A
Power Dissipation ^a	P_D	$T_A=25^\circ C$	2.5
		$T_A=70^\circ C$	1.3
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	50	$^\circ C/W$
	Steady State	7	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

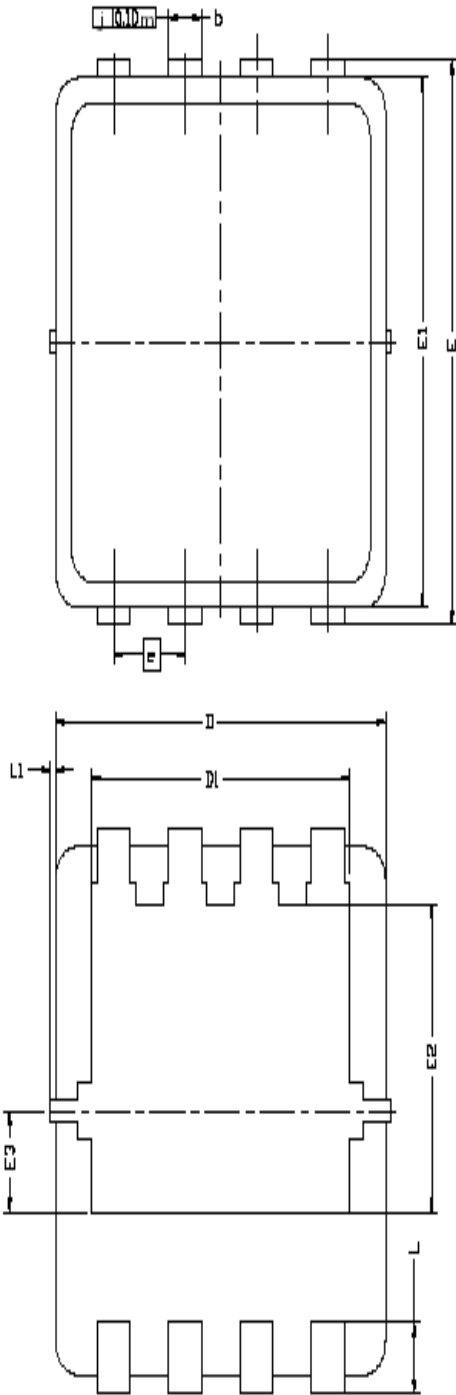
SPECIFICATIONS (T _A = 25 ^o C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 μA	1			V
Gate-Body Leakage	I _{GSS}	V _{GS} = 20 V, V _{DS} = 0 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 32 V, V _{GS} = 0 V			1	μA
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	20			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 1 A			35	mΩ
		V _{GS} = 4.5 V, I _D = 1 A			46	
Forward Transconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 1 A		26		S
Dynamic						
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, V _{GS} =4.5V, I _D =1A		7		nC
Gate-Source Charge	Q _{gs}			2		
Gate-Drain Charge	Q _{gd}			2		
Input Capacitance	C _{iss}	N-Channel V _{DS} =15V, V _{GS} =0V, f=1MHz		400		pF
Output Capacitance	C _{oss}			80		
Reverse Transfer Capacitance	C _{rss}			40		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} =15V, V _{GS} =10V, I _D =1A , R _{GEN} =25Ω		2		nS
Rise Time	t _r			3		
Turn-Off Delay Time	t _{d(off)}			12		
Fall-Time	t _f			4		

Notes

- Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

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Package Information



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
AL	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
LL	D	---	0.100	D	---	0.004
BL	0°	10°	12°	0°	10°	12°