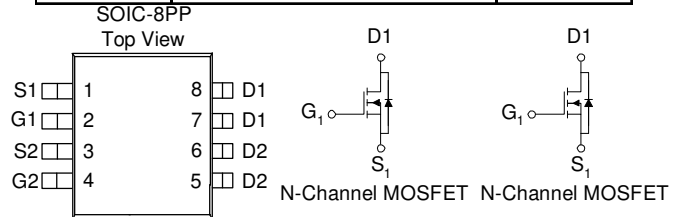


Dual N-Channel 20-V (D-S) MOSFET

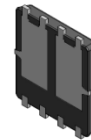
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8PP saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
20	10 @ $V_{GS} = 4.5V$	33
	13 @ $V_{GS} = 2.5V$	29



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	8	
Continuous Drain Current ^a	I_D	$T_A=25^\circ C$	33
		$T_A=70^\circ C$	27
Pulsed Drain Current ^b	I_{DM}	± 50	A
Continuous Source Current (Diode Conduction) ^a	I_S	13	A
Power Dissipation ^a	P_D	$T_A=25^\circ C$	16
		$T_A=70^\circ C$	10
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	t <= 10 sec	$R_{\theta JA}$	35	$^\circ C/W$
	Steady State	$R_{\theta JC}$	8	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

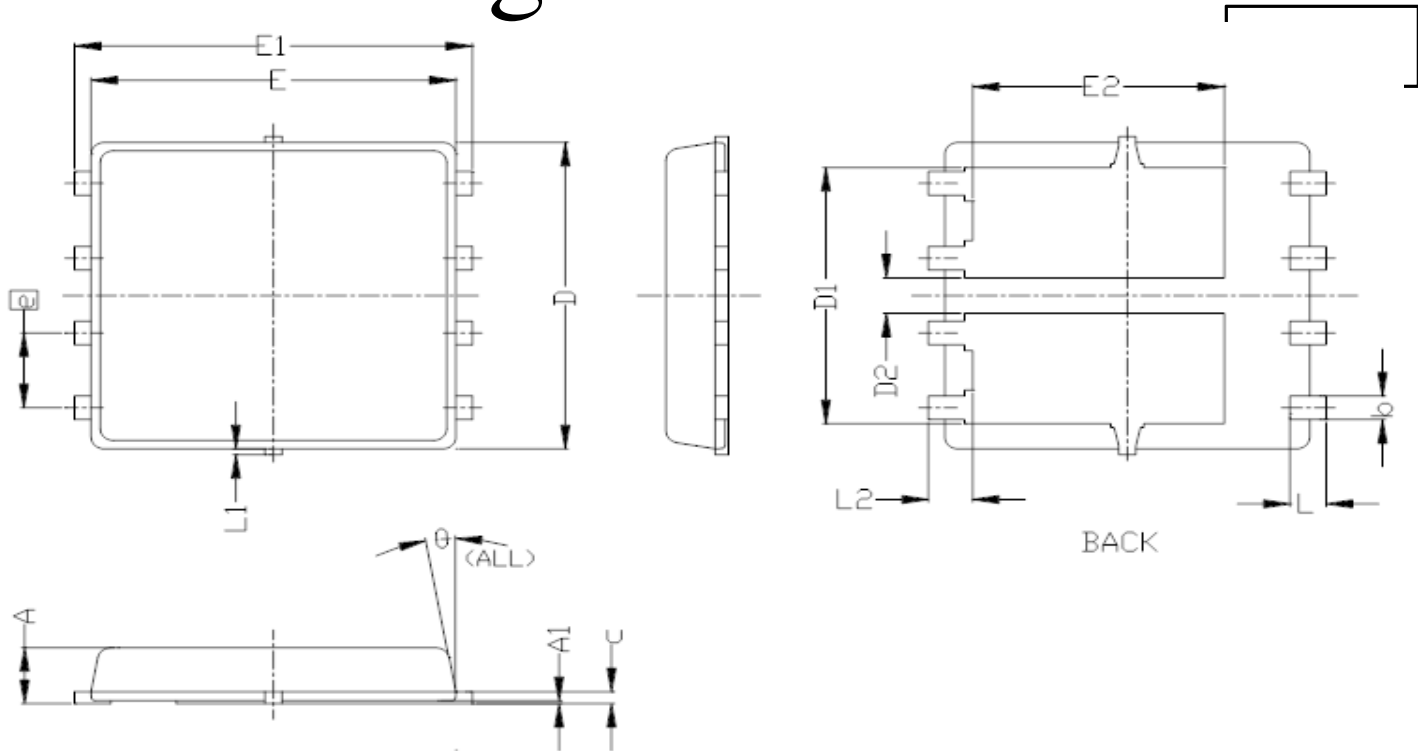
SPECIFICATIONS ($T_A = 25^{\circ}\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{GS} = 8 \text{ V}, V_{DS} = 0 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 1 \text{ A}$			10	m Ω
		$V_{GS} = 2.5 \text{ V}, I_D = 1 \text{ A}$			13	
Forward Transconductance ^A	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 1 \text{ A}$		40		S
Dynamic						
Total Gate Charge	Q_g	N-Channel $V_{DS}=15\text{V}, V_{GS}=4.5\text{V}, I_D=1\text{A}$		30		nC
Gate-Source Charge	Q_{gs}			5		
Gate-Drain Charge	Q_{gd}			10		
Input Capacitance	C_{iss}	N-Channel $V_{DS}=15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$		3000		pF
Output Capacitance	C_{oss}			300		
Reverse Transfer Capacitance	C_{rss}			200		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD}=15\text{V}, V_{GS}=10\text{V}, I_D=1\text{A}$, $R_{GEN}=25\Omega$		10		nS
Rise Time	t_r			20		
Turn-Off Delay Time	$t_{d(off)}$			60		
Fall-Time	t_f			10		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	—	0.05	0.000	—	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.20 BSC			0.205 BSC		
D1	4.35 BSC			0.171 BSC		
D2	0.50	0.60	0.75	0.020	0.024	0.030
E	5.55 BSC			0.219 BSC		
E1	6.05 BSC			0.238 BSC		
E2	3.82 BSC			0.150 BSC		
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	—	0.15	0	—	0.006
L2	0.68 REF			0.027 REF		
θ	0°	—	10°	0°	—	10°