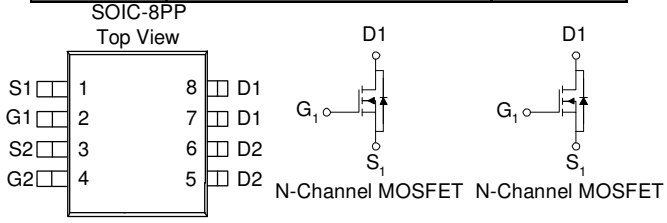
Dual N-Channel 20-V (D-S) MOSFET

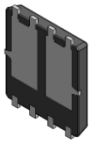
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8PP saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
20	10 @ V_{GS} = 4.5V	33
	13 @ V_{GS} = 2.5V	29



Pb-free
RoHS COMPLIANT
HALOGEN FREE



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NO				
Parameter		**Symbol**	**Limit**	**Units**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	8	
Continuous Drain Current[a]	T_A=25°C	I_D	33	A
	T_A=70°C		27	
Pulsed Drain Current[b]		I_{DM}	±50	
Continuous Source Current (Diode Conduction)[a]		I_S	13	A
Power Dissipation[a]	T_A=25°C	P_D	16	W
	T_A=70°C		10	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Ambient[a]	t <= 10 sec	$R_{\theta JA}$	35	°C/W
	Steady State	$R_{\theta JC}$	8	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

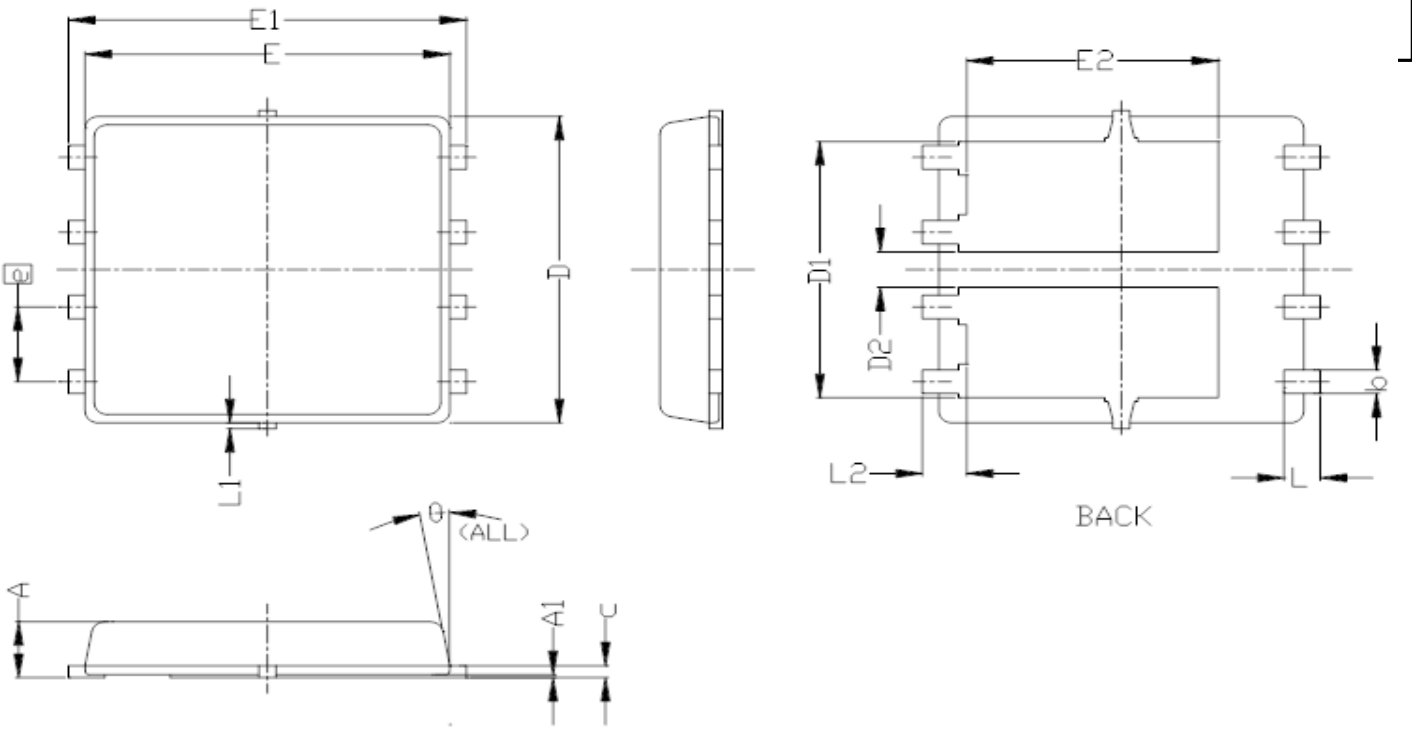
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Limits**			**Unit**
			Min	**Typ**	**Max**	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	VGS = VDS, ID = 250 uA	1			V
Gate-Body Leakage	I_{GSS}	V_{GS} = 8 V, V_{DS} = 0 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V			1	uA
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	20			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	VGS = 4.5 V, ID = 1 A			10	mΩ
		VGS = 2.5 V, ID = 1 A			13	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 15 V, I_D = 1 A		40		S
Dynamic						
Total Gate Charge	Q_g	N-Channel V_{DS}=15V, V_{GS}=4.5V, I_D=1A		30		nC
Gate-Source Charge	Q_{gs}			5		
Gate-Drain Charge	Q_{gd}			10		
Input Capacitance	C_{iss}	N-Channel V_{DS}=15V, V_{GS}=0V, f=1MHz		3000		pF
Output Capacitance	C_{oss}			300		
Reverse Transfer Capacitance	C_{rss}			200		
Turn-On Delay Time	$t_{d(on)}$	N-Chaneel V_{DD}=15V, VGS=10V, ID=1A , R_{GEN}=25Ω		10		nS
Rise Time	t_r			20		
Turn-Off Delay Time	$t_{d(off)}$			60		
Fall-Time	t_f			10		

Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0. 85	0. 95	1. 00	0. 033	0. 037	0. 039
A1	0. 00	——	0. 05	0. 000	——	0. 002
b	0. 30	0. 40	0. 50	0. 012	0. 016	0. 020
c	0. 15	0. 20	0. 25	0. 006	0. 008	0. 010
D		5. 20 BSC			0. 205 BSC	
D1		4. 35 BSC			0. 171 BSC	
D2	0. 50	0. 60	0. 75	0. 020	0. 024	0. 030
E		5. 55 BSC			0. 219 BSC	
E1		6. 05 BSC			0. 238 BSC	
E2		3. 82 BSC			0. 150 BSC	
e		1. 27 BSC			0. 050 BSC	
L	0. 45	0. 55	0. 65	0. 018	0. 022	0. 026
L1	0	---	0. 15	0	---	0. 006
L2		0. 68 REF			0. 027 REF	
θ	0°	---	10°	0°	---	10°